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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY8C20xx7/S
RAM Size	2K x 8
Interface	I²C, SPI
Number of I/O	27
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	30-XFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.2x2.3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20767-24fdxct

Contents

Additional System Resources

System resources provide additional capability, such as configurable I^2C slave, SPI master/slave communication interface, three 16-bit programmable timers, various system resets supported by the M8C low voltage detection and power-on reset. The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I^2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I^2C enhanced slave interface appears as a 32-byte RAM buffer to the external I^2C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For more details, refer to the I2CSBUF User Module datasheet.
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20x37/47/67/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Application Notes/Design Guides

Application notes and design guides are an excellent introduction to the wide variety of possible PSoC designs. They are located at www.cypress.com/gocapsense. Select Application Notes under the Related Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark. See “Development Kits” on page 31.

Training

Free PSoC and CapSense technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

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Designing with PSoC Designer

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate and Verify

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

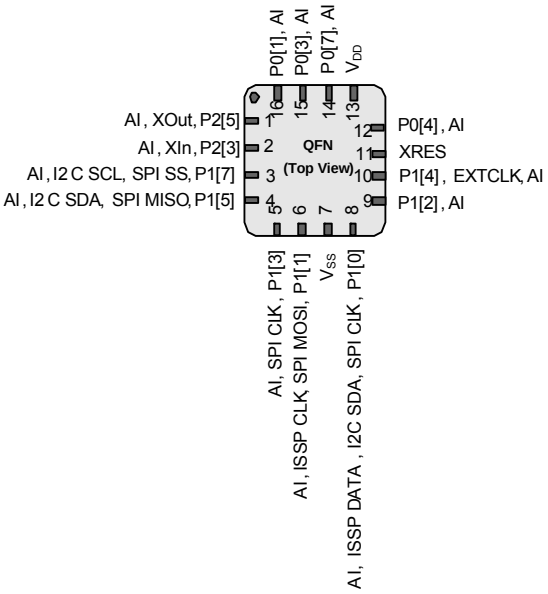
16-pin QFN (10 Sensing Inputs)[8]

Table 2. Pin Definitions – CY8C20237, CY8C20247/S [9]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I^2C SCL, SPI SS
4	IOHR	I	P1[5]	I^2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[10], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection[13]
8	IOHR	I	P1[0]	ISSP DATA[10], I^2C SDA, SPI CLK[11]
9	IOHR	I	P1[2]	Driven Shield Output (optional)
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down[12]
12	IOH	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20237, CY8C20247/S Device



Notes
8. No center pad.
9. 13 GPIOs = 10 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
10. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
11. Alternate SPI clock.
12. The internal pull down is 5KOhm.
13. All VSS pins should be brought out to one common GND plane.

30-ball WLCSP (24 Sensing Inputs)

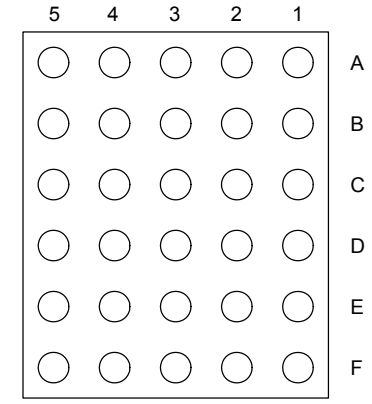
Table 4. Pin Definitions – CY8C20767, CY8C20747 30-ball Part Pinout (WLCSP) [20]

Pin No.	Type		Name	Description
	Digital	Analog		
A1	IOH	I	P0[2]	Driven Shield Output (optional)
A2	IOH	I	P0[6]	
A3	Power		V_{DD}	Supply voltage
A4	IOH	I	P0[1]	Integrating Input
A5	I/O	I	P2[7]	
B1	I/O	I	P4[2]	
B2	IOH	I	P0[0]	Driven Shield Output (optional)
B3	IOH	I	P0[4]	
B4	IOH	I	P0[3]	Integrating Input
B5	I/O	I	P2[5]	Crystal Output (Xout)
C1	I/O	I	P2[2]	Driven Shield Output (optional)
C2	I/O	I	P2[4]	Driven Shield Output (optional)
C3	I/O	I	P0[7]	
C4	IOH	I	P3[2]	
C5	I/O	I	P2[3]	Crystal Input (Xin)
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[1]	
D4	I/O	I	P3[3]	
D5	I/O	I	P2[1]	
E1	Input		XRES	Active high external reset with internal pull-down[21]
E2	IOHR	I	P1[6]	
E3	IOHR	I	P1[4]	Optional external clock input (EXT CLK)
E4	IOHR	I	P1[7]	I^2C SCL, SPI SS
E5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
F1	IOHR	I	P1[2]	Driven Shield Output (optional)
F2	IOHR	I	P1[0]	ISSP DATA[22], I^2C SDA, SPI CLK[23]
F3	Power		V_{SS}	Supply ground[24]
F4	IOHR	I	P1[1]	ISSP CLK[22], I^2C SCL, SPI MOSI
F5	IOHR	I	P1[3]	SPI CLK

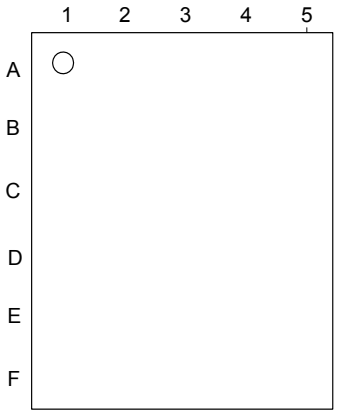
LEGEND: A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20767, CY8C20747 30-ball WLCSP

Bottom View



Top View



Notes

20. 27 GPIOs = 24 pins for capacitive sensing+2 pins for I^2C + 1 pin for modulator capacitor.
21. The internal pull down is 5KOhm.
22. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
23. Alternate SPI clock.
24. All VSS pins should be brought out to one common GND plane.

DC Chip-Level Specifications

Table 9 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 9. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD} [37, 38, 39]	Supply voltage	See Table 14 on page 17.	1.71	–	5.50	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
I_{SB0} [40, 41, 42, 43]	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.1	µA
I_{SB1} [40, 41, 42, 43]	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C} [40, 41, 42, 43]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

37. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
38. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register. For the referenced registers, refer to the Technical Reference Manual. In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected and resets the device when V_{DD} goes lower than 1.1 V at edge rates slower than 1 V/ms.
39. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
40. Errata: When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the “Errata” on page 37.
41. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the “Errata” on page 37.
42. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the “Errata” on page 37.
43. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the “Errata” on page 37.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.80	V
V_{IH}	Input high voltage	–	V_{DD} × 0.65	–	V_{DD} + 0.7	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (Absolute Value)	–	–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT3.3}$	Input Low Voltage with low threshold enable set, Enable for Port1 [44]	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT3.3}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
$V_{ILLVT5.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT5.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

Note

44. Errata: Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C20xx7/S VDD. For more information see item #7 in "Errata" on page 37.

Comparator User Module Electrical Specifications

Table 16 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ TA ≤ 85 °C, 1.71 V ≤ V_{DD} ≤ 5.5 V.

Table 16. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset	–	Valid from 0.2 V to 1.5 V	–	2.5	30	mV
Current	–	Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range	–	–	0.2		1.5	V

ADC Electrical Specifications

Table 17. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications on page 21 for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8, 9, or 10 bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

DC POR and LVD Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR0}	1.66 V selected in PSoC Designer	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V_{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	V
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	V
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	V
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[46]	2.71	2.78	V
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[47]	2.92	2.99	V
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[48]	3.02	3.09	V
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	V
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	V
V_{LVD6}	1.80 V selected in PSoC Designer		1.75[49]	1.80	1.84	V
V_{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	V

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations	–	1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See appropriate "DC GPIO Specifications" on page 15	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See appropriate "DC GPIO Specifications" on page 15	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify	–	–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate "DC GPIO Specifications" on page 15. For V_{DD} > 3V use V_{OH4} in Table 10 on page 15.	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes
46. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
47. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
48. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
49. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

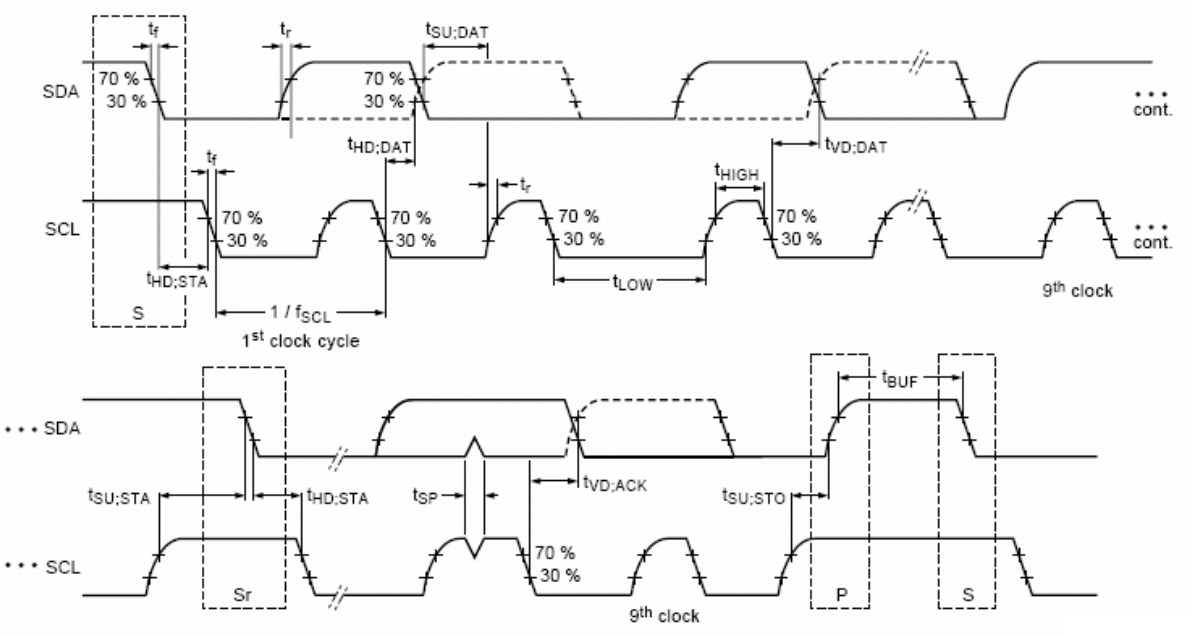
AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$[55]	Data hold time	20	3.45	20	0.90	µs
$t_{SU;DAT}$	Data setup time	250	–	100[56]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

55. Errata: To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. For more information see item #5 in the "Errata" on page 37.
56. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 30. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	60 100	– –	– –	ns ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

Figure 12. SPI Master Mode 0 and 2

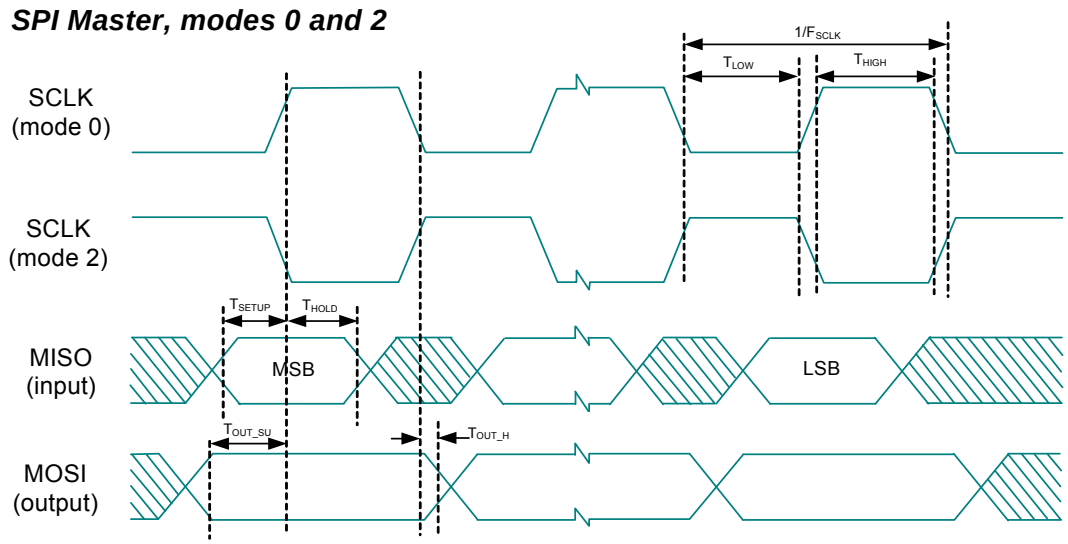
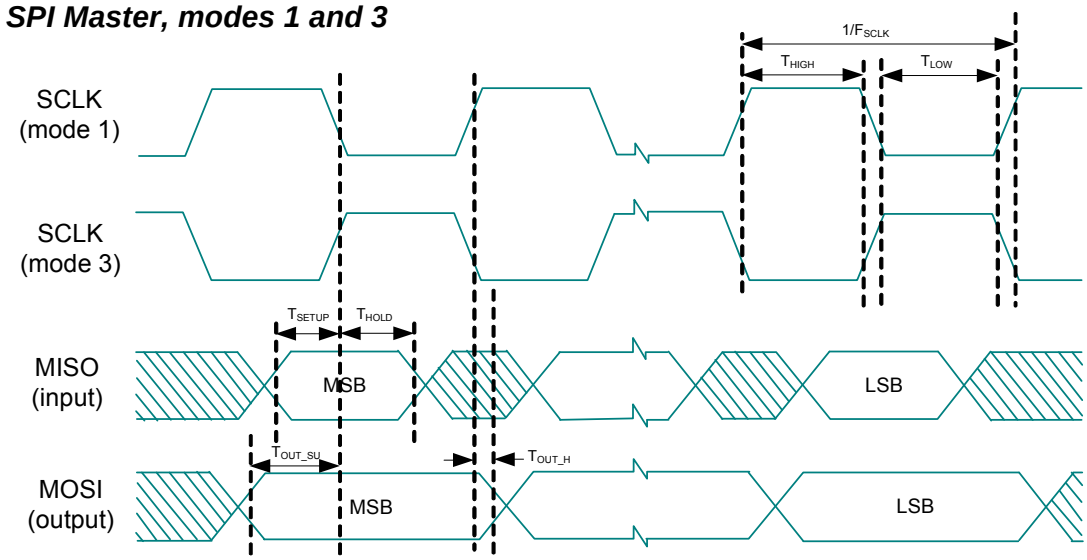


Figure 13. SPI Master Mode 1 and 3



Packaging Information

This section illustrates the packaging specifications for the CY8C20x37/47/67 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 16. 16-pin (150 Mil) SOIC

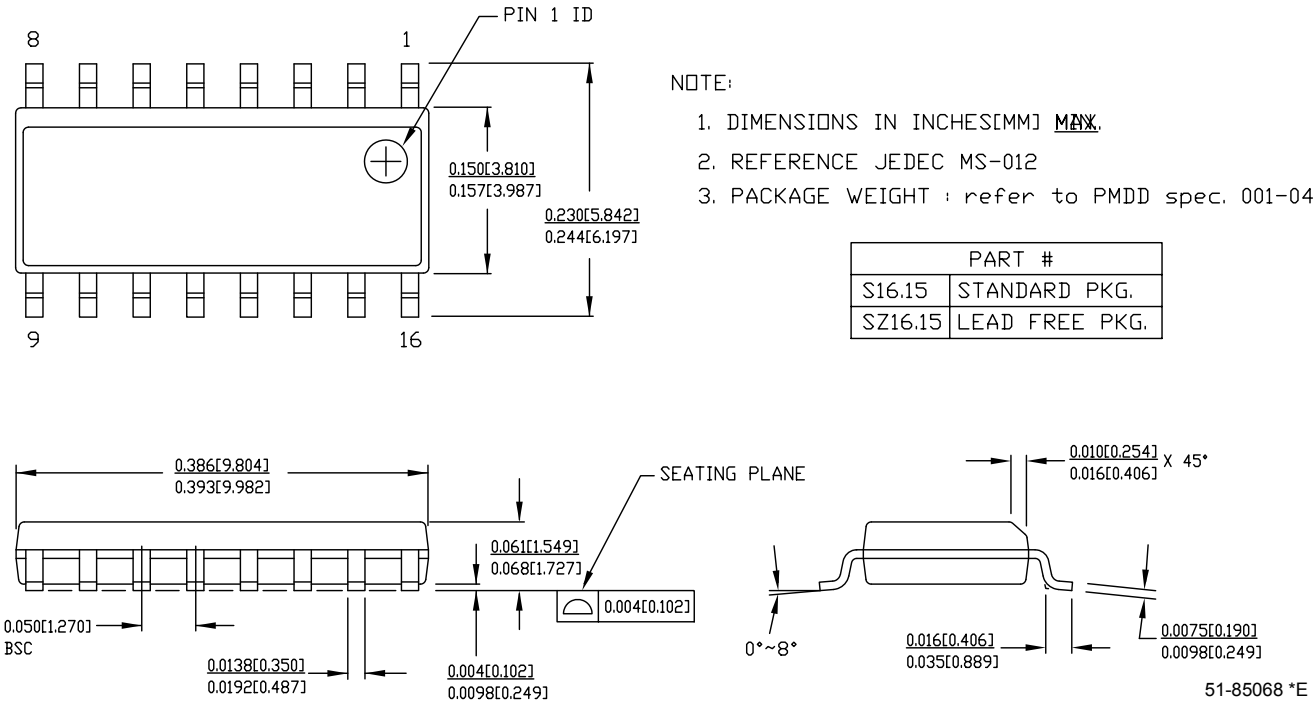


Figure 17. 16-pin Chip-On-Lead (3 × 3 × 0.6 mm) (Sawn) Package Outline, 001-09116

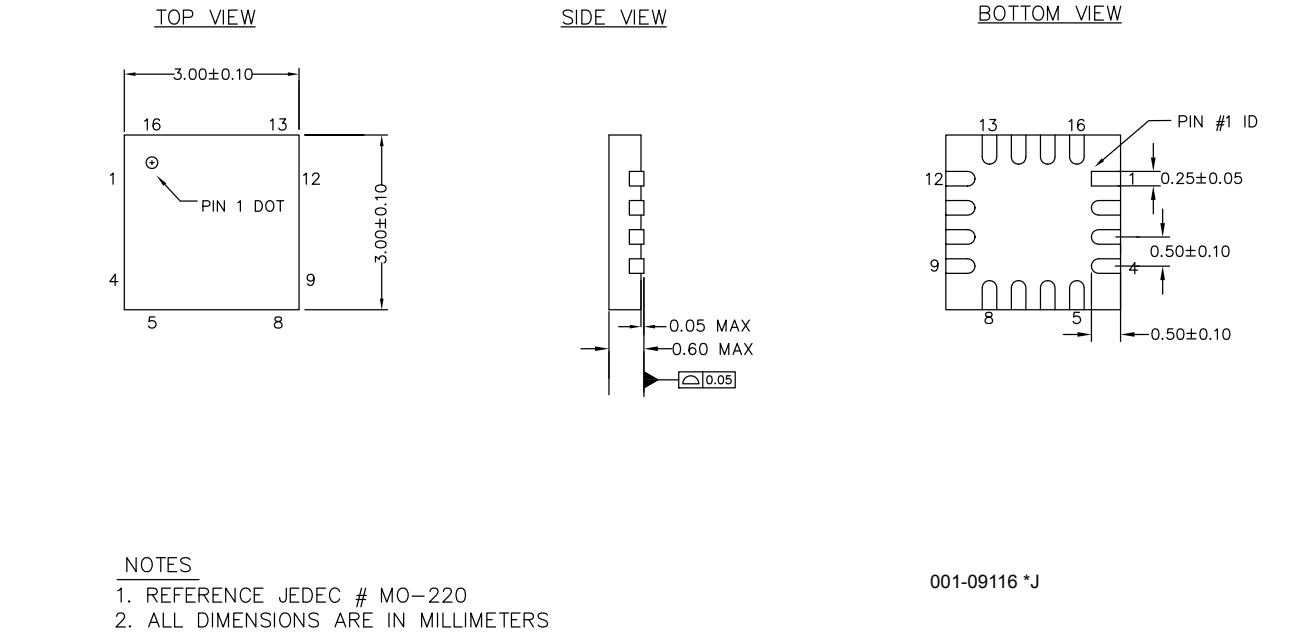
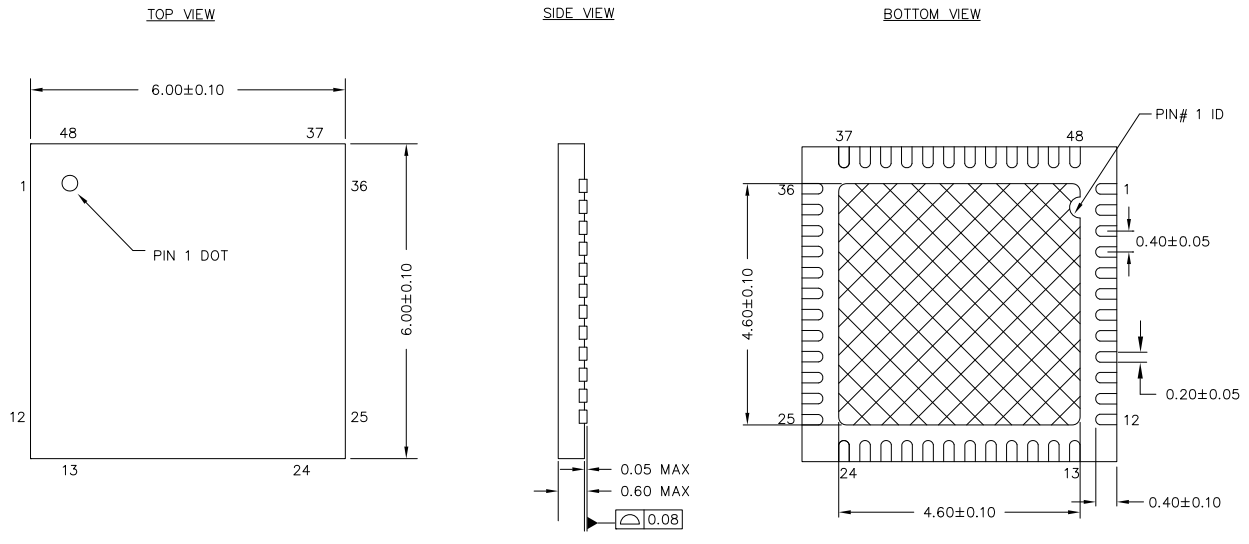


Figure 20. 48-Pin (6 × 6 × 0.6 mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 32. Thermal Impedances per Package

Package	Typical θ_{JA} [57]
16-pin SOIC	95 °C/W
16-pin QFN	33 °C/W
24-pin QFN[58]	21 °C/W
32-pin QFN[58]	20 °C/W
48-pin QFN[58]	18 °C/W
30-ball WLCSP	54 °C/W

Capacitance on Crystal Pins

Table 33. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-Pin QFN	3.2 pF
48-Pin QFN	3.3 pF

Solder Reflow Peak Temperature

Table 34 shows the solder reflow temperature limits that must not be exceeded.

Table 34. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin SOIC	260 °C	30 seconds
16-pin QFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

Notes
57. $T_J = T_A + \text{Power} \times \theta_{JA}$.
58. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, in-system programming support, and built-in support for third-party assemblers and C compilers. PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

PSoC Designer Software Subsystems

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube in-circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at http://www.cypress.com/psocprogrammer.

Development Kits

All development kits are sold at the Cypress Online Store.

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

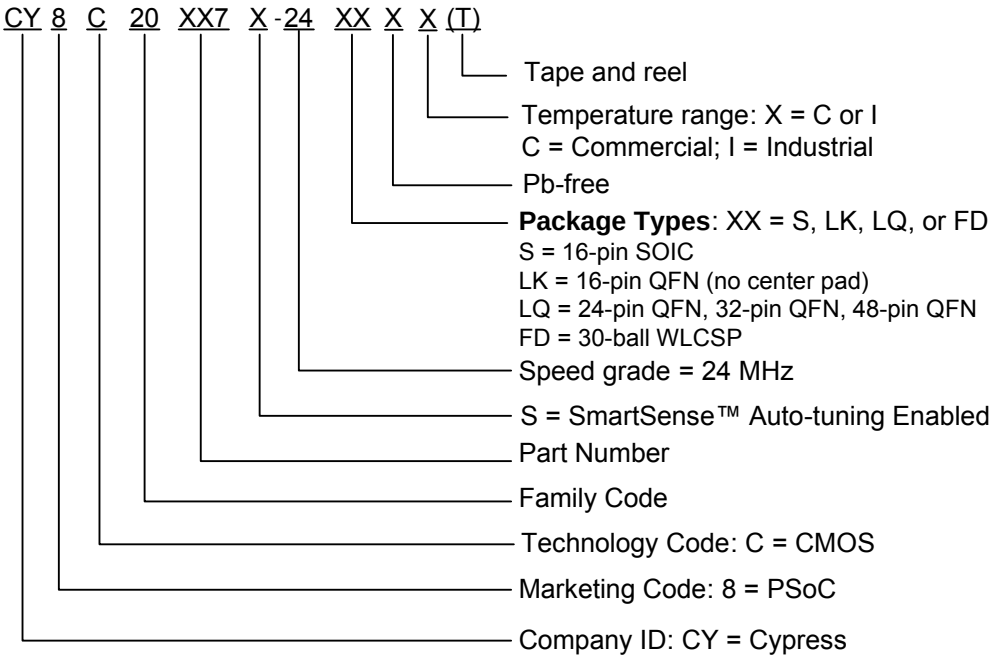
Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Table 35. PSoC Device Key Features and Ordering Information *(continued)*

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	CapSense Sensors	Digital I/O Pins	Analog Inputs [59]	XRES Pin	ADC
CY8C20767-24FDXC	30-pin WLCSP	32 K	2 K	24	27	27	Yes	Yes
CY8C20767-24FDXCT	30-pin WLCSP (Tape and Reel)	32 K	2 K	24	27	27	Yes	Yes

Ordering Code Definitions



Document History Page *(continued)*

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	4248645	DST	01/16/2014	Updated Pinouts: Updated 32-pin QFN (25 Sensing Inputs)[25]: Updated Figure 6. Updated Packaging Information: spec 001-09116 – Changed revision from *H to *I.
*L	4404150	SLAN	06/10/2014	Updated Pinouts: Updated 16-pin SOIC (10 Sensing Inputs): Updated Table 1: Added Note 6 and referred the same note in description of XRES pin. Updated 16-pin QFN (10 Sensing Inputs)[8]: Updated Table 2: Added Note 12 and referred the same note in description of XRES pin. Updated 24-pin QFN (16 Sensing Inputs)[14]: Updated Table 3: Added Note 18 and referred the same note in description of XRES pin. Updated 30-ball WLCSP (24 Sensing Inputs): Updated Table 4: Added Note 21 and referred the same note in description of XRES pin. Updated 32-pin QFN (25 Sensing Inputs)[25]: Updated Table 5: Added Note 29 and referred the same note in description of XRES pin. Updated 48-pin QFN (31 Sensing Inputs)[31]: Updated Table 6: Added Note 35 and referred the same note in description of XRES pin. Updated Electrical Specifications: Updated DC GPIO Specifications: Updated Table 10: Updated minimum and maximum values of V_{IH} parameter. Updated Table 11: Updated minimum and maximum values of V_{IH} parameter. Updated AC Chip-Level Specifications: Updated Table 24: Removed minimum and maximum values of “ILO untrimmed frequency”. Updated Packaging Information: spec 001-09116 – Changed revision from *I to *J. Completing Sunset Review.
*M	4825924	SLAN	07/07/2015	Added the footnote “All VSS pins should be brought out to one common GND plane” in pinout tables (Table 1 through Table 6). Updated Packaging Information: spec 001-13937 – Changed revision from *E to *F. Updated to new template.
*N	5068999	ARVI	12/31/2015	Updated hyperlink of “Technical Reference Manual” in all instances across the document. Updated PSoC® Functional Overview: Updated Additional System Resources: Updated description. Updated Development Tool Selection: Removed “Accessories (Emulation and Programming)”. Removed “Build a PSoC Emulator into Your Board”.

Document History Page *(continued)*

Document Title: CY8C20xx7/S, 1.8 V CapSense® Controller with SmartSense™ Auto-tuning 31 Buttons, 6 Sliders, Proximity Sensors Document Number: 001-69257				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*O	5122184	JFMD	02/02/2016	Updated Features: Removed Note “Please contact your nearest sales office for additional details.” and its reference. Updated Ordering Information: Updated Table 35: Updated part numbers.

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