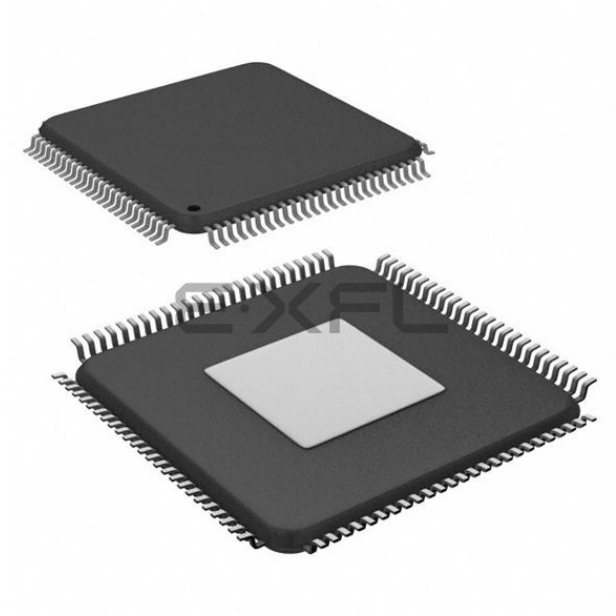

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP Exposed Pad
Supplier Device Package	100-eTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc572l64e3bc6ay

Table of contents

1 Introduction 7

1.1 Document overview 7

1.2 Description 7

1.3 Device feature summary 7

1.4 Block diagram 8

1.5 Features overview 11

2 Package pinouts and signal descriptions 13

2.1 Package pinouts 13

2.2 Pin descriptions 14

2.2.1 Power supply and reference voltage pins 14

2.2.2 System pins 15

2.2.3 LVDS pins 16

2.2.4 Generic pins 16

3 Electrical characteristics 18

3.1 Introduction 18

3.2 Parameter classification 18

3.3 Absolute maximum ratings 19

3.4 Electromagnetic Compatibility (EMC) 20

3.5 Electrostatic discharge (ESD) 20

3.6 Operating conditions 20

3.7 DC electrical specifications 22

3.8 I/O pad specification 23

3.8.1 I/O input DC characteristics 24

3.8.2 I/O output DC characteristics 28

3.9 I/O pad current specification 33

3.10 Reset pad (PORST, ESR0) electrical characteristics 36

3.11 Oscillator and PLL 39

3.12 ADC specifications 43

3.12.1 ADC input description 43

3.12.2 SAR ADC electrical specification 46

Table 45. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1) . . . 85
Table 46. RMII serial management channel timing . . . 87
Table 47. RMII receive signal timing . . . 88
Table 48. RMII transmit signal timing . . . 89
Table 49. UART frequency support . . . 90
Table 50. GPIO delay timing . . . 90
Table 51. eTQFP80 – STMicroelectronics package mechanical data . . . 93
Table 52. eTQFP100 – STMicroelectronics package mechanical data . . . 96
Table 53. Thermal characteristics for eTQFP80 . . . 97
Table 54. Thermal characteristics for eTQFP100 . . . 98
Table 55. Document revision history . . . 102

List of figures

Figure 1. Block diagram . . . 9
Figure 2. Periphery allocation . . . 10
Figure 3. 80-pin QFP configuration (top view) . . . 13
Figure 4. 100-pin QFP configuration (top view) . . . 14
Figure 5. I/O input DC electrical characteristics definition . . . 24
Figure 6. Weak pull-up electrical characteristics definition . . . 27
Figure 7. I/O output DC electrical characteristics definition . . . 28
Figure 8. Start-up reset requirements . . . 37
Figure 9. Noise filtering on reset signal . . . 38
Figure 10. PLL integration . . . 40
Figure 11. Test circuit . . . 43
Figure 12. Input equivalent circuit (Fast SARn channels) . . . 44
Figure 13. Input equivalent circuit (SARB channels) . . . 45
Figure 14. LFAST and MSC/DSPI LVDS timing definition . . . 58
Figure 15. Power-down exit time . . . 59
Figure 16. Rise/fall time . . . 59
Figure 17. LVDS pad external load diagram . . . 62
Figure 18. Voltage regulator capacitance connection . . . 63
Figure 19. Voltage monitor threshold definition . . . 65
Figure 20. JTAG test clock input timing . . . 71
Figure 21. JTAG test access port timing . . . 71
Figure 22. JTAG JCOMP timing . . . 72
Figure 23. JTAG boundary scan timing . . . 73
Figure 24. Nexus event trigger and test clock timings . . . 74
Figure 25. Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing . . . 75
Figure 26. DSPI CMOS master mode – classic timing, CPHA = 0 . . . 78
Figure 27. DSPI CMOS master mode – classic timing, CPHA = 1 . . . 78
Figure 28. DSPI PCS strobe (PCSS) timing (master mode) . . . 79
Figure 29. DSPI CMOS master mode – modified timing, CPHA = 0 . . . 82
Figure 30. DSPI CMOS master mode – modified timing, CPHA = 1 . . . 82
Figure 31. DSPI PCS strobe (PCSS) timing (master mode) . . . 83
Figure 32. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1 . . . 85
Figure 33. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0 . . . 86
Figure 34. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1 . . . 87
Figure 35. RMII serial management channel timing diagram . . . 88
Figure 36. RMII receive signal timing diagram . . . 89
Figure 37. RMII transmit signal timing diagram . . . 89
Figure 38. eTQFP80 – STMicroelectronics package mechanical drawing . . . 92
Figure 39. eTQFP100 – STMicroelectronics package mechanical drawing . . . 95
Figure 40. Product code structure . . . 101

Figure 1. Block diagram

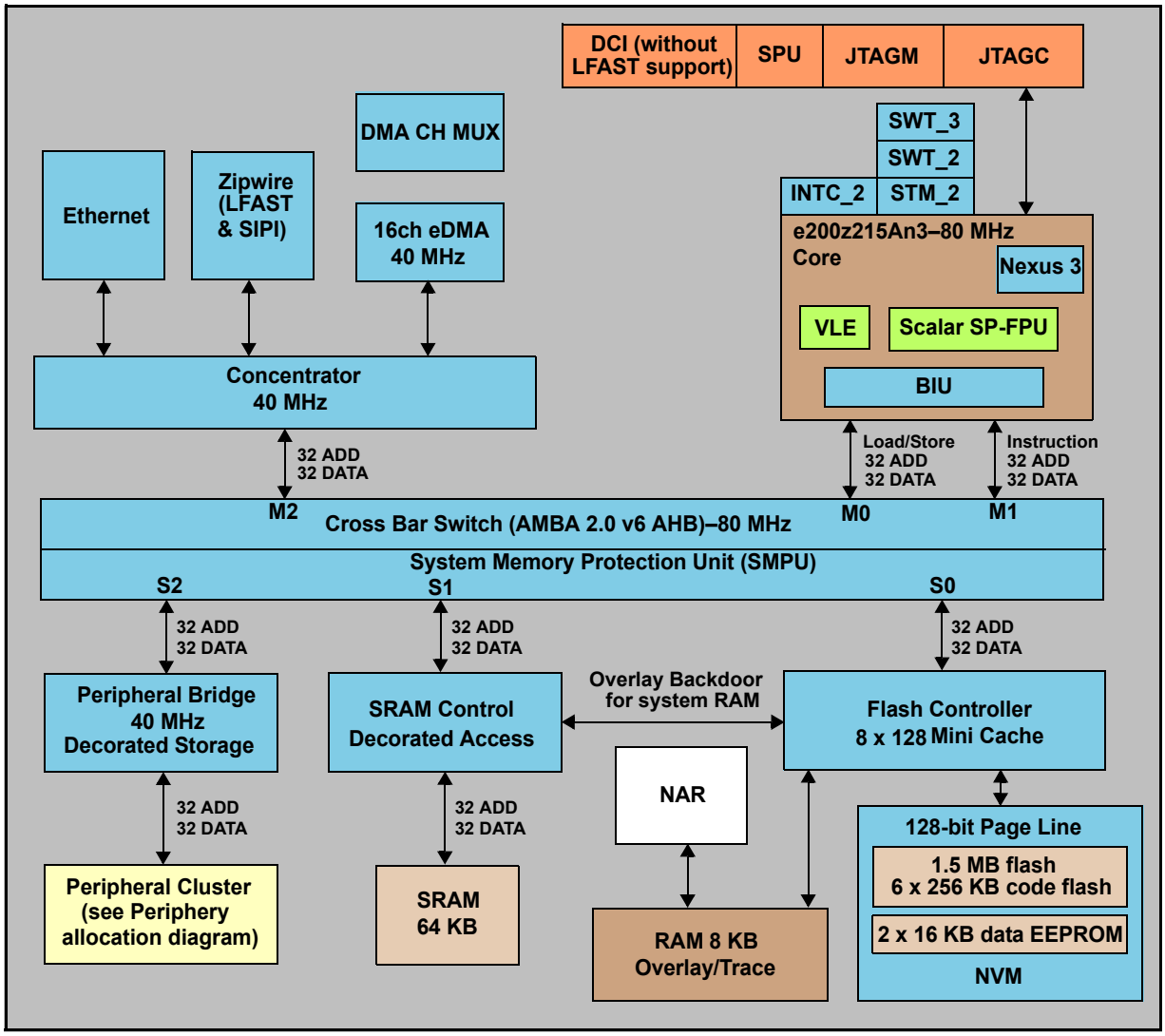
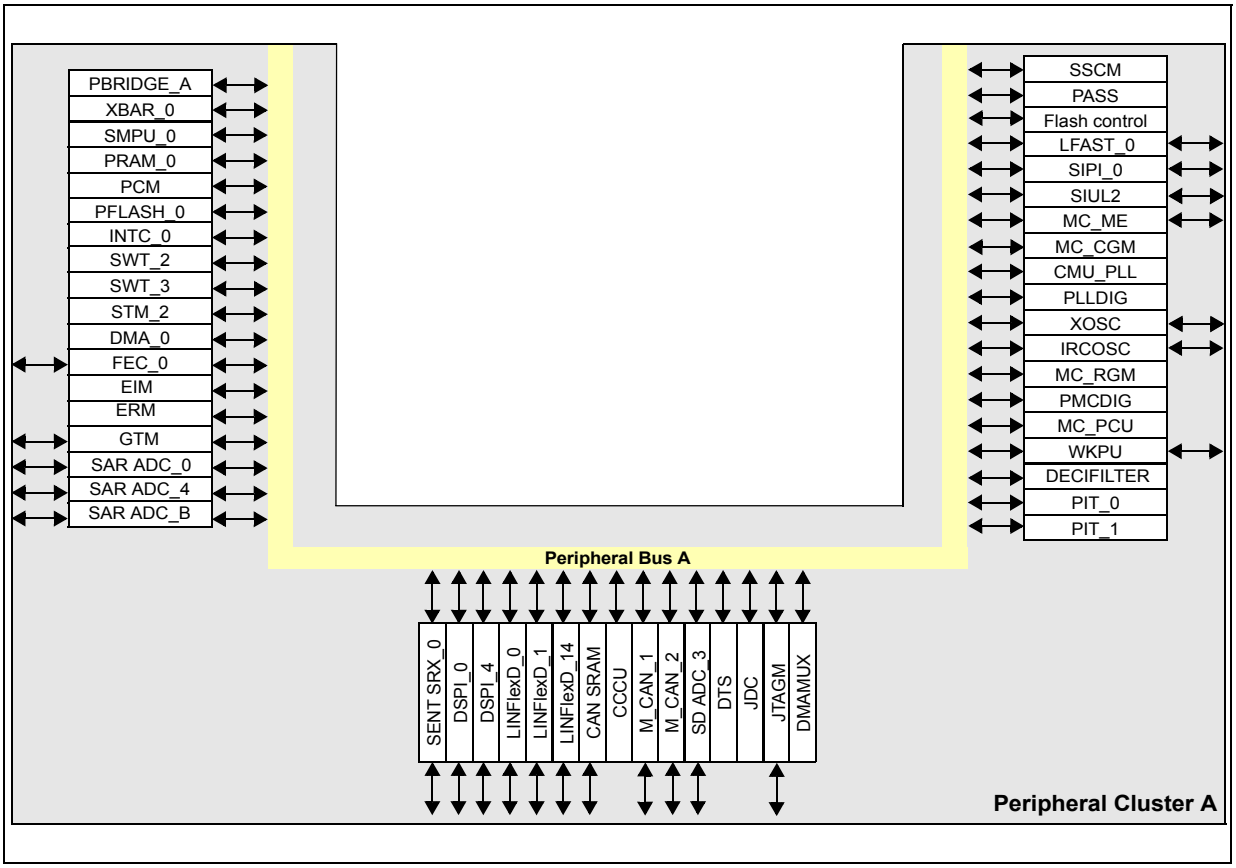


Figure 2. Periphery allocation



paperclip symbol on the left side of the PDF window, and click it. Double-click on the excel file to open it and select the I/O Signal Description Table tab.

Table 12. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{LKG}	CC	P	Digital input leakage	4.5 V < V_{DD_HV} < 5.5 V 0.1*V_{DD_HV} < V_{IN} < 0.9*V_{DD_HV} TJ < 150 °C	—	—	1	µA
		C		4.5 V < V_{DD_HV} < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV}	—	—	2	
I_{LKG_MED}	CC	C	Digital input leakage for MEDIUM pad	4.5 V < V_{DD_HV} < 5.5 V 0.1*V_{DD_HV} < V_{IN} < 0.9*V_{DD_HV}	—	—	500	nA
C_{IN}	CC	D	Digital input capacitance	GPIO input pins	—	—	10	pF
				Ethernet input pins	—	—	8	

1. A good approximation for the variation of the minimum value with supply is given by formula V_{IHAUT} = 0.69 × $V_{DD\_HV\_IO}$.
2. A good approximation for the variation of the maximum value with supply is given by formula V_{ILAUT} = 0.49 × $V_{DD\_HV\_IO}$.
3. Sum of V_{ILAUT} and V_{HYSAUT} is guaranteed to remain above 2.6 V in the 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. Production test done with 2.06 V limit at cold, T_J < 25 °C.
4. A good approximation of the variation of the minimum value with supply is given by formula V_{HYSAUT} = 0.11 × $V_{DD\_HV\_IO}$.
5. In a 1 ms period, assuming stable voltage and a temperature variation of ±30 °C, V_{IL}/V_{IH} shift is within ±50 mV. For SENT requirement refer to NOTE on *page 34*.
6. Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_ETH}$ power segment. The TTL threshold are controlled by the VSIO bit. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V.
7. For LFAST, microsecond bus and LVDS input characteristics, refer to dedicated communication module chapters.
8. Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_ETH}$ power segment.

Table 13 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 13. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	T	Weak pull-up current absolute value(1)	V_{IN} = 0 V V_{DD_POR}(2) < $V_{DD\_HV\_IO}$ < 3.0 V(3)(4)	10.6 * V_{DD_HV} – 10.6	—	—	µA
	CC	T		V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	
	CC	P		V_{IN} = 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	23	—	65	
	CC	T		V_{IN} = 0.49* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	82	
R_{WPU}	CC	D	Weak pull-up resistance	0.49* V_{DD_HVIO} < V_{IN} < 0.69* $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	34	—	62	kΩ

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static currents of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided in the I/O Signal Description table. The sum of all pad usage ratios within a segment should remain below 100%.

Note: In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 50 %. See the I/O Signal Description attachment.

Note: The SPC572Lx I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® workbook file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it and select the I/O Signal Description Table tab.

Table 18. I/O consumption(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_SEG}	SR	D	Sum of all the DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	80	mA
				V_{DD} = 3.3 V ± 10%	—	—	80	
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
				C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
				C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
				C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
				C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
				C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
				C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	

Figure 9. Noise filtering on reset signal

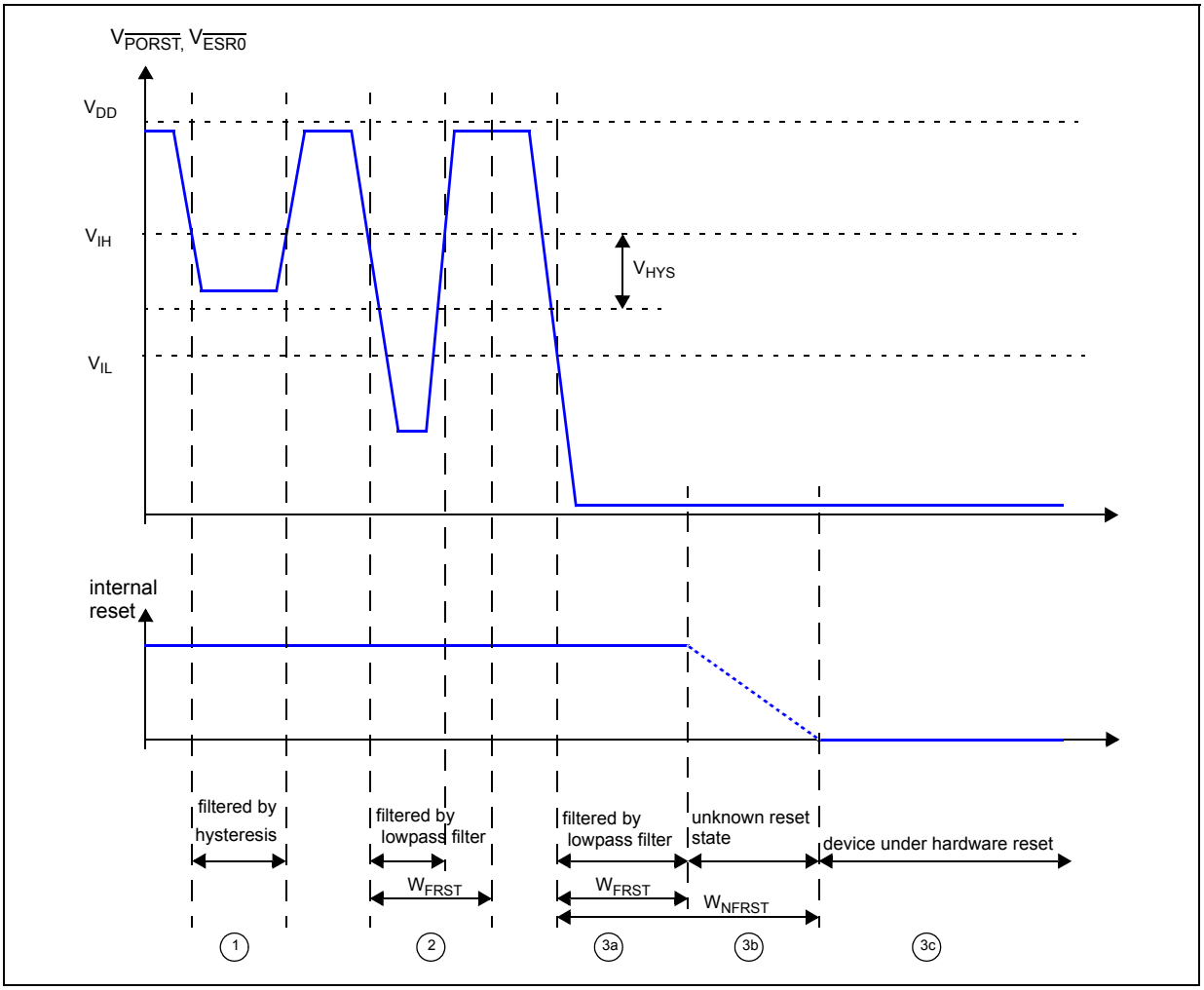


Table 19. Reset electrical characteristics

Symbol			Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level TTL (Schmitt trigger)	—	2.0	—	$V_{DD\_HV\_IO}$ +0.4	V
V_{IL}	SR	P	Input low level TTL (Schmitt trigger)	—	–0.4	—	0.8	V
V_{HYS}	CC	C	Input hysteresis TTL (Schmitt trigger)	—	275	—	—	mV
V_{DD_POR}	CC	C	Minimum supply for strong pull-down activation	—	—	—	1.2	V

Figure 11. Test circuit

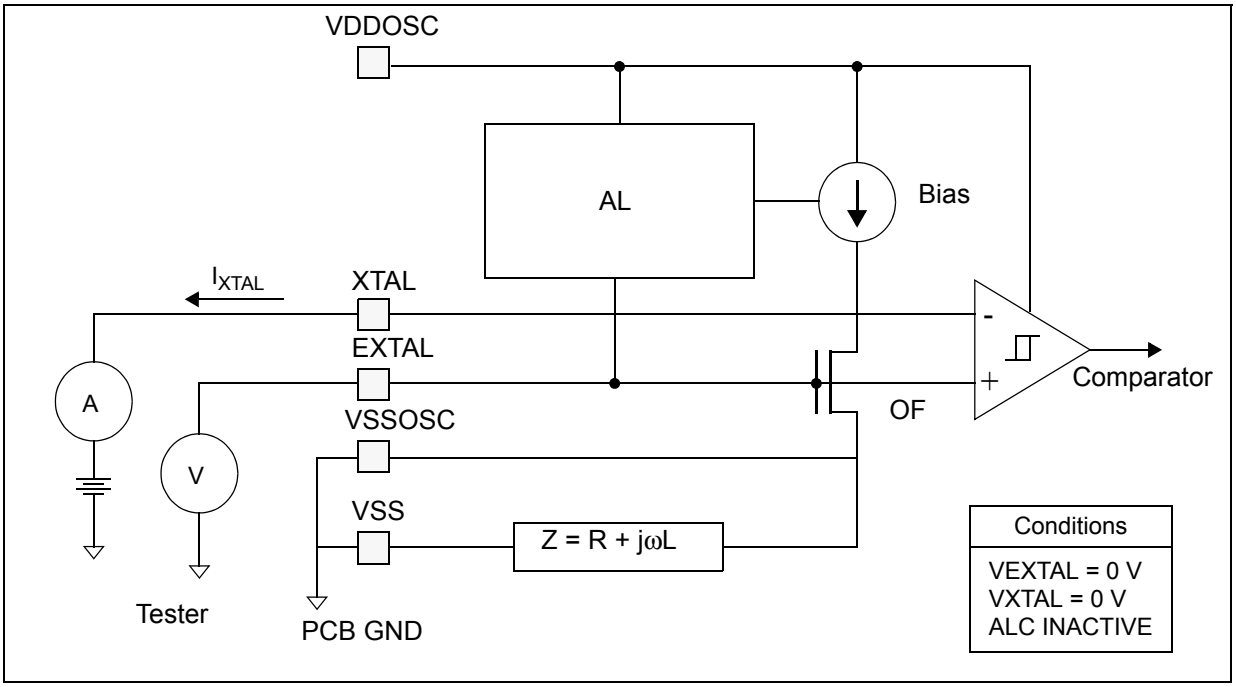


Table 23. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	—	–8	—	+8	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T_J < 150 °C	–1.5	—	+1.5	%
δf_{var_SW}	—	T	IRC frequency accuracy after software trimming accuracy(1)	Trimming temperature	–1	—	+1	%
t_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs
t_{start_T}	CC	D	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs

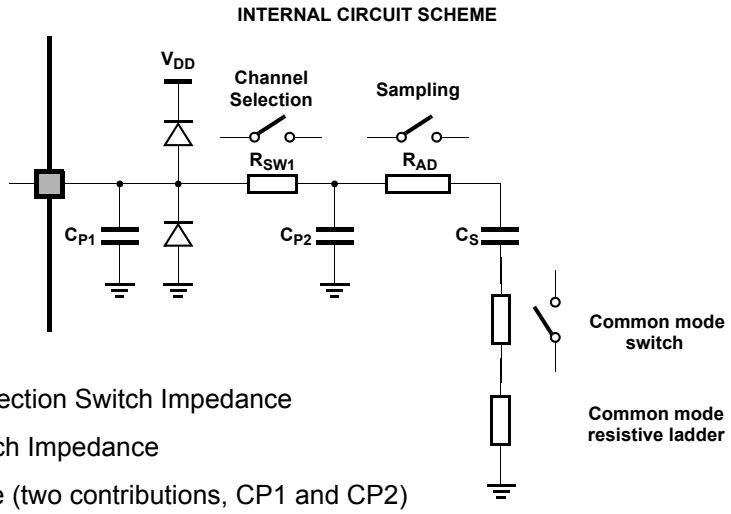
1. The typical user trim step size of δf_{TRIM} = 0.35 %

3.12 ADC specifications

3.12.1 ADC input description

Figure 12 shows the input equivalent circuit for fast SARn channels.

Figure 12. Input equivalent circuit (Fast SARn channels)



RSW1 Channel Selection Switch Impedance

RADSampling Switch Impedance

CP Pin Capacitance (two contributions, CP1 and CP2)

CS Sampling Capacitance

RCMSWCommon mode switch

RCMLCommon mode resistive ladder

This figure can be used as approximation circuitry for external filtering definition.It is also applicable for channel AN16, AN17 and AN24 (Fast channels).

Figure 13 shows the input equivalent circuit for SARB channels.

Table 25. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ALTREF}	SR	P	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	4.5	5.5	V
		C			2.0	4.0	
		C			4.0	5.9	
V_{IN}	SR	D	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$	V
f_{ADCK}	SR	P	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast SAR—fast precharge	135	—	ns
				Fast SAR—full precharge	270	—	
				Slow SAR (SARADC_B)(2)—fast precharge	270	—	
				Slow SAR (SARADC_B)(2)—full precharge	540	—	
ΔV_{PRECH}	SR	D	ADC precharge voltage	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.25	0.25	V
		D		Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(3)	Fast SAR – 12-bit configuration	0.750	—	µs
		D		Fast SAR – 10-bit configuration	0.555	—	
		P		Slow SAR (SARADC_B)(2) – 12-bit configuration	1.500	—	
		D		Slow SAR (SARADC_B)(2) – 10-bit configuration	0.833	—	
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
		D		10-bit configuration (21 clock cycles)	1.458	—	

Table 25. SARn ADC electrical specification[1] (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
Δ_{TUE12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	0	0	LSB (12b)
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–2	2	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–4	4	
		D		$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–6	6	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [0:25 mV]	–2.5	2.5	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [25:50 mV]	–4	4	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [50:75 mV]	–7	7	
		D		$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in$ [75:100 mV]	–12	12	
DNL	CC	P	Differential non-linearity	$V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR} > 4$ V	–1	2	LSB (12b)

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Characteristics corresponding to SARB channels apply only for slow SAR channels i.e., all SARB channels except AN16, AN17, and AN24.
3. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to *Figure 12* and *Figure 13* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
4. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
5. Current parameter values are for a single ADC.
6. Total consumption is given by the sum for all ADCs (associated to the reference pin) of their dynamic consumption and their static consumption.
7. Typical consumption is 2 µA.
8. Typical consumption is 4 µA.

12. The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.
13. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 29. LFAST transmitter electrical characteristics(1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{DATA}	SR	D	Data rate	—	—	—	320	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	CC	P	Differential output voltage swing (terminated)(3)(4)	—	110	171	285	mV
t_{TR}	CC	T	Rise/Fall time (absolute value of the differential output voltage swing)(3),(4)	—	0.26	—	1.5	ns
C_L	SR	D	External lumped differential load capacitance(3)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	9.0	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	CC	T	Transmitter DC current consumption	Enabled	—	—	3.2	mA

1. The LFAST pad electrical characteristics are based on worst case internal capacitance values shown in *Figure 17*.
2. All LFAST LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 17*.
4. Valid for maximum external load C_L.

Table 30. MSC/DSPI LVDS transmitter electrical characteristics (1)(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Data Rate								
f_{DATA}	SR	D	Data rate	—	—	—	80	Mbps
V_{OS}	CC	P	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	CC	P	Differential output voltage swing (terminated)(3)(4)	—	150	214	400	mV
t_{TR}	CC	T	Rise/Fall time (absolute value of the differential output voltage swing)(3),(4)	—	0.8	—	4.0	ns
C_L	SR	D	External lumped differential load capacitance(3)	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	41	pF
				$V_{DD\_HV\_IO}$ = 3.0 V	—	—	39	
I_{LVDS_TX}	CC	T	Transmitter DC current consumption	Enabled	—	—	4.0	mA

1. The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in *Figure 17*.
2. All MSC and DSPI LVDS pad electrical characteristics are valid from –40 °C to 150 °C.
3. Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in *Figure 17*.
4. Valid for maximum external load C_L.

Table 32. Voltage monitor electrical characteristics[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					Min	Typ	Max	
$t_{VDASSERT}$	CC	D	Voltage detector threshold crossing assertion	—	0.1	—	2	µs
$t_{VDRELEASE}$	CC	D	Voltage detector threshold crossing de-assertion	—	5	—	20	µs

1. For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by the multiplying the supply current by 0.5 Ω.
2. The threshold for all PORs and LVDs are defined when the output transits to 1, i.e., when the sense goes above the reference.
3. Across process, temperature and voltage range.

3.15.4 Power up/down sequencing

The following table shows the constraints and relationships for the different power supplies.

Table 33. Device supply relation during power-up/power-down sequence

		Supply 2[1]				
		V_{DD_LV}	$V_{DD\_HV\_IO}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	ALTREF[2]
Supply 1[1]	V_{DD_LV}					
	$V_{DD\_HV\_IO}$					
	$V_{DD\_HV\_ADV}$					
	$V_{DD\_HV\_ADR}$			5 mA		
	ALTREF		10 mA[3]	10 mA[3]		

1. Grey cells: Supply 1 (row) can exceed Supply 2 (column), granted that external circuitry ensures current flowing from supply1 is less than absolute maximum rating current value provided.
2. ALTREF are the alternate references for the ADC that can be used in place of the default reference ($V_{DD\_HV\_ADR\_*}$). It is the SARB.ALTREF.
3. ADC performance is not guaranteed with ALTREFn above $V_{DD\_HV\_IO}$/$V_{DD\_HV\_ADV}$.

During power-up, all functional terminals are maintained into a known state as described in the following table.

Table 34. Functional terminals state during power-up and reset

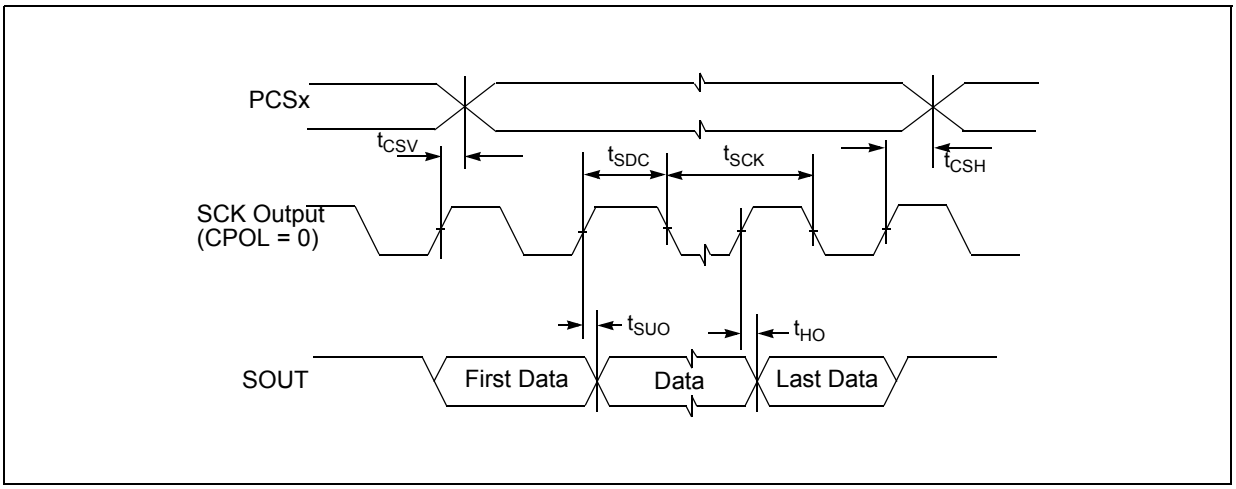
TERMINAL[1]	POWER-UP[2] pad state	RESET pad state	Default pad state[3]	Comments
PORST	Strong pull-down[4]	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0[5]	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad

Table 42. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
					Strong	25 pF	12.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
					Strong	25 pF	12.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
					Very strong	25 pF	25 – ($P^{(10)}$ × $t_{SYS}^{(5)}$)	—	ns
					Strong	50 pF	31 – ($P^{(10)}$ × $t_{SYS}^{(5)}$)	—	
					Medium	50 pF	52 – ($P^{(10)}$ × $t_{SYS}^{(5)}$)	—	
				SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
					Very strong	0 pF	– 1 + ($P^{(9)}$ × $t_{SYS}^{(4)}$)	—	ns
					Strong	0 pF	– 1 + ($P^{(9)}$ × $t_{SYS}^{(4)}$)	—	
					Medium	0 pF	– 1 + ($P^{(9)}$ × $t_{SYS}^{(4)}$)	—	
				SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)									

3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 32. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1



3.17.2.2 Slave Mode timing

Table 45. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(2)	—	—	62	—	ns
2	t_{CSC}	SR	D	$\overline{SS}$ to SCK Delay(2)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to $\overline{SS}$ Delay(2)	—	—	16	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle(2)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(2),(3),(4) ($\overline{SS}$ active to SOUT driven)	Very Strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(2),(3),(4) ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very Strong	25 pF	5	22	ns
					Strong	50 pF	5	28	ns
					Medium	50 pF	5	54	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs(2)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(2)	—	—	10	—	ns

Table 45. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)(1) (continued)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
11	t_{SUO}	CC	D	SOUT Valid Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	55	ns
12	t_{HO}	CC	D	SOUT Hold Time(2),(3),(4) (after SCK edge)	Very Strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.
2. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.
3. All timing values for output signals in this table, are measured to 50% of the output voltage.
4. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Figure 33. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0

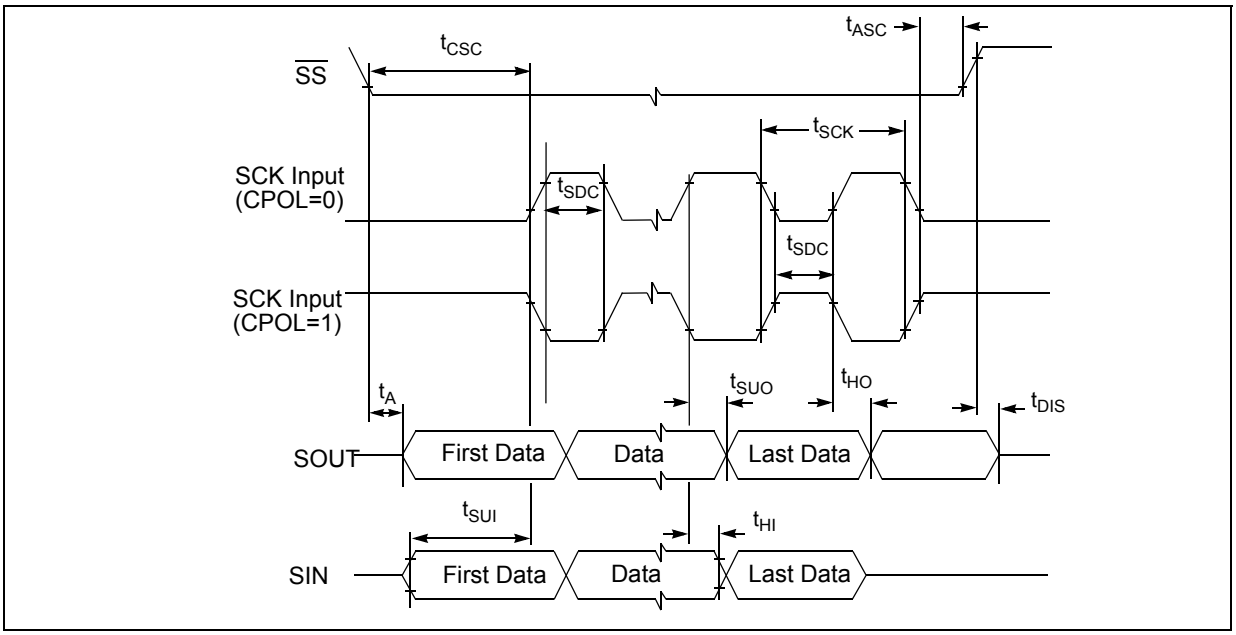


Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Table 21 (External oscillator electrical specifications)*: Updated the minimum and maximum values of f_{XTAL}. Updated V_{IHEXT}, V_{ILEXT}, g_{m}, and I_{XTAL}. Added V_{HYS}. *Table 22 (Selectable load capacitance)*: Updated the table. *Table 23 (Internal RC oscillator electrical specifications)*: Removed I_{AVDD5}, and I_{DVDD12} rows. Updated parameter column of δf_{var_SW}. *Table 24 (ADC pin specification)*: Removed I_{LK_IN} symbol. Added $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$, and $V_{REF\_BG\_LR}$ symbols. Updated conditions column of I_{BG} symbol. Removed the table footnote “Leakage current is a....” Added ΣI_{ADR} Updated I_{LK_INUD}, I_{LK_INUSD}, I_{LK_INREF}, and I_{LK_INOUT}. Replaced maximum value of “6.5” with “8.5” for C_S. *Table 25 (SARn ADC electrical specification)*: Updated conditions, minimum, and maximum columns of V_{ALTREF}. Updated parameter, conditions, and maximum columns of $I_{ADCREFH}$. Replaced the maximum value of “1” with “+8” in $I_{ADCREFH}$ symbol (power down mode). Replaced “I_{ADCVDD}” with “I_{ADV_S}” and updated its conditions and maximum columns. Updated minimum and maximum columns of DNL. *Table 26 (SDn ADC electrical specification)*: In the f_{ADCD_M} symbol replaced “S/D clock 3” with “S/D modulator Input clock”. Added minimum value of “4”. Updated the maximum values of $\lvert\delta_{GAIN}\rvert$ Replaced the unit values of “dB” with “dBFS” in the $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} symbols. Replaced the unit values of “dB” with “dBc” in SFDR symbol. Added CMRR symbol and replaced the minimum value of “20” with “54”. Added R_{Caaf} and $F_{rolloff}$ symbols. Updated the maximum values of I_{ADV_D} and ΣI_{ADR_D}. Removed ΣI_{ADR_D}. Replaced maximum value of “$2*\delta_{GROUP}$” with “δ_{GROUP}” for $t_{LATENCY}$. Replaced maximum value of “15” with “16” for GAIN. Added I_{ADCS/D_REFH}. Updated the minimum, typical and maximum values of Z_{IN}. *Table 27 (Temperature sensor electrical characteristics)*: Added rows: • *temperature monitoring range* • *temperature sensitivity (T_{SENS})* • *temperature accuracy (T_{ACC})*

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Section 3.17.5, GPIO delay timing*: Added this section. Replaced “four” with “three” in the table footnotes in *Table 51 (eTQFP80 – STMicroelectronics package mechanical data)* and *Table 52 (eTQFP100 – STMicroelectronics package mechanical data)*. *Table 51 (eTQFP80 – STMicroelectronics package mechanical data)*: Second note removed from E2 parameter and added to E3 parameter. *Table 53 (Thermal characteristics for eTQFP80)*: Updated the table and its values. *Table 54 (Thermal characteristics for eTQFP100)*: Updated the table and its values. *Table 60 (Order codes (ST))* Updated the table.
15-Jun-2017	4	Following are the changes in this version of the Datasheet: Replaced eLQFP100 with eTQFP100 throughout the document. Removed all requirement tagging from the document. Replaced RPNs: SPC572L64F2B, SPC572L64E3B with SPC572Lx. Replaced SPC572LxB with SPC572Lx. Replaced bullet point “On-chip voltage...” with “Single 5V +/-10%....” on the cover page. *Table 1 (Device summary)*: – Updated the table. *Table 2 (SPC572Lx device feature summary)*: – Updated the notes of “External power supplies” *Section 3.4: Electromagnetic Compatibility (EMC)*: – Updated the section. *Table 9 (Device operating conditions)*: – Updated the values of parameter $V_{DD\_LV.}$ – Updated notes in the table. Removed section: “Temperature profile.” *Table 26 (SDn ADC electrical specification)*: – Updated the values for R_{BIAS} parameter. – Added parameters $Z_{DIFF,}$ Z_{CM}, and $\Delta V_{INTCM.}$ *Table 31 (Voltage regulator electrical characteristics)*: – Added parameter C_{DECFLA} *Table 32 (Voltage monitor electrical characteristics)*: – Added parameter V_{LVD108} *Section 4.3: eTQFP100 case drawing*: – Updated the *Figure 39: eTQFP100 – STMicroelectronics package mechanical drawing*. – Updated the *Table 52 (eTQFP100 – STMicroelectronics package mechanical data)*. *Section 5: Ordering information*: – Removed table: Order codes (ST). Added *Figure 40: Product code structure*.