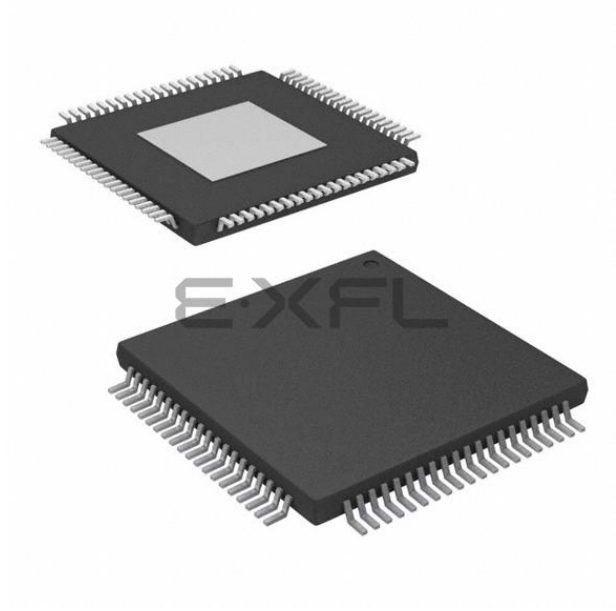

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP Exposed Pad
Supplier Device Package	80-eTQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc572l64f2bc6ar

Table 2. SPC572Lx device feature summary (continued)

Feature	Description
SENT bus	4 channels
Ethernet	Yes
Zipwire (SIPI / LFAST) Interprocessor bus	High speed (4-phase only)
System timers	4 PIT channels 1 AUTOSAR® (STM) 64-bit PIT
GTM timer	16 input channels, 56 output channels
GTM RAM	18.53 KB
Interrupt controller	1024 sources
ADC (SAR)	3
ADC (SD)	1
Temperature sensor	Yes
PLL	Single PLL with no FM
Internal linear voltage regulator	1.2 V
External power supplies	5 V(1) 3.3 V(2)
Low-power modes	Stop mode Slow mode
Packages	eTQFP80 eTQFP100

1. The device can be powered up at 5 V only.
2. Optional: can be used for special I/O segments

1.4 Block diagram

Figure 1 and *Figure 2* show the top-level block diagrams.

Figure 2. Periphery allocation

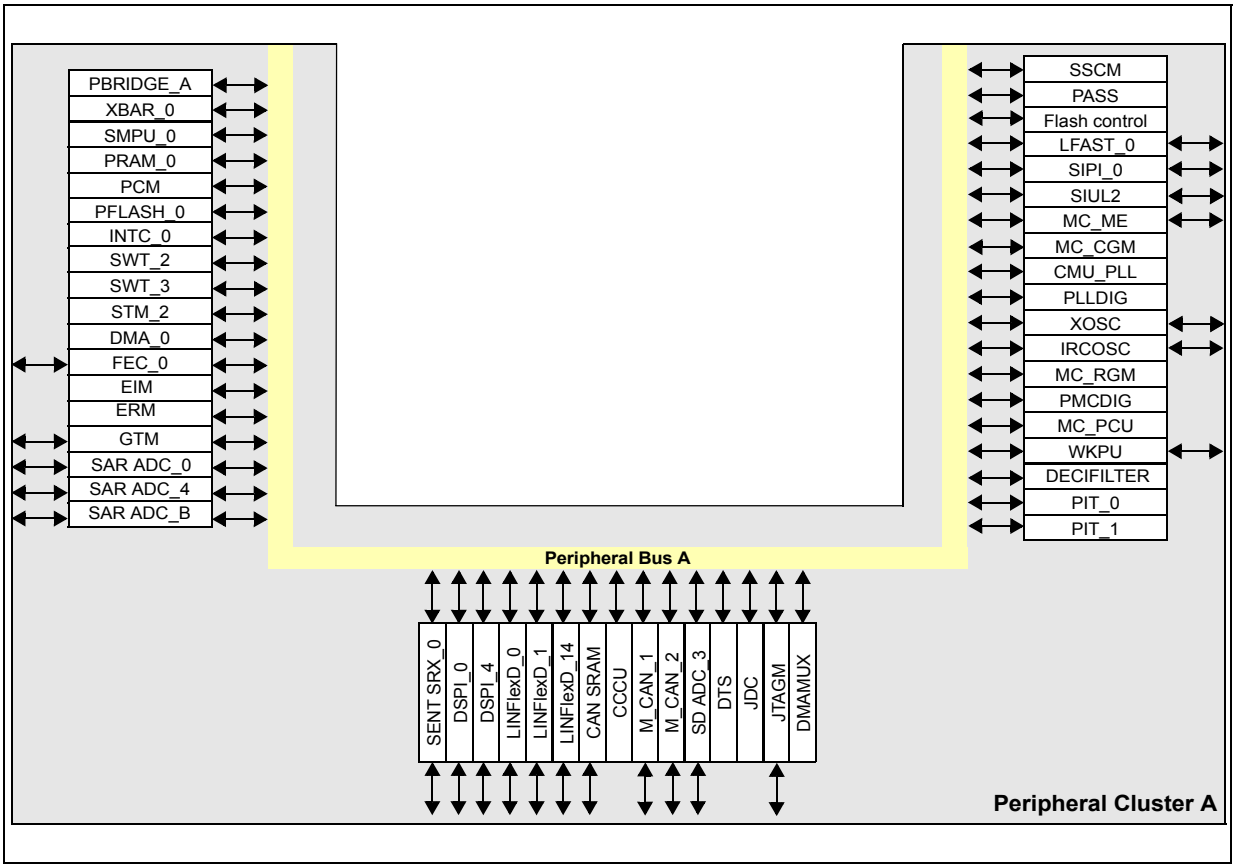


Table 9. Device operating conditions[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)[13],[14],[15]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	SR	D	Maximum current per power segment[16]	—	–80	—	80	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the core and platform for the device. See the Clocking chapter in the *SPC572Lx Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *SPC572Lx Microcontroller Reference Manual* for further information.
5. The $V_{DD\_HV\_PMC}$ supply providing power to the internal regulator is shorted with the $V_{DD\_HV\_IO}$ supply within package.
6. LVD400 can be disabled by SW (always enabled after power-up).
7. Maximum voltage is not permitted for entire product life. See *Absolute maximum rating*.
8. When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.
9. Reduced output/input capabilities below 4.2 V. See performance operating values in I/O pad electrical characteristics. Not all functionality are guaranteed below 4.2 V. Please check specific supply constraints by module in *Table 9 (Device operating conditions)*.
10. $V_{DD\_HV\_IO\_JTAG}$ supply is shorted with $V_{DD\_HV\_OSC}$ supply within package.
11. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_FLA}$ value of 3.0 V.
12. This voltage can be measured on the pin but is not supplied by an external regulator. The Power Management Controller generates PORs based on this voltage.
13. Full device lifetime without performance degradation
14. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the *Absolute maximum ratings* table for maximum input current for reliability requirements.
15. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current is injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
16. Sum of all controller pins (including both digital and analog) must not exceed 150 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

3.7 DC electrical specifications

The following table describes the DC electrical specifications.

Table 14. WEAK configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_W}	CC	P	PMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	520	800	1040	Ω
R_{OL_W}	CC	P	NMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	520	800	1040	Ω
f_{MAX_W}	CC	T	Output frequency weak configuration	C_L = 25 pF[3]	—	—	2	MHz
				C_L = 50 pF[3]	—	—	1	
		D		C_L = 200 pF[3]	—	—	0.25	
t_{TR_W}	CC	T	Transition time output pin weak configuration[4]	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	ns
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	80	—	240	
		D		C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	320	—	820	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	50	—	150	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	100	—	300	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	350	—	1050	
$\lvert t_{SKEW\_W} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	120	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	150	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	240	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	300	

1. All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula:

   0 pF < C_L < 50 pFt_{TR_W}(ns) = 22 ns + C_L(pF) × 4.4 ns/pF

   50 pF < C_L < 200 pFt_{TR_W}(ns) = 50 ns + C_L(pF) × 3.85 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0.

Table 15 shows the MEDIUM configuration output buffer electrical characteristics.

4. Transition time maximum value is approximated by the following formula:
   0 pF < C_L < 50 pFt_{TR_M}(ns) = 5.6 ns + C_L(pF) × 1.11 ns/pF
   50 pF < C_L < 200 pFt_{TR_M}(ns) = 13 ns + C_L(pF) × 0.96 ns/pF
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0

Table 16 shows the STRONG configuration output buffer electrical characteristics.

Table 16. STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions(1)	Value(2)			Unit
					Min	Typ	Max	
R_{OH_S}	CC	P	PMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	30	50	65	Ω
R_{OL_S}	CC	P	NMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	30	50	65	Ω
f_{MAX_S}	CC	T	Output frequency STRONG configuration	C_L = 25 pF(3)	—	—	40	MHz
				C_L = 50 pF(3)	—	—	20	
				C_L = 200 pF(3)	—	—	5	
t_{TR_S}	CC	T	Transition time output pin STRONG configuration(4)	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.5	—	10	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.5	—	16	
				C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	13	—	50	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V(5)	4	—	15	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V(5)	6	—	27	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V(5)	20	—	83	
I_{DCMAX_S}	CC	D	Maximum DC current	—	—	—	10	mA
$\|t_{SKEW\_S}\|$	CC	T	Difference between rise and fall time	—	—	—	25	%

Table 16. STRONG configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	12	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	18	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	20	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	36	

1. All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.5 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0 V to 3.6 V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula: t_{TR_S}(ns) = 4.5 ns + C_L(pF) x 0.23 ns/pF.
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0

Table 17 shows the VERY STRONG configuration output buffer electrical characteristics.

Table 17. VERY STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_V}	CC	P	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OH} = 8 mA	20	40	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA[3]	30	50	75	
R_{OL_V}	CC	P	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OL} = 8 mA	20	40	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA[3]	30	50	75	
f_{MAX_V}	CC	T	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[4]	—	—	50	MHz
				VSIO[VSIO_xx] = 1, C_L = 15 pF[3],[4]	—	—	50	

Table 18. I/O consumption(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	50	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	55	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	22	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	25	
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	60	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	64	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	26	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	29	

1. I/O current consumption specifications for the 4.5 V <= $V_{DD\_HV\_IO}$ <= 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V <= $V_{DD\_HV\_IO}$ <= 3.6 V.
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

3.10 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

Note: $\overline{PORST}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

Table 19. Reset electrical characteristics (continued)

Symbol			Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{OL_R}	CC	C	Strong pull-down current(1)	Device under power-on reset $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{OL} = 0.35 * V_{DD\_HV\_IO}$	0.2	—	—	mA
				—	—	—	—	—
				Device under power-on reset $3.0\ V < V_{DD\_HV\_IO} < 5.5\ V$, $V_{OL} > 1.0\ V$	12	—	—	mA
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$\overline{ESR0}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	23	—	—	µA
				$\overline{ESR0}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	—	—	82	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$\overline{PORST}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	—	—	130	µA
				$\overline{PORST}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	40	—	—	
W_{FRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	P	$\overline{PORST}$ and $\overline{ESR0}$ input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	SR	P	ESR1 input filtered pulse	—	—	—	15	ns
W_{NFNMI}	SR	P	ESR1 input not filtered pulse	—	400	—	—	ns

1. I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0.

$\overline{PORST}$ must be connected to an external power-on supply circuitry. Minimum requested circuitry is external pull-up to ensure device can exit reset.

Note: No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

3.11 Oscillator and PLL

Single phase-locked loop (PLL) module with the reference PLL (PLL0) generating the system and auxiliary clocks from the main oscillator driver.

1. PLL0IN clock retrieved directly from either Internal RC Oscillator (IRCOSC) or External Oscillator (XOSC) clock. Input characteristics are granted when using XOSC.
2. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range of 8 MHz-20 MHz.
3. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.25 V ± 5% with frequency below PLL bandwidth (40 kHz) is filtered.

Table 21. External oscillator electrical specifications

Symbol		C	Parameter	Conditions		Value		Unit
						Min	Max	
f_{XTAL}	CC	D	Crystal frequency range(1)	—		4	8	MHz
				—		> 8	20	
				—		> 20	40	
t_{cst}	CC	T	Crystal start-up time(2)(3)	—		—	5	ms
t_{rec}	CC	T	Crystal recovery time(4)	—		—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		V_{REF} + 0.6	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage(5)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	CC	T	Total on-chip stray capacitance on EXTAL pin	—		—	2.5 + value from *Table 22*	pF
C_{S_XTAL}	CC	T	Total on-chip stray capacitance on XTAL pin	—		—	2.5 + value from *Table 22*	pF
g_m	CC	D	Oscillator Transconductance	T_J = -40 °C to 150 °C 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	$f_{XTAL} \leq$ 8 MHz	2.6	11.0	mA/V
		D			$f_{XTAL} \leq$ 20 MHz	7.9	26.0	
		D			$f_{XTAL} \leq$ 40 MHz	10.4	34.0	
I_{XTAL}	CC	D	XTAL current(6)	T_J = 150 °C		—	14	mA
V_{HYS}	CC	D	Comparator Hysteresis	T_J = 150 °C		0.1	1.0	V

1. The range is selectable by DCF record.
2. This value is determined by the crystal manufacturer and board design.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
5. Applies to an external clock input and not to crystal mode.
6. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. Test circuit is shown in *Figure 11*.

Table 24. ADC pin specification(1) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LK_INREF}	CC	C	Input leakage current, two ADC channels input with weak pull-up and weak pull-down and alternate reference	T_J< 40 °C, no current injection on adjacent pin	—	160	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	400	
I_{LK_INOUT}	CC	C	Input leakage current, two ADC channels input, GPIO output buffer with weak pull-up and weak pull-down	T_J < 40 °C, no current injection on adjacent pin	—	140	nA
		C		T_J < 150 °C, no current injection on adjacent pin	—	380	
I_{INJ}	CC	T	Injection current on analog input preserving functionality	Applies to any analog pins	–3	3	mA
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance(2)		1	2.2	µF
C_{P1}	CC	D	Pad capacitance	—	0	10	pF
C_{P2}	CC	D	Internal routing capacitance	SARn channels	0	0.5	pF
		D		SARB channels(3)	0	1	
C_{P3}	CC	D	Internal routing capacitance	Only for SARB channels	0	1	pF
C_S	CC	D	SAR ADC sampling capacitance	—	6	8.5	pF
R_{SWn}	CC	D	Analog switches resistance	SARn channels	0	1.1	kΩ
		D		SARB channels(4)	0	1.7	
R_{AD}	CC	D	ADC input analog switches resistance	—	0	0.6	kΩ
R_{CMSW}	CC	D	Common mode switch resistance	—	0	2.6	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder	—	0	3.5	kΩ
R_{SAFEPD}(4)	CC	D	Discharge resistance for AN7 channels (strong pull-down for safety)	—	0	300	W
ΣI_{ADR}	CC	C+P	Sum of ADC and S/D reference consumption	ADC enabled	—	40	µA

1. All specifications in this table valid for the full input voltage range for the analog inputs.
2. For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.
3. Characteristics corresponding to fast SARn channels also apply to SARB fast channels (AN16, AN17 and AN24).
4. Safety pull-down is available for port pin PE[14]. It enables discharge of up to 100 nF from 5 V every 300 ms.

3.12.2 SAR ADC electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 25. SARn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{ALTREF}	SR	P	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$ $V_{ALTREF} < V_{DD\_HV\_ADV}$	4.5	5.5	V
		C			2.0	4.0	
		C			4.0	5.9	
V_{IN}	SR	D	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$	V
f_{ADCK}	SR	P	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	Fast SAR—fast precharge	135	—	ns
				Fast SAR—full precharge	270	—	
				Slow SAR (SARADC_B)(2)—fast precharge	270	—	
				Slow SAR (SARADC_B)(2)—full precharge	540	—	
ΔV_{PRECH}	SR	D	ADC precharge voltage	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.25	0.25	V
		D		Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time(3)	Fast SAR – 12-bit configuration	0.750	—	µs
		D		Fast SAR – 10-bit configuration	0.555	—	
		P		Slow SAR (SARADC_B)(2) – 12-bit configuration	1.500	—	
		D		Slow SAR (SARADC_B)(2) – 10-bit configuration	0.833	—	
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
		D		10-bit configuration (21 clock cycles)	1.458	—	

9. Extra bias current is present only when BIAS is selected. Apply only once for all ADCs.
10. Extended bench validation performed on 3 samples for each process corner.
11. This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to ± 6 LSB.

3.12.3 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 26. SDn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	P	ADC input signal	—	0	—	$V_{DD\_HV\_ADR\_D}$	V
V_{IN_PK2PK}(2)	SR	D	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$(3) $- V_{INM}$(4)	Single ended $V_{INM} = V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$/GAIN			V
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 1	±0.5*$V_{DD\_HV\_ADR}$			
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 2,4,8,16	±$V_{DD\_HV\_ADR}$/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	±$V_{DD\_HV\_ADR}$/GAIN			
f_{ADCD_M}	SR	P	S/D modulator Input Clock	—	4	14.4	16	MHz
f_{IN}	SR	D	Input signal frequency	SNR = 80 dB f_{ADCD_S} = 150 kHz	0.01	—	50(5)	kHz
		D		SNR = 74 dB f_{ADCD_S} = 333 kHz	0.01	—	111(5)	
f_{ADCD_S}	SR	D	Output conversion rate	—	—	—	333	ksps
—	CC	D	Oversampling ratio	Internal modulator	24	—	256	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution(6)	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\lvert\delta_{GAIN}\rvert$	CC	C	Absolute value of the ADC gain error(7),(8)	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		D		After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
				After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
				After calibration, $\Delta V_{DD\_HV\_ADR} < 5\%$ $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	CC	P	Input Referred Offset Error(7),(8),(9)	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	20	mV
		D		After calibration, $\Delta V_{DD\_HV\_ADR} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
				After calibration, $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 100$ °C			7.5	
				After calibration, $\Delta V_{DD\_HV\_ADV} < 10\%$ $\Delta T_J < 150$ °C	0.5		10	

Table 26. SDn ADC electrical specification(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$t_{SETTLING}$	CC	D	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP} + 3*f_{ADCD\_S}$	—
				HPF = OFF	—	—	$2*\delta_{GROUP} + 2*f_{ADCD\_S}$	—
$t_{ODRECOVERY}$	CC	D	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP} + f_{ADCD\_S}$	—
				HPF = OFF	—	—	$2*\delta_{GROUP}$	—
C_{S_D}	CC	D	S/D ADC sampling capacitance after sampling switch(14)	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		D		GAIN = 16	—	—	600	fF
IBIAS	CC	D	Bias consumption	At least 1 ADCD enabled	—	—	3.5	mA
I_{ADV_D}	CC	P	$V_{DD\_HV\_ADV}$ power supply current (single S/D ADC)	S/D ADC Dynamic consumption	—	—	3.5	mA
I_{ADCS/D_REFH}	CC	T	S/D ADC Reference High Current	Dynamic consumption (Conversion)	—	—	3.5	µA
		T		Static consumption (Power down)	—	—	+8	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be 'clipped'.
3. V_{INP} is the input voltage applied to the positive terminal of the SDADC.
4. V_{INM} is the input voltage applied to the negative terminal of the SDADC.
5. Maximum input of 166.67 kHz supported with reduced accuracy. See SNR specifications.
6. When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. This gives an effective resolution of 15 bits.
7. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.
8. Calibration of gain is possible when gain = 1.
   Offset Calibration should be done with respect to $0.5*V_{DD\_HV\_ADR}$ for *differential mode* and *single ended mode with negative input=0.5*$V_{DD\_HV\_ADR}$*.
   Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0".
   Both offset and Gain Calibration is guaranteed for ±5% variation of $V_{DD\_HV\_ADR}$, ±10% variation of $V_{DD\_HV\_ADV}$, and ± 50 °C temperature variation.
9. Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.
10. This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to a value of 6 dB less.
11. Impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to frequency:
    $Z_{DIFF}(f_{ADCD\_M})$ = 16 MHz/f_{ADCD_M}* Z_{DIFF}
    $Z_{CM}(f_{ADCD\_M})$ = 16 MHz/f_{ADCD_M}* Z_{CM}
12. SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of $f_{ADCD\_M} - f_{ADCD\_S}$ to $f_{ADCD\_M} + f_{ADCD\_S}$, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.
13. The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.

Table 32. Voltage monitor electrical characteristics[1] (continued)

Symbol		C	Parameter	Conditions	Value[2]			Unit
					Min	Typ	Max	
$t_{VDASSERT}$	CC	D	Voltage detector threshold crossing assertion	—	0.1	—	2	µs
$t_{VDRELEASE}$	CC	D	Voltage detector threshold crossing de-assertion	—	5	—	20	µs

1. For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by the multiplying the supply current by 0.5 Ω.
2. The threshold for all PORs and LVDs are defined when the output transits to 1, i.e., when the sense goes above the reference.
3. Across process, temperature and voltage range.

3.15.4 Power up/down sequencing

The following table shows the constraints and relationships for the different power supplies.

Table 33. Device supply relation during power-up/power-down sequence

		Supply 2[1]				
		V_{DD_LV}	$V_{DD\_HV\_IO}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	ALTREF[2]
Supply 1[1]	V_{DD_LV}					
	$V_{DD\_HV\_IO}$					
	$V_{DD\_HV\_ADV}$					
	$V_{DD\_HV\_ADR}$			5 mA		
	ALTREF		10 mA[3]	10 mA[3]		

1. Grey cells: Supply 1 (row) can exceed Supply 2 (column), granted that external circuitry ensures current flowing from supply1 is less than absolute maximum rating current value provided.
2. ALTREF are the alternate references for the ADC that can be used in place of the default reference ($V_{DD\_HV\_ADR\_*}$). It is the SARB.ALTREF.
3. ADC performance is not guaranteed with ALTREFn above $V_{DD\_HV\_IO}$/$V_{DD\_HV\_ADV}$.

During power-up, all functional terminals are maintained into a known state as described in the following table.

Table 34. Functional terminals state during power-up and reset

TERMINAL[1]	POWER-UP[2] pad state	RESET pad state	Default pad state[3]	Comments
PORST	Strong pull-down[4]	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0[5]	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad

Table 34. Functional terminals state during power-up and reset (continued)

TERMINAL(1)	POWER-UP(2) pad state	RESET pad state	Default pad state(3)	Comments
ESR1	High impedance	Weak pull-down	Weak pull-down	—
TEST_MODE	Weak pull-down	Weak pull-down(6)	Weak pull-down(6)	—
GPIO	Weak pull-up(4)	Weak pull-up	Weak pull-up	—
ANALOG	High impedance	High impedance	High impedance	—
ERROR	High impedance	High impedance	High impedance	—
TRST	High impedance	Weak pull-down	Weak pull-down	—
TCK	High impedance	Weak pull-down	Weak pull-down	—
TMS	High impedance	Weak pull-up	Weak pull-up	—
TDI	High impedance	Weak pull-up	Weak pull-up	—
TDO	High impedance	High impedance	High impedance	—

1. Refer to pinout information for terminal type.
2. POWER-UP state is guaranteed from $V_{DD\_HV\_IO}$ > 1.1 V and maintained until supply crosses the power-on reset threshold: V_{PORUP_LV} for LV supply, V_{PORUP_HV} for high voltage supply.
3. Before software configuration.
4. Pull-down and pull-up strength are provided as part of *Section 3.8.2, I/O output DC characteristics*.
5. As opposed to ESR0, ESR1 is provided via normal GPIO and implements weak pull-up during power-up.
6. TESTMODE pull-down is implemented to prevent device to enter TESTMODE. It is recommended to connect TESTMODE pin to $V_{SS\_HV\_IO}$ on the board.

3.16 Flash memory electrical characteristics

The flash array access time for reads is affected by the number of wait-states added to the minimum time, which is one cycle.

Wait states are set in the RWSC field of the Platform Flash Configuration Register 1 (PFCR1) to a value corresponding to the operating frequency of the flash memory controller and the actual read access time of the flash memory controller. Higher operating frequencies require non-zero settings for this field for proper flash operation.

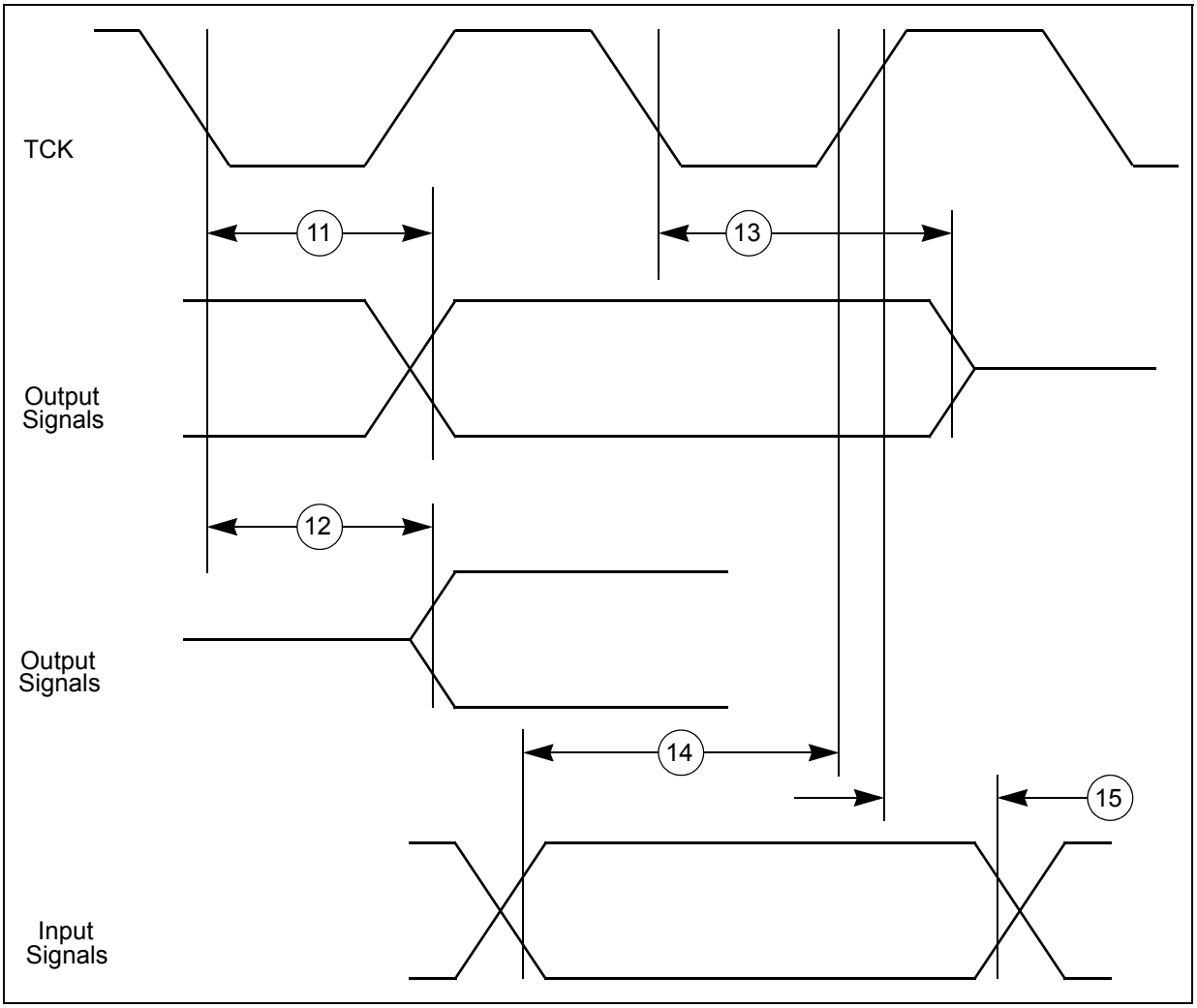
Shown below are the maximum operating frequencies (f_{sys}) for legal RWSC settings based on specified access times at 150 °C:

Table 35. RWSC settings

Flash operating frequency range (MHz)	RWSC
00 MHz < f_{sys} < 20 MHz	0
20 MHz < f_{sys} < 40 MHz	1
40 MHz < f_{sys} < 60 MHz	2
60 MHz < f_{sys} < 80 MHz	3

Table 36 shows the estimated Program/Erase characteristics.

Figure 23. JTAG boundary scan timing



3.17.1.2 Nexus interface timing

Table 39. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Value		Unit
					Min	Max	
7	t_{EVTIPW}	CC	D	$\overline{EVTI}$ pulse width	4	—	t_{CYC}[2]
8	t_{EVTOPW}	CC	D	$\overline{EVTO}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2[3],[4]	—	t_{CYC}[2]
9	t_{TCYC}	CC	D	Absolute minimum TCK cycle time[5] (TDO/TDOC sampled on posedge of TCK)	40[6]	—	ns
				Absolute minimum TCK cycle time[7] (TDO/TDOC sampled on negedge of TCK)	20[6]	—	
11[8]	t_{NTDIS}	CC	D	TDI/TDIC data setup time	5	—	ns

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Table 28 (LVDS pad startup and receiver electrical characteristics)*: Replaced “C” with “T” in the characteristics column of I_{LVDS_BIAS} and I_{LVDS_RX}. *Table 29 (LFAST transmitter electrical characteristics)*, and *Table 30 (MSC/DSPI LVDS transmitter electrical characteristics)*: Replaced “C” with “T” in the characteristics column of I_{LVDS_TX}. *Table 39 (Nexus debug port timing)*: Replaced “P” with “D” in the characteristics column of t_{EVTIPW} and tEVTOPW. *Figure 18 (Voltage regulator capacitance connection)*: Updated the figure. *Table 31 (Voltage regulator electrical characteristics)*: Replaced $R_{DECREGn}$ with R_{REG}. Updated the conditions column of C_{DECBV} and C_{DECHV}. Changed the classification of $I_{MREGINT}$ from “P” to “D”. Added “- at 27 ^{o}C , no load” to note 6. Added “with full load” to note 7. *Table 36 (Flash memory program and erase specifications (pending silicon characterization))*: For tESUS, replaced lifetime max value of “20” WITH “30”. For tpsus, replaced lifetime max value of “10” WITH “15”. *Table 40 (DSPI channel frequency support)*: Removed “Full duplex” from LVDS (Master mode). *Table 41 (DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1)*: Updated the minimum values of t_{CSC}, t_{PCSC}, and t_{PASC} and maximum values of t_{SUO}. *Table 42 (DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1)*: Updated the minimum values of t_{CSC}, t_{PCSC}, and t_{PASC} and maximum values of t_{SUO}. Removed section “DSPI LVDS Master Mode — Modified Timing.” *Table 44 (DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock)*: Updated the minimum values of t_{CSV} and maximum values of t_{SUO}. *Table 45 (DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1))*: Updated the minimum and maximum values of t_{DIS}. Replaced the maximum value of “50” with “55” in $t_{SUO\ (medium)}$. *Table 48 (RMII transmit signal timing)*: Replaced the maximum value of “14” with “16” for R6.