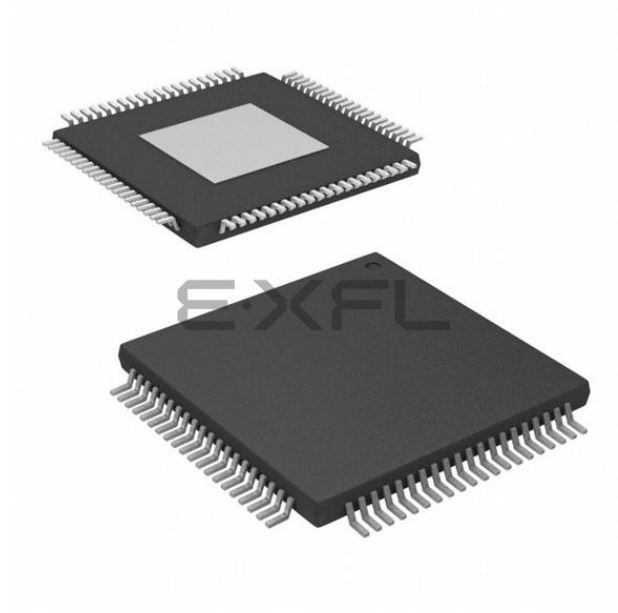

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Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP Exposed Pad
Supplier Device Package	80-eTQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc572l64f2bc6ay

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Figure 1. Block diagram

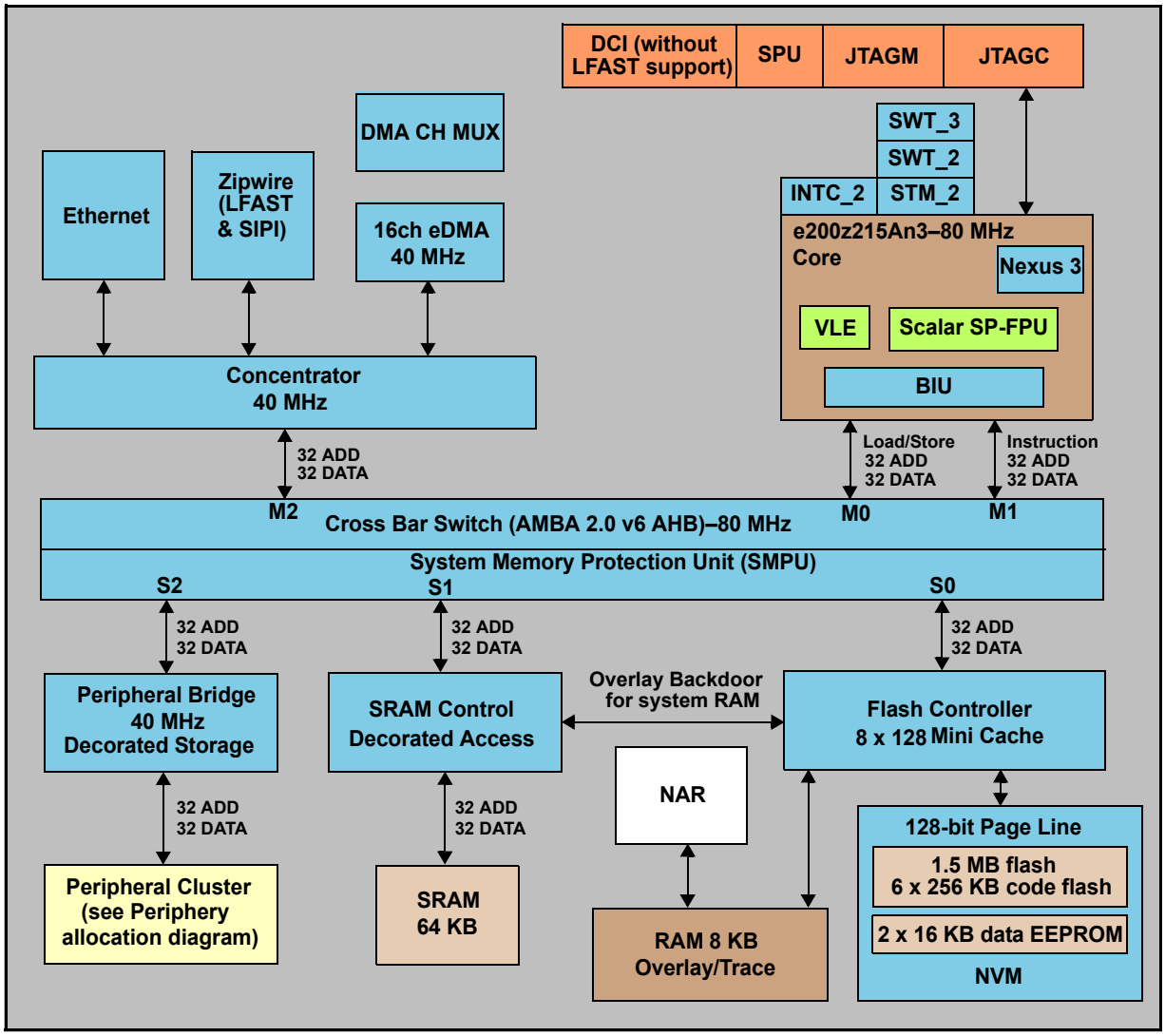
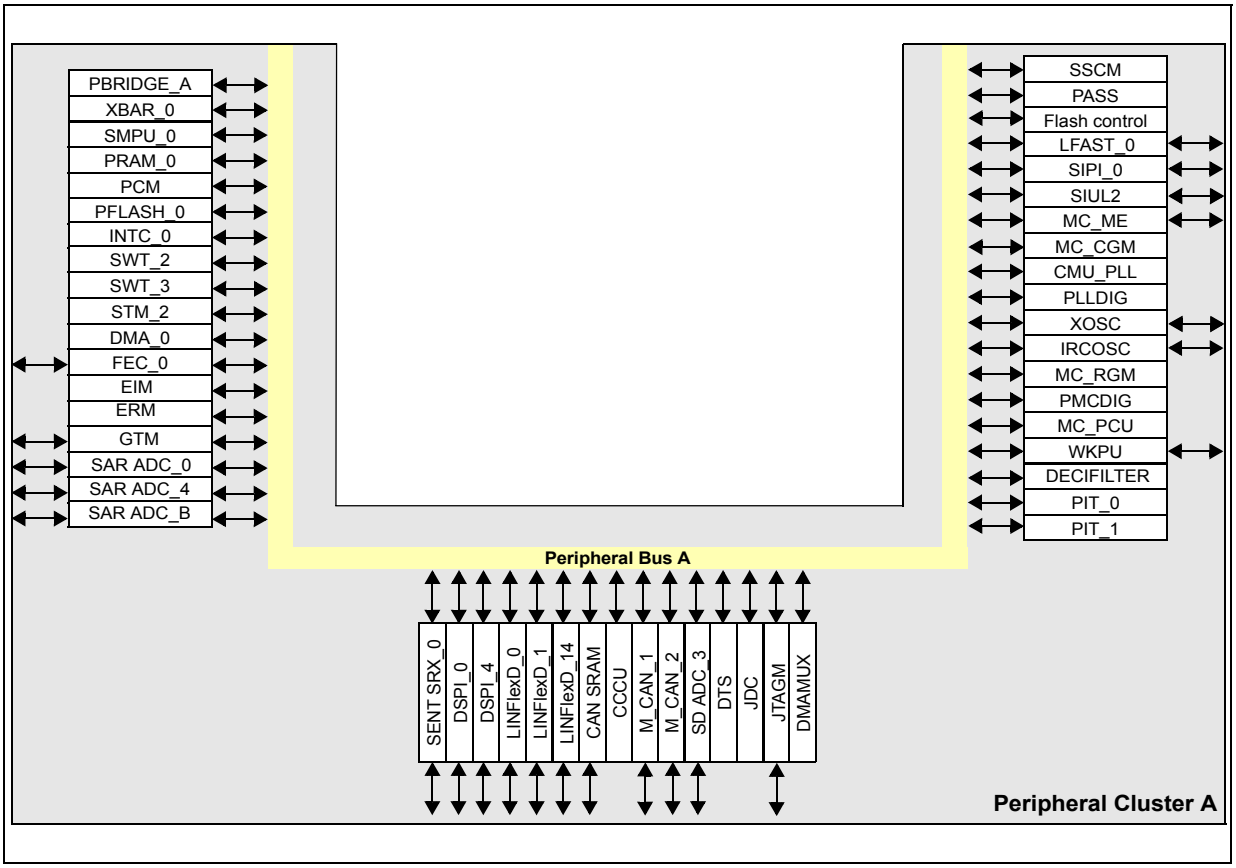


Figure 2. Periphery allocation



- 1 Clock Calibration on CAN Unit (CCCU)
- Fast Ethernet Controller (FEC)
- Fast Asynchronous Serial Transmission (LFAST)
- Nexus Development Interface (NDI) per IEEE-ISTO 5001-2003 standard, with partial support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1 and IEEE 1149.7)
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic
- Self-test capability

2 Package pinouts and signal descriptions

2.1 Package pinouts

The QFP package pinouts are shown in *Figure 3* and *Figure 4*.

Figure 3. 80-pin QFP configuration (top view)

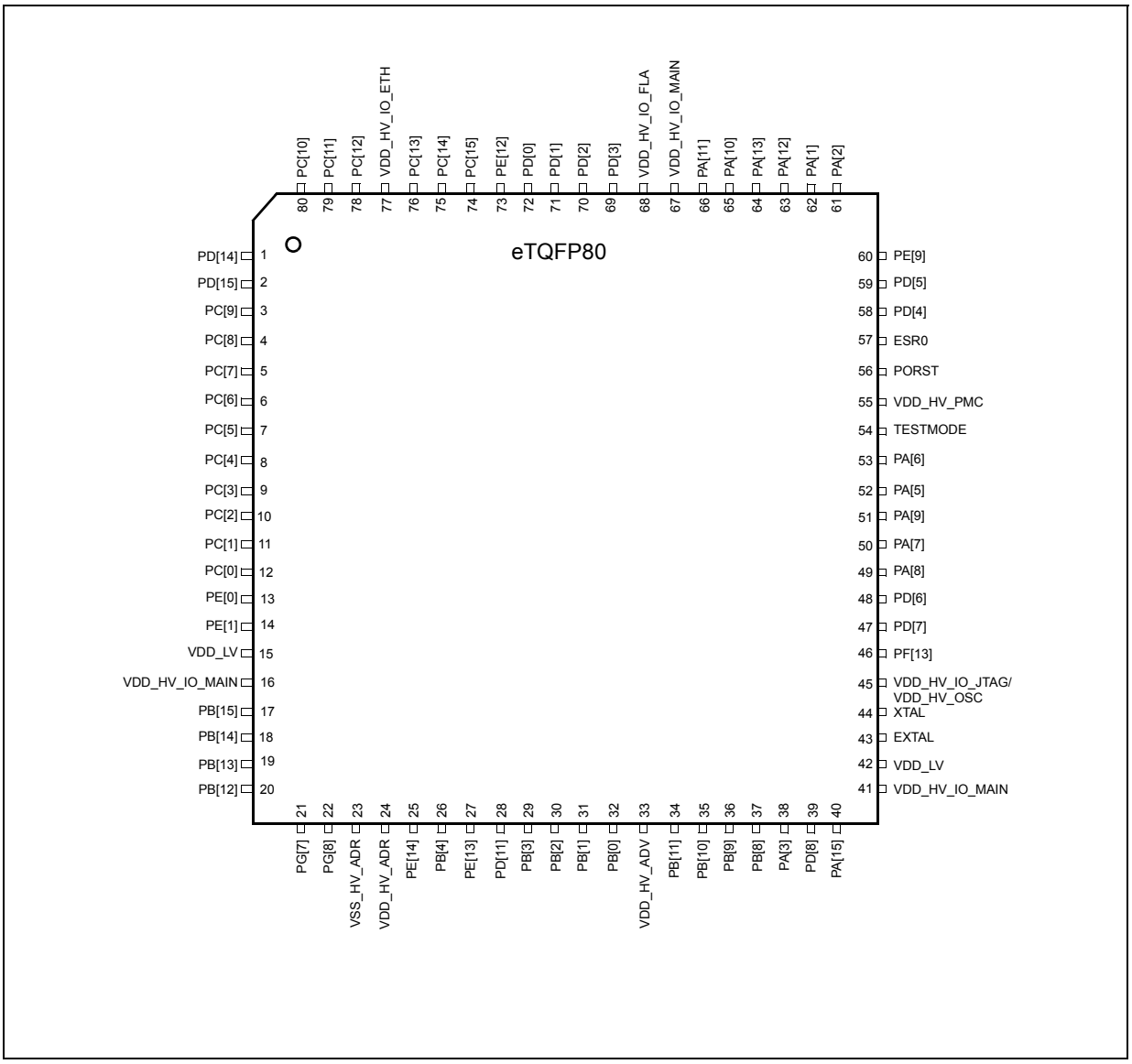


Table 9. Device operating conditions[1] (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)[13],[14],[15]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	SR	D	Maximum current per power segment[16]	—	–80	—	80	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the core and platform for the device. See the Clocking chapter in the *SPC572Lx Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. Core voltage as measured on device pin to guarantee published silicon performance.
4. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *SPC572Lx Microcontroller Reference Manual* for further information.
5. The $V_{DD\_HV\_PMC}$ supply providing power to the internal regulator is shorted with the $V_{DD\_HV\_IO}$ supply within package.
6. LVD400 can be disabled by SW (always enabled after power-up).
7. Maximum voltage is not permitted for entire product life. See *Absolute maximum rating*.
8. When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.
9. Reduced output/input capabilities below 4.2 V. See performance operating values in I/O pad electrical characteristics. Not all functionality are guaranteed below 4.2 V. Please check specific supply constraints by module in *Table 9 (Device operating conditions)*.
10. $V_{DD\_HV\_IO\_JTAG}$ supply is shorted with $V_{DD\_HV\_OSC}$ supply within package.
11. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_FLA}$ value of 3.0 V.
12. This voltage can be measured on the pin but is not supplied by an external regulator. The Power Management Controller generates PORs based on this voltage.
13. Full device lifetime without performance degradation
14. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the *Absolute maximum ratings* table for maximum input current for reliability requirements.
15. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current is injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
16. Sum of all controller pins (including both digital and analog) must not exceed 150 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

3.7 DC electrical specifications

The following table describes the DC electrical specifications.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_M}	CC	P	PMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 2 mA	120	200	260	Ω
R_{OL_M}	CC	P	NMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 2 mA	120	200	260	Ω
f_{MAX_M}	CC	T	Output frequency MEDIUM configuration	C_L = 25 pF[3]	—	—	12	MHz
				C_L = 50 pF[3]	—	—	6	
		D		C_L = 200 pF[3]	—	—	1.5	
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration[4]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	10	—	30	ns
				C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	20	—	60	
		D		C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	60	—	200	
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	12	—	42	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	24	—	86	
				C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	70	—	300	
$\lvert t_{SKEW\_M} \rvert$	CC	T	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	—	—	—	4	mA
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	35	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	42	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	70	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	85	

1. All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.5 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance (C_{TOT} = C_L + C_{IN}).

Table 16. STRONG configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$T_{PHL/PLH}$	CC	D	Propagation delay	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	12	ns
				C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	18	
				C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V	—	—	20	
				C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	—	—	36	

1. All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.5 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0 V to 3.6 V are valid for VSIO[VSIO_xx] = 0
2. All values need to be confirmed during device validation.
3. C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in *Table 12*) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).
4. Transition time maximum value is approximated by the following formula: t_{TR_S}(ns) = 4.5 ns + C_L(pF) x 0.23 ns/pF.
5. Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_ETH}$ segment when VSIO[VSIO_IF] = 0

Table 17 shows the VERY STRONG configuration output buffer electrical characteristics.

Table 17. VERY STRONG configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
R_{OH_V}	CC	P	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OH} = 8 mA	20	40	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA[3]	30	50	75	
R_{OL_V}	CC	P	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1, I_{OL} = 8 mA	20	40	60	Ω
		C		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA[3]	30	50	75	
f_{MAX_V}	CC	T	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[4]	—	—	50	MHz
				VSIO[VSIO_xx] = 1, C_L = 15 pF[3],[4]	—	—	50	

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static currents of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided in the I/O Signal Description table. The sum of all pad usage ratios within a segment should remain below 100%.

Note: In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 50 %. See the I/O Signal Description attachment.

Note: The SPC572Lx I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® workbook file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it and select the I/O Signal Description Table tab.

Table 18. I/O consumption(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{RMS_SEG}	SR	D	Sum of all the DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	80	mA
				V_{DD} = 3.3 V ± 10%	—	—	80	
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
				C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
				C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
				C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
				C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
				C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
				C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	

Table 25. SARn ADC electrical specification[1] (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
$I_{ADCREFH}$[4], [5]	CC	T	ADC high reference current[6]	Dynamic consumption $t_{conv} \geq 5$ µs (average across all codes)	—	3.5[7]	µA
				Dynamic consumption $t_{conv} \geq 2.5$ µs (average across all codes)	—	7[8]	
				Static consumption (Power Down mode)	—	+8	
		T		Bias Current[9]	—	+2	
$I_{ADCREFL}$[5]	CC	D	ADC low reference current	Run mode $t_{conv} \geq 5$ µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	15	µA
				Run mode t_{conv} = 2.5 µs $V_{DD\_HV\_ADR}$ <= 5.5 V	—	30	
				Power Down mode $V_{DD\_HV\_ADR}$ <= 5.5 V	—	1	
I_{ADV_S}	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode[5] $t_{conv} \geq 5$ µs	—	4.0	mA
TUE_{12}	CC	T[10]	Total unadjusted error in 12-bit configuration[11]	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$, V_{ALTREF}> 4 V	–4	4	LSB (12b)
		P		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, $V_{DD\_HV\_ADR}$, V_{ALTREF}> 4 V	–6	6	
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > V_{ALTREF}> 2 V	–6	6	
		T		T_J < 150 °C, 4 V > $V_{DD\_HV\_ADV}$ > 3.5 V	–12	12	
TUE_{10}	CC	T	Total unadjusted error in 10-bit configuration	T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V $V_{DD\_HV\_ADR}$, V_{ALTREF} > 4 V	–1.5	1.5	LSB (10b)
		T		T_J < 150 °C, $V_{DD\_HV\_ADV}$ > 4 V, 4 V > $V_{DD\_HV\_ADR}$, V_{ALTREF}> 2 V	–2.0	2.0	

9. Extra bias current is present only when BIAS is selected. Apply only once for all ADCs.
10. Extended bench validation performed on 3 samples for each process corner.
11. This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to ± 6 LSB.

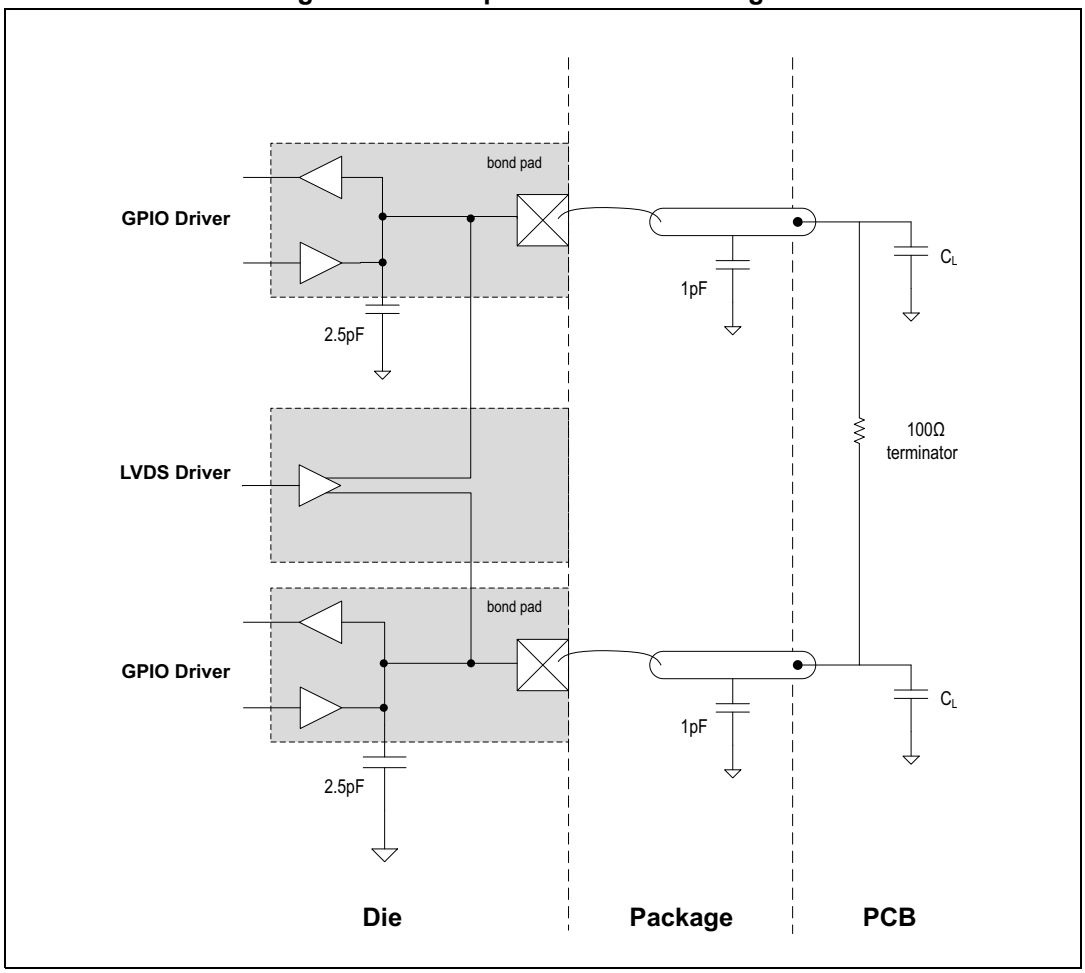
3.12.3 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 26. SDn ADC electrical specification(1)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IN}	SR	P	ADC input signal	—	0	—	$V_{DD\_HV\_ADR\_D}$	V
V_{IN_PK2PK}(2)	SR	D	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$(3) $- V_{INM}$(4)	Single ended $V_{INM} = V_{SS\_HV\_ADR}$	$V_{DD\_HV\_ADR}$/GAIN			V
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 1	±0.5*$V_{DD\_HV\_ADR}$			
		D		Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR}$ GAIN = 2,4,8,16	±$V_{DD\_HV\_ADR}$/GAIN			
		D		Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	±$V_{DD\_HV\_ADR}$/GAIN			
f_{ADCD_M}	SR	P	S/D modulator Input Clock	—	4	14.4	16	MHz
f_{IN}	SR	D	Input signal frequency	SNR = 80 dB f_{ADCD_S} = 150 kHz	0.01	—	50(5)	kHz
		D		SNR = 74 dB f_{ADCD_S} = 333 kHz	0.01	—	111(5)	
f_{ADCD_S}	SR	D	Output conversion rate	—	—	—	333	ksps
—	CC	D	Oversampling ratio	Internal modulator	24	—	256	—
				External modulator	—	—	256	—
RESOLUTION	CC	D	S/D register resolution(6)	2's complement notation	16			bit
GAIN	SR	D	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—

Figure 17. LVDS pad external load diagram



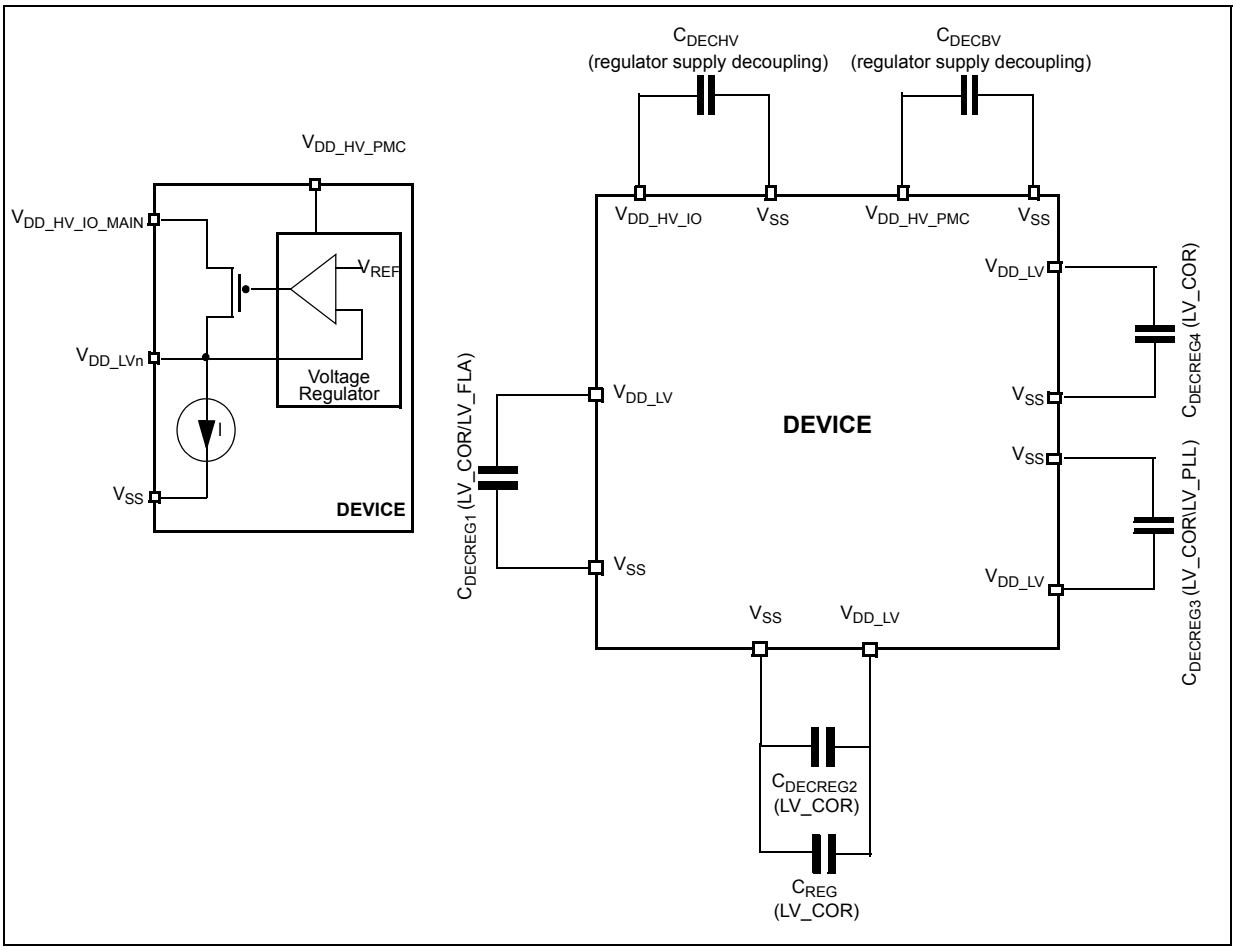
3.15 Power management: PMC, POR/LVD, sequencing

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the $V_{DD\_HV\_PMC}$ supply, with voltage monitors ensuring safe state operation.

3.15.1 Power management integration

Refer to the integration scheme provided below to ensure correct functionality of the device.

Figure 18. Voltage regulator capacitance connection



The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

A decoupling capacitor must be placed between each V_{DD_LV} supply pin and V_{SS} ground plane to ensure stable voltage. The capacitor should be placed as near as possible to the V_{DD_LV} supply pin.

3.15.2 Main voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD\_BV\_PMC}$. The regulator itself is supplied by $V_{DD\_HV\_PMC}$.

Note: Both HV supplies, $V_{DD\_HV\_PMC}$ and $V_{DD\_BV\_PMC}$, are shorted with $V_{DD\_HV\_IO}$ supply at package level.

The following supplies are involved:

- HV—High voltage external power supply for voltage regulator module. It is shorted with $V_{DD\_HV\_IO}$.
- BV—High voltage external power supply for internal ballast module. It is shorted with $V_{DD\_HV\_IO}$.
- LV—Low voltage internal power supply for core, PLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is split into three further domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for PLL through double bonding.
  - LV_FLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for PLL. It is shorted to LV_COR through double bonding.

Table 31. Voltage regulator electrical characteristics

Symbol		Parameter	Conditions[1]	Value[2]			Unit
				Min	Typ	Max	
C_{REG}	SR	Internal voltage regulator stability external capacitance	—	1.1	2.2[3]	2.97	µF
R_{REG}	SR	Stability capacitor equivalent serial resistance	Total resistance including board track	1	—	50	mΩ
$C_{DECREGn}$	SR	Internal voltage regulator decoupling external capacitance	—	50	100	135	nF
$R_{DECREGn}$	SR	Stability capacitor equivalent serial resistance	—	1	—	50	mΩ
C_{DECBV}	SR	Decoupling capacitance[4] ballast	$V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	—	4[3]	—	µF
C_{DECHV}	SR	Decoupling capacitance regulator supply	$V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	10	100	—	nF
C_{DECFLA}	SR	Decoupling capacitance for flash supply	$V_{DD\_HV\_FLA}/V_{SS}$ pair	65	100	—	nF
	D						
V_{MREG}	CC	Main regulator output voltage	Before trimming	1.19	1.26	1.33[5]	V
	CC		After trimming	1.16	1.28	1.32[6]	
IDD_{MREG}	SR	Main regulator current provided to V_{DD_LV} domain	—	—	—	125	mA
ΔIDD_{MREG}	SR	Main regulator current variation	20 µs observation window	–60	—	60	mA
$I_{MREGINT}$[7]	D	Main regulator current consumption	—	—	1.5	3.0	mA

1. V_{DD} = 5.0 V ± 10%, T_A = –40 / 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
4. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
5. At power-up condition before trimming at 27 °C, no load.

Figure 20. JTAG test clock input timing

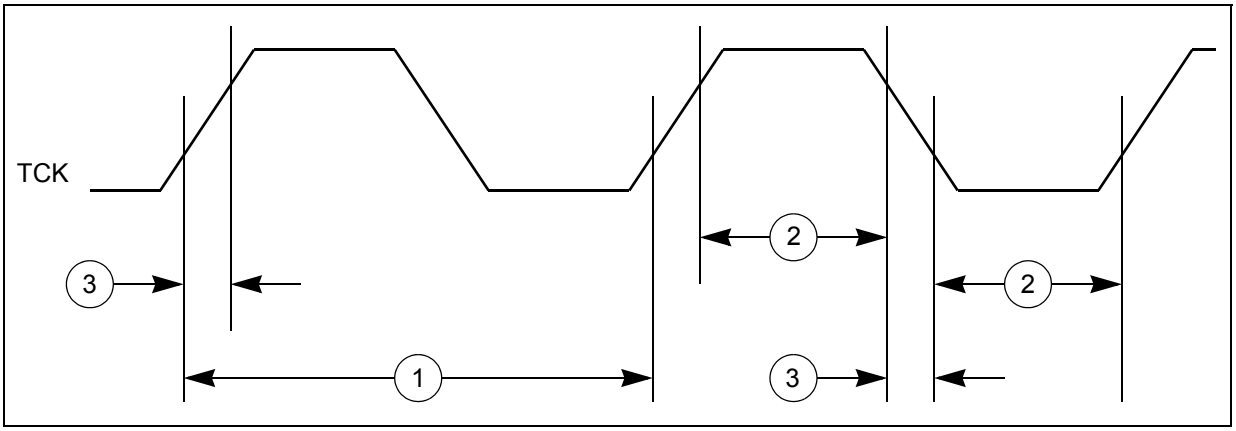


Figure 21. JTAG test access port timing

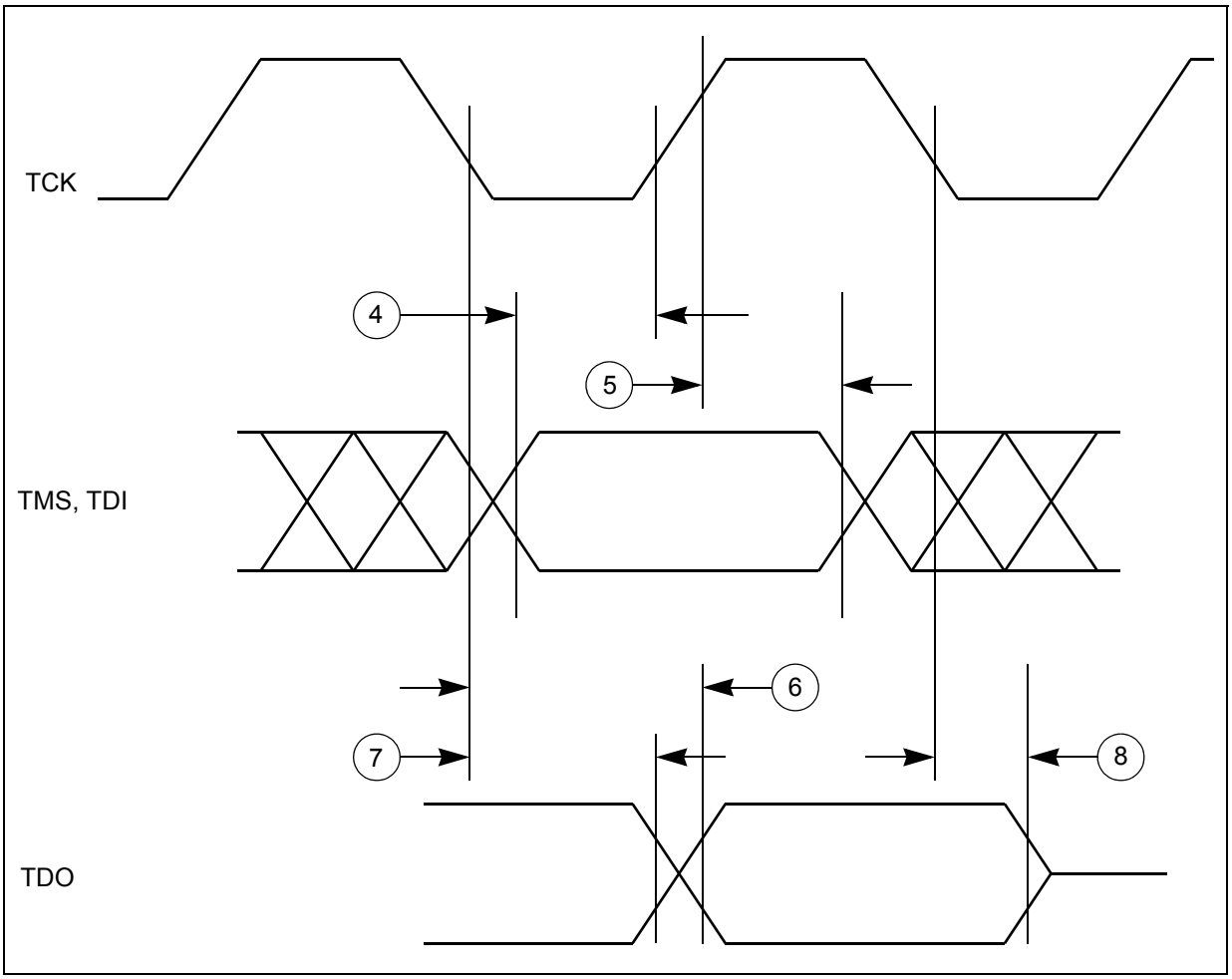


Table 44. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock(1)(2)

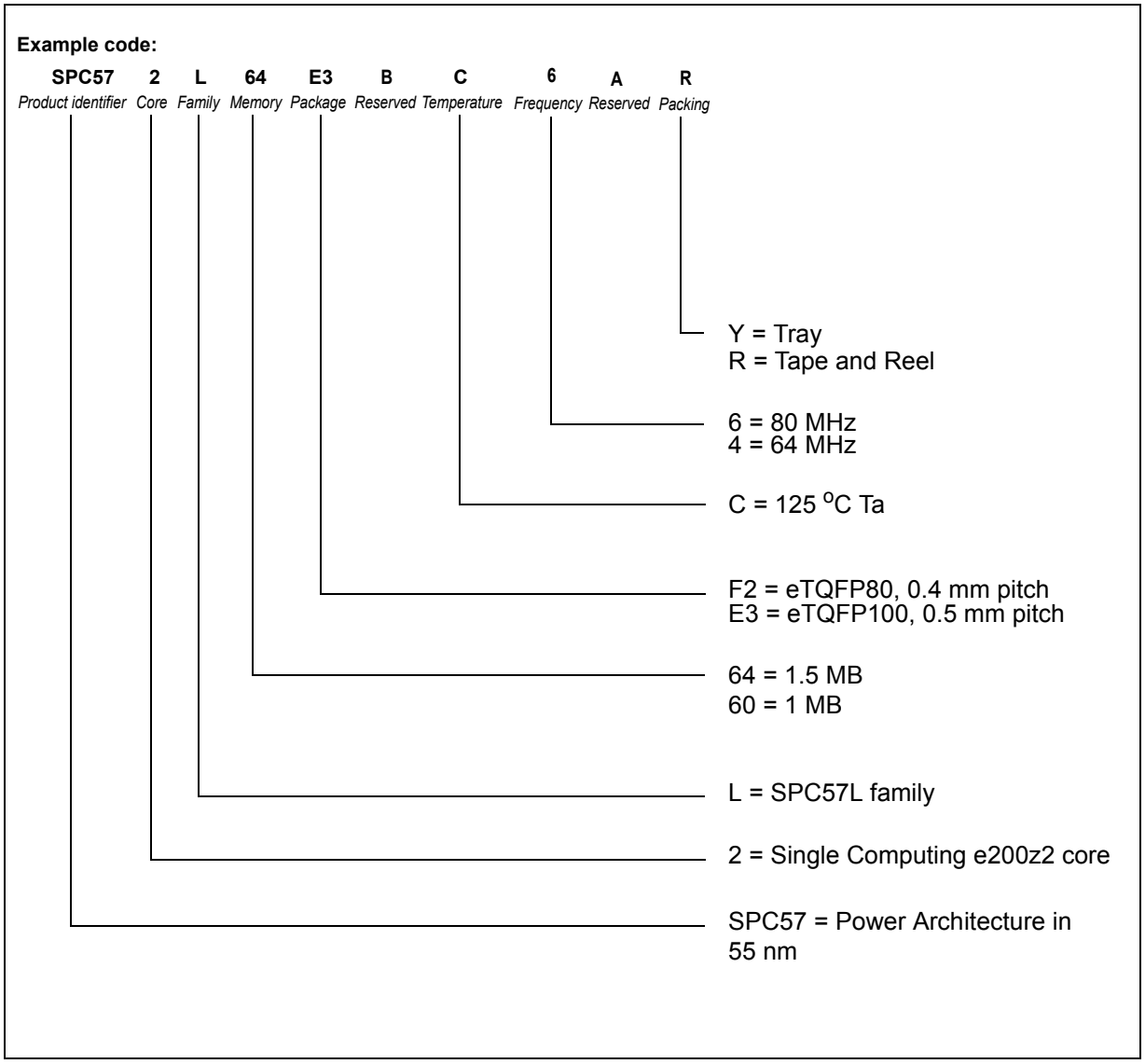
#	Symbol		C	Characteristic	Condition		Value(3)		Unit
					Pad drive(4)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSV}	CC	D	PCS valid after SCK(5)	SCK and PCS drive strength				
					Very strong	25 pF	16	—	ns
					Strong	50 pF	16	—	ns
					Medium	50 pF	26	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	38	—	ns
3	t_{CSH}	CC	D	PCS hold after SCK(5)	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(6)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2t_{SCK} - 2$	$^1/_2t_{SCK} + 2$	ns
					Medium	0 pF	$^1/_2t_{SCK} - 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 1(7)	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	9.0	ns
					Medium	50 pF	—	25.0	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 1(7)	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	ns
					Medium	50 pF	–15.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. To be determined at seating datum plane C.
7. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
8. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
9. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad is variable depending on leadframe pad design (T1, T2, T3). End user should verify D2 and E2 dimensions according to specific device application.
10. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
11. “N” is the number of terminal positions for the specified body size.
12. Tolerance

5 Ordering information

Figure 40. Product code structure



1. Order on 1 MB part numbers can be entered upon ST's acceptance conditioned by volumes. Please contact your ST sales office to ask for the availability of a particular commercial product.
2. Features (e.g. flash, RAM or peripherals) not included in the commercial product cannot be used. ST cannot be called to take any liability for features used outside the commercial product.

6 Revision history

Table 55 summarizes revisions to this document.

Table 55. Document revision history

Date	Revision	Changes
18-Jul- 2012	1	Initial release.
03-Apr-2013	2	Formatting and editorial changes throughout document. *Table 2: SPC572Lx device feature summary*: Changed title (was *SPC5726SPC572L64 device feature summary*) *Figure 2 (Periphery allocation)*: Removed BAR module from diagram. *Section 1.5, Features overview*: Added detail to PIT descriptions (2 bullets). Added *Saturation Instructions Extension...* feature item. *Figure 4 (100-pin QFP configuration (top view))*: Changed pin 65 to “ESR1” *Table 3 (Power supply and reference pins)*: For row V_{DD_LV}: added pin 68 for 100 pin and 80 pin packages. *Section 2.2.1, Power supply and reference voltage pins*: Added 2 sentences starting from “The Supply Pins Table contains...” Table 5 (Port pins description): From PC[10] to PC[15] - changed *VDD_HV_IO_FLEX* to *VDD_HV_IO_ETH* *Table 7 (Absolute maximum ratings)*: Added footnote *VDD_HV_IO refers to...* *Section 2.2.1, Power supply and reference voltage pins*: Added 2 sentences starting from *The Supply Pins Table contains...* *Table 8 (ESD ratings,)*: Added classification column *Table 9 (Device operating conditions)*: Removed rows $V_{DD\_HV\_ADR\_D}$ and $V_{DD\_HV\_ADR\_S}$ For row $V_{DD\_HV\_ADR}$: divided Value Min column data into “C” (3.0) and “P” (4.0) values and added the word *reference* to the Parameter description column Changed row $V_{SS\_HV\_ADR}$ symbol (was $V_{SS\_HV\_ADR\_D}$) Changed VDD_HV_ADV Value Min column data for *P* characteristic to 4.0 (was 4.2) *Table 9 (Device operating conditions)*: For row $V_{DD\_HV\_ADR}$: inverted the *C* and *P* Parameter Classification values. *Table 10 (DC electrical specifications)*: Removed the following rows: $V_{DD\_HV\_IO}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_ETH}$, $V_{DD\_HV\_ADV}$, $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$ – $V_{DD\_HV\_ADV}$ *Table 12 (I/O input DC electrical characteristics)*: In row V_{IHTTL} condition changed to 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. In row V_{ILTTL} condition changed to 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. In row V_{HYSTTL} condition changed to 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. In row V_{IHCMOS_H} condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V. In row V_{IHCMOS} condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V. In row V_{ILCMOS_H} condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V. In row $V_{HYSCMOS}$ condition changed to 2.7 V < $V_{DD\_HV\_IO}$ < 3.0 V and 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V.

Table 55. Document revision history (continued)

Date	Revision	Changes
18-May-2015	3 (cont.)	*Section 3.17.5, GPIO delay timing*: Added this section. Replaced “four” with “three” in the table footnotes in *Table 51 (eTQFP80 – STMicroelectronics package mechanical data)* and *Table 52 (eTQFP100 – STMicroelectronics package mechanical data)*. *Table 51 (eTQFP80 – STMicroelectronics package mechanical data)*: Second note removed from E2 parameter and added to E3 parameter. *Table 53 (Thermal characteristics for eTQFP80)*: Updated the table and its values. *Table 54 (Thermal characteristics for eTQFP100)*: Updated the table and its values. *Table 60 (Order codes (ST))* Updated the table.
15-Jun-2017	4	Following are the changes in this version of the Datasheet: Replaced eLQFP100 with eTQFP100 throughout the document. Removed all requirement tagging from the document. Replaced RPNs: SPC572L64F2B, SPC572L64E3B with SPC572Lx. Replaced SPC572LxB with SPC572Lx. Replaced bullet point “On-chip voltage...” with “Single 5V +/-10%....” on the cover page. *Table 1 (Device summary)*: – Updated the table. *Table 2 (SPC572Lx device feature summary)*: – Updated the notes of “External power supplies” *Section 3.4: Electromagnetic Compatibility (EMC)*: – Updated the section. *Table 9 (Device operating conditions)*: – Updated the values of parameter $V_{DD\_LV.}$ – Updated notes in the table. Removed section: “Temperature profile.” *Table 26 (SDn ADC electrical specification)*: – Updated the values for R_{BIAS} parameter. – Added parameters $Z_{DIFF,}$ Z_{CM}, and $\Delta V_{INTCM.}$ *Table 31 (Voltage regulator electrical characteristics)*: – Added parameter C_{DECFLA} *Table 32 (Voltage monitor electrical characteristics)*: – Added parameter V_{LVD108} *Section 4.3: eTQFP100 case drawing*: – Updated the *Figure 39: eTQFP100 – STMicroelectronics package mechanical drawing*. – Updated the *Table 52 (eTQFP100 – STMicroelectronics package mechanical data)*. *Section 5: Ordering information*: – Removed table: Order codes (ST). Added *Figure 40: Product code structure*.