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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b, 8x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84565vlkr

- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation parameters

- Up to 80 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-chip memory and memory protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.

- Support for simultaneous triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, FlexPWMs, PDBs, EWM, quadrature decoder, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

2 MC56F8458x signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIO_x_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- There are 2 PWM modules: PWM**A**, PWM**B**. Each PWM module has 4 submodules: PWMA has PWMA_**0**, PWMA_**1**, PWMA_**2**, PWMA_**3**; PWMB has PWMB_0, PWMB_1, PWMB_2, PWMB_3. Each PWM module's submodules have 3 pins (A, B, X) each, with the syntax for the pins being PWMA_0**A**, PWMA_0**B**, PWMA_0**X**, and PWMA_1A, PWMA_1B, PWMA_1X, and so on. Each submodule pin can be configured as a PWM output or as a capture input.
- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA (or PWMB) outputs, in cases where the fault conditions originate off-chip.
- EWM_OUT_B is the output of the External Watchdog Module (EWM), and is active low (denoted by the "_B" part of the syntax).

For the MC56F84**58X** family, which uses 80-pin LQFP and 100-pin LQFP packages:

Table 2. Signal descriptions

Signal Name	100 LQFP	80 LQFP	Type	State During Reset[1]	Signal Description
V_{DD}	7	-	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
V_{DD}	43	35			
V_{DD}	67	54			
V_{DD}	96	76			
V_{SS}	8	-	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
V_{SS}	15	11			
V_{SS}	44	36			
V_{SS}	66	53			
V_{SS}	97	77			
V_{DDA}	31	26	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	32	27	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	Type	State During Reset[1]	Signal Description
GPIOA3	25	20	Input/Output	Input	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)			Input		ANA3 is input to channel 3 of ADCA; VREFLA is the reference low of ADCA; CMPA_IN2 is input 2 of analog comparator A. When used as an analog input, the signal goes to both places (ANA3 and CMPA_IN2), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin. This input can be configured as either ANA3 or VREFLA using the ADCA control register.
GPIOA4	21	16	Input/Output	Input	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&ANC8&CMPD_IN0)			Input		ANA4 is input to channel 4 of ADCA; ANC8 is input to channel 8 of ADCC; CMPD_IN0 is input 0 to comparator D. When used as an analog input, the signal goes to all three places (ANA4 and ANC8 and CMPA_IN0), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA5	20	15	Input/Output	Input	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&ANC9)			Input		ANA5 is input to channel 5 of ADCA; ANC9 is input to channel 9 of ADCC. When used as an analog input, the signal goes to both places (ANA5 and ANC9), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA6	19	14	Input/ Output	Input	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&ANC10)			Input		ANA6 is input to channel 5 of ADCA; ANC10 is input to channel 10 of ADCC. When used as an analog input, the signal goes to both places (ANA6 and ANC10), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA7	17	13	Input/Output	Input	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&ANC11)			Input		ANA7 is input to channel 7 of ADCA; ANC11 is input to channel 11 of ADCC. When used as an analog input, the signal goes to both places (ANA7 and ANC11), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	Type	State During Reset[1]	Signal Description
GPIOD7	47	37	Input/ Output	Input	GPIO Port D7: After reset, the default state is GPIOD7.
(XB_OUT11)			Output		Crossbar module output 11
(XB_IN7)			Input		Crossbar module input 7
(MISO1)			Input/ Output		Master in/slave out for SPI1 — In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOE0	68	55	Input/ Output	Input	GPIO Port E0: After reset, the default state is GPIOE0.
PWMA_0B			Input/ Output		PWM module A, submodule 0, output B or input capture B
GPIOE1	69	56	Input/ Output	Input	GPIO Port E1: After reset, the default state is GPIOE1.
(PWMA_0A)			Input/ Output		PWM module A, submodule 0, output A or input capture A
GPIOE2	74	59	Input/ Output	Input	GPIO Port E2: After reset, the default state is GPIOE2.
(PWMA_0B)			Input/ Output		PWM module A, submodule 0, output B or input capture B
GPIOE3	75	60	Input/ Output	Input	GPIO Port E3: After reset, the default state is GPIOE3.
(PWMA_1A)			Input/ Output		PWM module A, submodule 1, output A or input capture A
GPIOE4	82	65	Input/ Output	Input	GPIO Port E4: After reset, the default state is GPIOE4.
(PWMA_2B)			Input/ Output		PWM module A, submodule 2, output B or input capture B
(XB_IN2)			Input		Crossbar module input 2
GPIOE5	83	66	Input/ Output	Input	GPIO Port E5: After reset, the default state is GPIOE5.
(PWMA_2A)			Input/ Output		PWM module A, submodule 2, output A or input capture A
(XB_IN3)			Input		Crossbar module input 3
GPIOE6	84	67	Input/ Output	Input	GPIO Port E6: After reset, the default state is GPIOE6.
(PWMA_3B)			Input/ Output		PWM module A, submodule 3, output B or input capture B
(XB_IN4)			Input		Crossbar module input 4
(PWMB_2B)			Input/ Output		PWM module B (enhanced), submodule 2, output B or input capture B

Table continues on the next page...

6.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

6.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

6.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

6.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

6.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

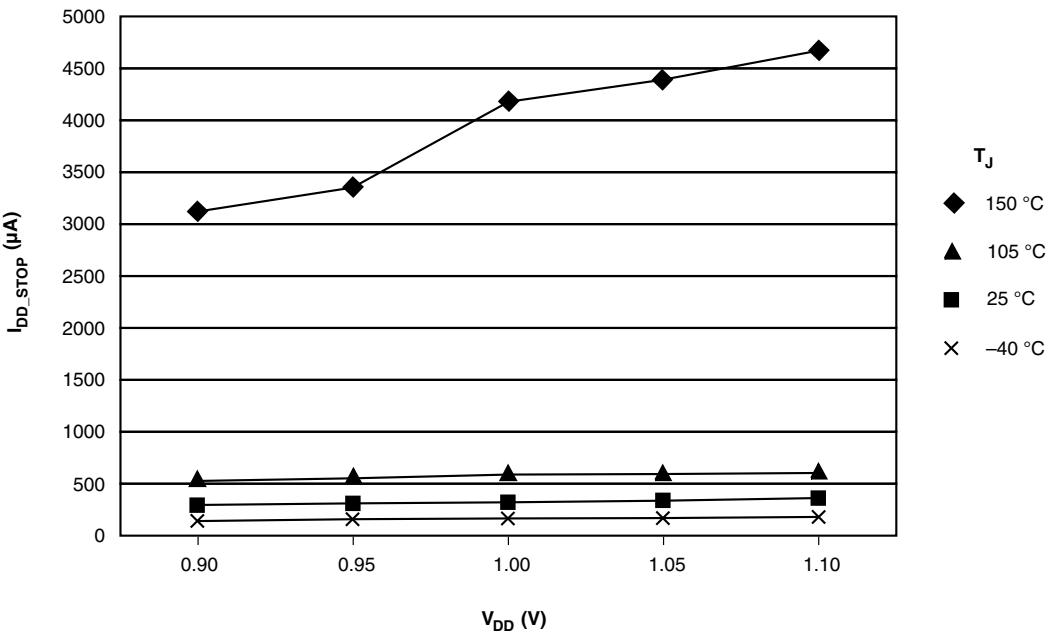
6.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

6.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



6.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

8.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

Table 8. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High	I_{IH}	Pin Group 1	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
pull-up enabled or disabled		Pin Group 2					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	—	50	kΩ	—
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	—	50	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ || C_{LD} = 400 pF
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

8.3.4 Power mode operating behaviors

Parameters listed are guaranteed by design.

NOTE

To filter noise on the RESETB pin, install a capacitor (up to 0.1 uF) on it.

Table 9. Reset, stop, wait, and interrupt timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.

NOTE

In the Table 9, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 80MHz, T=12.5ns. At 4MHz (used coming out of reset and stop modes), T=250ns.

Table 10. Power-On-Reset mode transition times

Symbol	Description	Min	Max	Unit	Notes
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7V to when the first instruction executes (over the operating temperature range).	199	225	us	
	LPS mode to LPRUN mode	240	551	us	4
	VLPS mode to VLPRUN mode	1424	1500	us	5
	STOP mode to RUN mode	6.79	7.29	us	3
	WAIT mode to RUN mode	0.570	0.650	us	2
	VLPWAIT mode to VLPRUN mode	1413	1500	us	5
	LPWAIT mode to LPRUN mode	237.2	554	us	4

1. Normal boot (FTFL_OPT[LPBOOT]=1)
2. Clock configuration: CPU clock = 80 MHz, bus clock = 80 MHz, flash clock = 20 MHz
3. Clock configuration: CPU clock = 4 MHz, system clock source is 8 MHz IRC
4. CPU Clock = 200 kHz and 8 Mhz IRC in standby mode
5. Clock configuration: Using 64 kHz external clock source, CPU Clock = 32 kHz

8.3.5 Power consumption operating behaviors

Table 11. Current Consumption

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	80 MHz	• 80 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 1X clock • ADC/DAC powered on and clocked at 5 MHz[2] • Comparator powered on	42.1 mA	16.3 mA	71.6 mA	26 mA
WAIT	80 MHz	• 80 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 2X clock • ADC/DAC/Comparator powered off	35.8 mA	13.52 µA	61.8 mA	45.00 µA
STOP	4 MHz	• 4 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/DAC/Comparator powered off	9.09 mA	13.14 µA	28.70 mA	43.20 µA
LPRUN (LsRUN)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • Repeat NOP instructions • All peripheral modules enabled, except NanoEdge and cyclic ADCs[3] • Simple loop with running from platform instruction buffer	1.86 mA	3.33 mA	20.86 mA	5.30 mA
LPWAIT (LsWAIT)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • All peripheral modules enabled, except NanoEdge and cyclic ADCs[3] • Processor core in wait mode	1.83 mA	2.67 mA	20.66 mA	5.30 mA

Table continues on the next page...

Table 11. Current Consumption (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
LPSTOP (LsSTOP)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off[3] • Processor core in stop mode	1.06 mA	13.13 µA	19.84 mA	43.2 µA
VLPRUN	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer	0.57 mA	12.22 µA	12.39 mA	17.40 µA
VLPWAIT	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode	0.56 mA	11.44 µA	12.30 mA	15.00 µA
VLPSTOP	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode	0.56 mA	10.44 µA	12.21 mA	13.14 µA

1. No output switching, all ports configured as inputs, all inputs low, no DC loads
2. ADC power consumption at higher frequency can be found in Table 28
3. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 250 kHz, because of the fixed frequency ratio of 1:4 between the CPU clock and the flash clock (when using a 2 MHz external input clock and the CPU is operating at 1 MHz).

8.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

8.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

8.4 Switching specifications

8.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 80 80	MHz	
f_{IPBUS}	IP bus clock	—	80	MHz	

8.4.2 General switching timing

Table 14. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	2
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	3
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	3

Table continues on the next page...

Table 14. Switching timing (continued)

Symbol	Description	Min	Max	Unit	Notes
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	4
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	4

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. The greater synchronous and asynchronous timing must be met.
3. 75 pF load
4. 15 pF load

8.5 Thermal specifications

8.5.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40		°C
T_A	Ambient temperature (extended industrial)	–40		°C

8.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See Thermal design considerations for more detail on thermal design considerations.

Board type	Symbol	Description	80 LQFP	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	55	62	°C/W	1, 2

Table continues on the next page...

9.2 System modules

9.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the MC56F84xxx's core logic. For proper operations, the voltage regulator requires an external 2.2 µF capacitor on each V_{CAP} pin. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 17.

Table 17. Regulator 1.2 V parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600	—	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 18. Bandgap electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

9.3 Clock modules

9.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 19. External clock operation timing requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

9.3.4 Relaxation oscillator timing

Table 22. Relaxation oscillator electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C		 7.84 7.76 266.8	 8 8 402	 8.16 8.24 554.3	 MHz kHz
8 MHz Frequency Variation RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C			 +/- 1.5 +/- 1.5	 +/-2 +/-3	 %
32 kHz Output Frequency[2] RUN Mode • -40°C to 105°C		 30.1	 32	 33.9	 kHz
32 kHz Output Frequency Variation RUN Mode Due to temperature • -40°C to 105°C			 +/-2.5	 +/-4	 %
Stabilization Time • 8 MHz output[3] • 32 kHz output[4]	tstab		0.12 14.4	0.4 16.2	µs
Output Duty Cycle		48	50	52	%

1. Frequency after application of 8 MHz trim
2. Frequency after application of 32 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

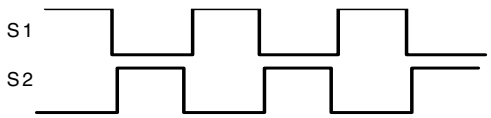


Figure 9. Equivalent circuit for A/D loading

9.5.2 16-bit SAR ADC electrical specifications

9.5.2.1 16-bit ADC operating conditions

Table 28. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	7
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.

Table 34. SPI timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Clock (SCK) high time Master Slave	t_{CH}	20 20	— —	ns ns	Figure 15 Figure 16 Figure 17 Figure 18
Clock (SCK) low time Master Slave	t_{CL}	20 20	— —	ns ns	Figure 18
Data set-up time required for inputs Master Slave	t_{DS}	20 1	— —	ns ns	Figure 15 Figure 16 Figure 17 Figure 18
Data hold time required for inputs Master Slave	t_{DH}	1 3	— —	ns ns	Figure 15 Figure 16 Figure 17 Figure 18
Access time (time to data active from high-impedance state) Slave	t_A	5	—	ns	Figure 18
Disable time (hold time to high-impedance state) Slave	t_D	5	—	ns	Figure 18
Data valid for outputs Master Slave (after enable edge)	t_{DV}	— —	6.25 18.7	ns ns	Figure 15 Figure 16 Figure 17 Figure 18
Data invalid Master Slave	t_{DI}	0 0	— —	ns ns	Figure 15 Figure 16 Figure 17 Figure 18
Rise time Master Slave	t_R	— —	1 1	ns ns	Figure 15 Figure 16 Figure 17 Figure 18
Fall time Master Slave	t_F	— —	1 1	ns ns	Figure 15 Figure 16 Figure 17 Figure 18

100 LQFP	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
45	—	GPIOF11	GPIOF11	TXD0	XB_IN11		
46	—	GPIOF15	GPIOF15	RXD0	XB_IN10		
47	37	GPIOD7	GPIOD7	XB_OUT11	XB_IN7	MISO1	
48	38	GPIOG11	GPIOG11	TB3	CLKO0	MOSI1	
49	39	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	
50	40	GPIOC7	GPIOC7	SS0_B	TXD0		
51	—	GPIOG10	GPIOG10	PWMB_2X	PWMA_2X	XB_IN8	SS2_B
52	41	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	
53	42	GPIOC9	GPIOC9	SCLK0	XB_IN4		
54	43	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	
55	44	GPIOF0	GPIOF0	XB_IN6	TB2	SCLK1	
56	45	GPIOF10	GPIOF10	TXD2	PWMA_FAULT6	PWMB_FAULT6	XB_OUT10
57	46	GPIOF9	GPIOF9	RXD2	PWMA_FAULT7	PWMB_FAULT7	XB_OUT11
58	47	GPIOC11	GPIOC11	CANTX	SCL1	TXD1	
59	48	GPIOC12	GPIOC12	CANRX	SDA1	RXD1	
60	49	GPIOF2	GPIOF2	SCL1	XB_OUT6		
61	50	GPIOF3	GPIOF3	SDA1	XB_OUT7		
62	51	GPIOF4	GPIOF4	TXD1	XB_OUT8		
63	52	GPIOF5	GPIOF5	RXD1	XB_OUT9		
64	—	GPIOG8	GPIOG8	PWMB_0X	PWMA_0X	TA2	XB_OUT10
65	—	GPIOG9	GPIOG9	PWMB_1X	PWMA_1X	TA3	XB_OUT11
66	53	VSS	VSS				
67	54	VDD	VDD				
68	55	GPIOE0	GPIOE0	PWMA_0B			
69	56	GPIOE1	GPIOE1	PWMA_0A			
70	57	GPIOG2	GPIOG2	PWMB_0B	XB_OUT4		
71	58	GPIOG3	GPIOG3	PWMB_0A	XB_OUT5		
72	—	GPIOE8	GPIOE8	PWMB_2B	PWMA_FAULT0		
73	—	GPIOE9	GPIOE9	PWMB_2A	PWMA_FAULT1		
74	59	GPIOE2	GPIOE2	PWMA_1B			
75	60	GPIOE3	GPIOE3	PWMA_1A			
76	61	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
77	62	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
78	63	GPIOG0	GPIOG0	PWMB_1B	XB_OUT6		
79	64	GPIOG1	GPIOG1	PWMB_1A	XB_OUT7		
80	—	GPIOG4	GPIOG4	PWMB_3B	PWMA_FAULT2		
81	—	GPIOG5	GPIOG5	PWMB_3A	PWMA_FAULT3		
82	65	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		
83	66	GPIOE5	GPIOE5	PWMA_2A	XB_IN3		
84	67	GPIOE6	GPIOE6	PWMA_3B	XB_IN4	PWMB_2B	
85	68	GPIOE7	GPIOE7	PWMA_3A	XB_IN5	PWMB_2A	

100 LQFP	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
86	69	GPIOG6	GPIOG6	PWMA_FAULT4	PWMB_FAULT4	TB2	XB_OUT8
87	70	GPIOC14	GPIOC14	SDA0	XB_OUT4		
88	71	GPIOC15	GPIOC15	SCL0	XB_OUT5		
89	—	GPIOF12	GPIOF12	MISO1	PWMB_FAULT2		
90	—	GPIOF13	GPIOF13	MOSI1	PWMB_FAULT1		
91	—	GPIOF14	GPIOF14	SCLK1	PWMB_FAULT0		
92	72	GPIOG7	GPIOG7	PWMA_FAULT5	PWMB_FAULT5	XB_OUT9	
93	73	VCAP	VCAP				
94	74	GPIOF6	GPIOF6	TB2	PWMA_3X	PWMB_3X	XB_IN2
95	75	GPIOF7	GPIOF7	TB3	CMPC_O	SS1_B	XB_IN3
96	76	VDD	VDD				
97	77	VSS	VSS				
98	78	TDO	TDO	GPIOD1			
99	79	TMS	TMS	GPIOD3			
100	80	TDI	TDI	GPIOD0			

12.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

Table 39. Revision history

Rev.	Date	Substantial Changes

3	06/2014	Changes include:
		• Updates and corrections to "56F844xx/5xx/7xx family" table.
		• In "Interrupt Controller" section, added info about Interrupt level 3.
		• In "Enhanced Flex Pulse Width Modulator (eFlexPWM)" section,
		  • Upated PWM frequencies based on device frequency, plus updated resolution of fractional clock digital dithering.
		  • Updated feature list.
		• Added new section "MC56F844xx signal and pin descriptions".
		• In "Signal groups" section, in "Functional Group Pin Allocations" table, made corrections to "Functional Group Pin Allocations" table.
		• In "Voltage and current operating requirements" section, added RESET voltage high to "Recommended Operating Conditions" table.
		• In "Voltage and current operating behaviors" section, in "DC Electrical Characteristics" table, updated Digital Input Current High for Pin Group 2.
		• For "Power mode transition operating behaviors" section,
		  • Changed the name to "Power mode operating behaviors".
		  • In "Reset, Stop, Wait, and Interrupt Timing" table, updated "RESET deassertion to First Address Fetch" parameters.
		  • Added new table "Power-On-Reset mode transition times".
		• In "Power consumption operating behaviors" section, updated mode currrent values in "Current Consumption" table.
		• In "JTAG Timing" section, changed "TCK frequency of operation" to SYS_CLK/16 from SYS_CLK/8.
		• In "System modules" section, in "Voltage regulator specifications" section, in "Regulator 1.2 V parameters" table, updated "Short Circuit Current" parameter.
		• In "Relaxation Oscillator Timing" section, updates in "Relaxation Oscillator Electrical Specifications" table.
		• In "Memories and memory interfaces" section,
		  • "Flash Memory Characteristics" section is now called "Flash electrical specifications" section.
		  • Added new section "Flash timing specifications — program and erase", where the "Flash Timing Parameters" table (now called "NVM program/erase timing specifications" table, and table was updated.
		  • Added new section "Flash high voltage current behaviors".
		• In "Analog" section, in "12-bit cyclic Analog-to-Digital Converter (ADC) parameters" section, updated "12-bit ADC electrical specifications" table.
		• In "Pinout" section, in "Signal Multiplexing and Pin Assignments" section,
		  • Added 2 notes.
		• In "Product Documentation" section, in "Device Documentation" table, removed Serial Bootloader User Guide, because it is not used for these devices.