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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Ethernet, I²C, TDM, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8113tvt3600v

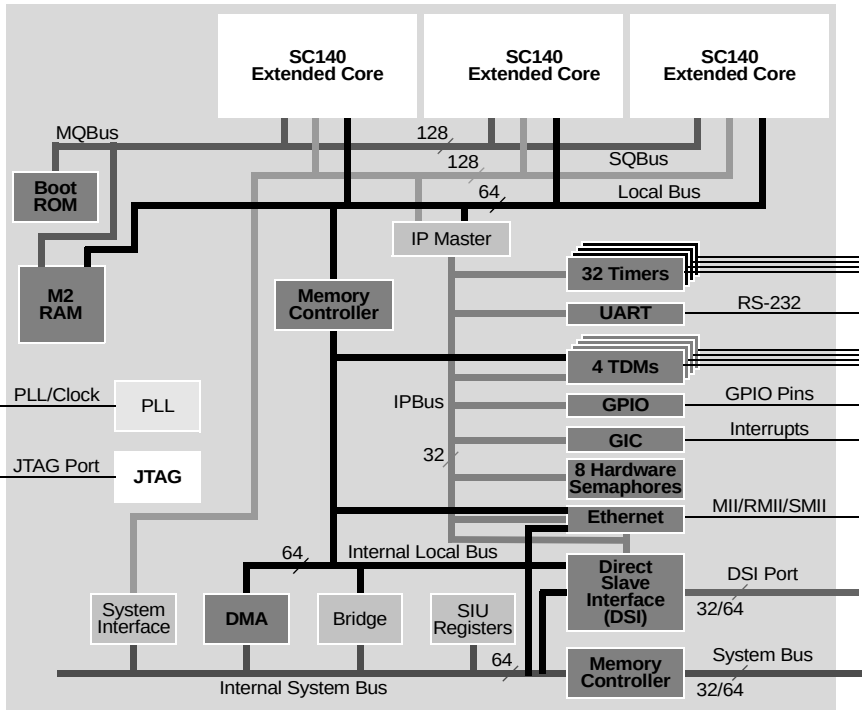
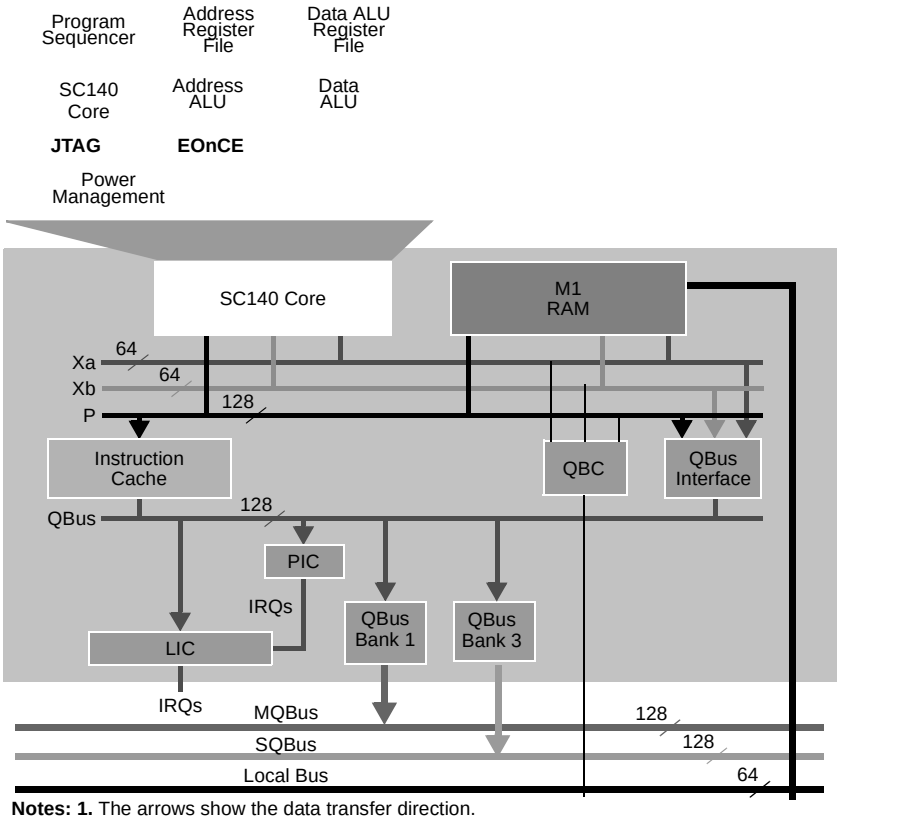


Figure 1. MSC8113 Block Diagram



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore® SC140 DSP Extended Core Block Diagram

Top View

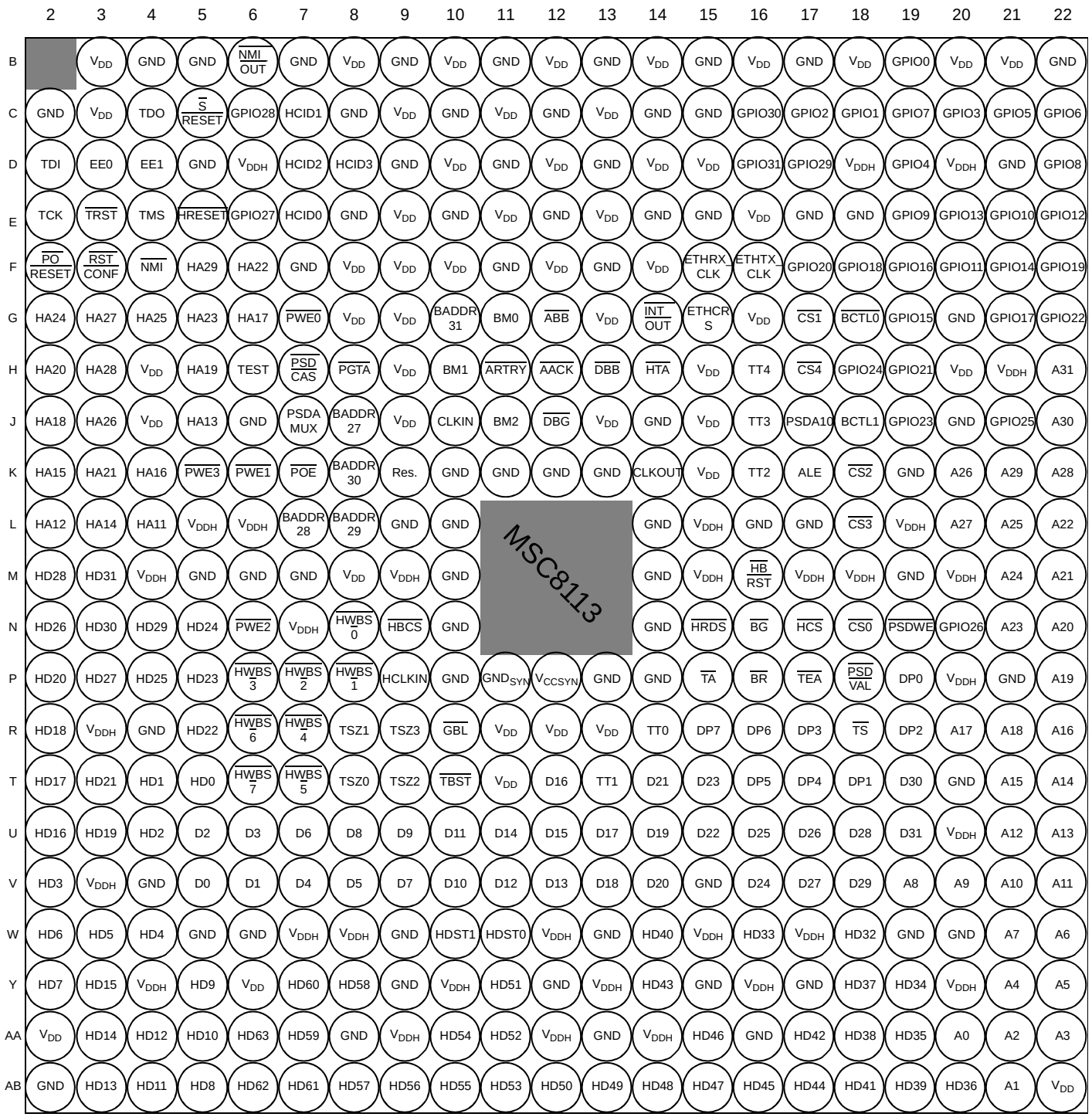


Figure 3. MSC8113 Package, Top View

Bottom View

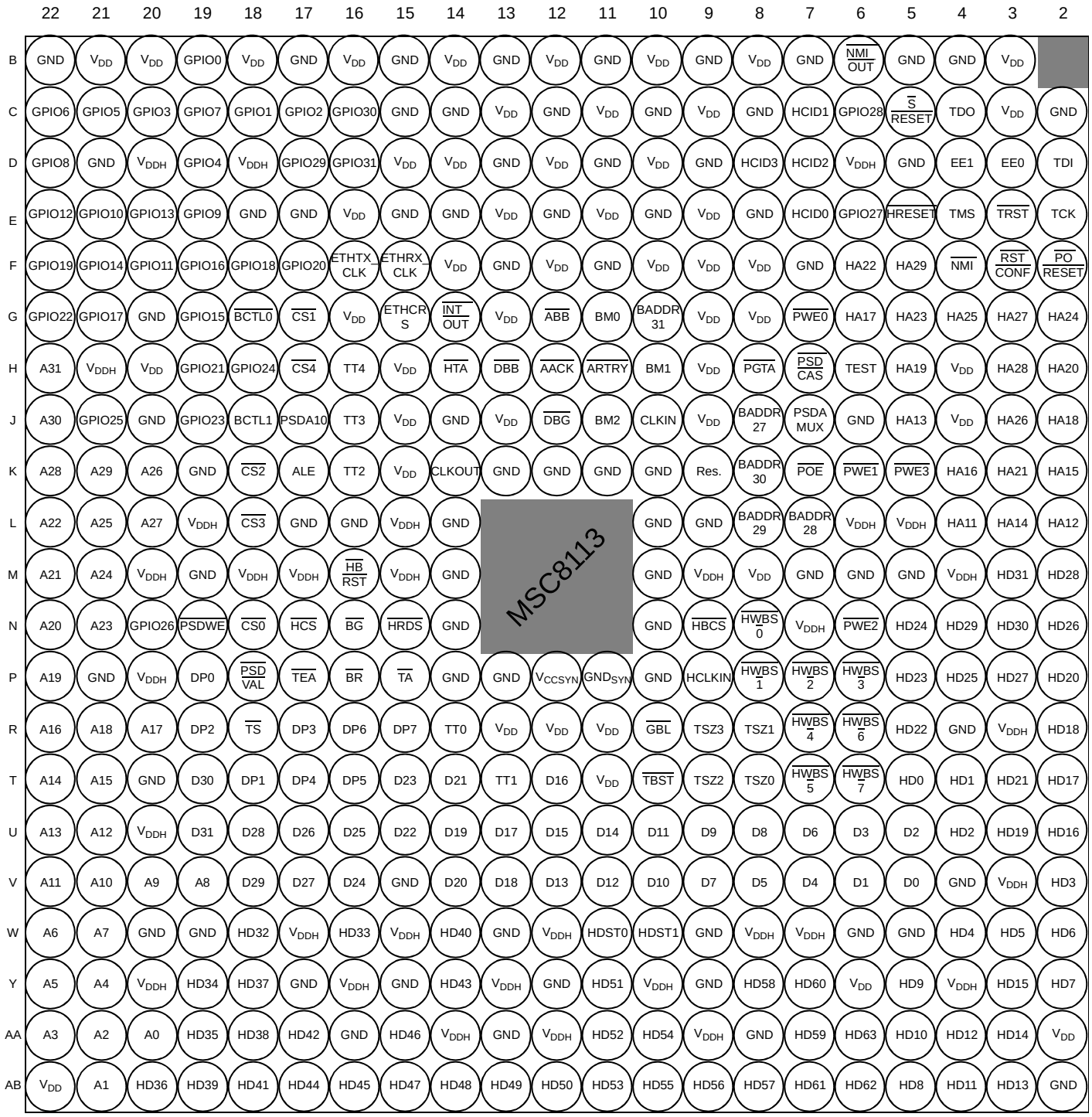


Figure 4. MSC8113 Package, Bottom View

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
E12	GND	G6	HA17
E13	V_{DD}	G7	PWE0/PSDDQM0/PBS0
E14	GND	G8	V_{DD}
E15	GND	G9	V_{DD}
E16	V_{DD}	G10	IRQ3/BADDR31
E17	GND	G11	BM0/TC0/BNKSEL0
E18	GND	G12	ABB/IRQ4
E19	GPIO9/TDM2TSYN/IRQ7/ETHMDIO	G13	V_{DD}
E20	GPIO13/TDM2RCLK/IRQ11/ETHMDC	G14	IRQ7/INT_OUT
E21	GPIO10/TDM2TCLK/IRQ8/ETHRX_DV/ETHCRS_DV/NC	G15	ETHCRS/ETHRXD
E22	GPIO12/TDM2RSYN/IRQ10/ETHRXD1/ETHSYNC	G16	V_{DD}
F2	PORESET	G17	CS1
F3	RSTCONF	G18	BCTL0
F4	NMI	G19	GPIO15/TDM1TSYN/DREQ1
F5	HA29	G20	GND
F6	HA22	G21	GPIO17/TDM1TDAT/DACK1
F7	GND	G22	GPIO22/TDM0TCLK/DONE2/DRACK2
F8	V_{DD}	H2	HA20
F9	V_{DD}	H3	HA28
F10	V_{DD}	H4	V_{DD}
F11	GND	H5	HA19
F12	V_{DD}	H6	TEST
F13	GND	H7	PSDCAS/PGPL3
F14	V_{DD}	H8	PGTA/PUPMWAIT/PGPL4/PPBS
F15	ETHRX_CLK/ETHSYNC_IN	H9	V_{DD}
F16	ETHTX_CLK/ETHREF_CLK/ETHCLOCK	H10	BM1/TC1/BNKSEL1
F17	GPIO20/TDM1RDAT	H11	ARTRY
F18	GPIO18/TDM1RSYN/DREQ2	H12	AACK
F19	GPIO16/TDM1TCLK/DONE1/DRACK1	H13	DBB/IRQ5
F20	GPIO11/TDM2TDAT/IRQ9/ETHRX_ER/ETHTXD	H14	HTA
F21	GPIO14/TDM2RDAT/IRQ12/ETHRXD0/NC	H15	V_{DD}
F22	GPIO19/TDM1RCLK/DACK2	H16	TT4/CS7
G2	HA24	H17	CS4
G3	HA27	H18	GPIO24/TDM0RSYN/IRQ14
G4	HA25	H19	GPIO21/TDM0TSYN
G5	HA23	H20	V_{DD}

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8113 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8113.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core and PLL supply voltage	V_{DD}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	–0.2 to 4.0	V
Maximum operating temperature:	T_J	105	°C
Minimum operating temperature	T_J	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core and PLL supply voltage:	V_{DD} V_{CCSYN}	1.07 to 1.13	V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range:	T_J	–40 to 105	°C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8113 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8113

Characteristic	Symbol	FC-PBGA 20 × 20 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	19	15	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	9		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.9		°C/W
Junction-to-package-top[6]	Ψ_{JT}	1		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8113. The measurements in **Table 5** assume the following system conditions:

- T_A = 25 °C
- V_{DD} = 1.1 V nominal = 1.07–1.13 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD}.

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	—	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.8	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–1.0	0.09	1	µA
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, $V_{IL} = 0.8$ V[2]	I_L	–1.0	0.09	1	µA
Signal high input current, $V_{IH} = 2.0$ V[2]	I_H	–1.0	0.09	1	µA
Output high voltage, $I_{OH} = –2$ mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, $I_{OL} = 3.2$ mA	V_{OL}	—	0	0.4	V
Internal supply current: • Wait mode • Stop mode	 I_{DDW} I_{DDS}	 — —	 375[3] 290[3]	 — —	 mA mA
Typical power 400 MHz at 1.1 V[4] Typical power 300 MHz at 1.1 V[4]	P	— —	826 676	— —	mW mW

Notes:
1. See **Figure 5** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.1 V core at 25°C junction temperature.
4. The typical power values were calculated using a power calculator configured for three cores performing an EFR code with the device running at the specified operating frequency and a junction temperature of 25°C. No peripherals were included. The calculator was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Section 3** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

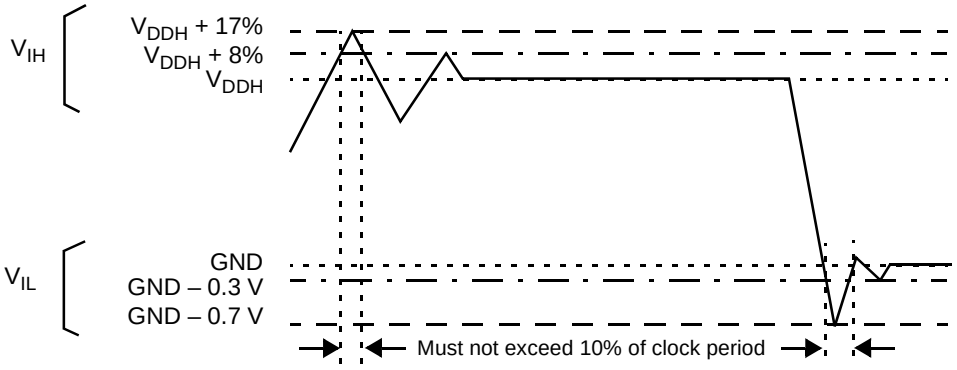


Figure 5. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

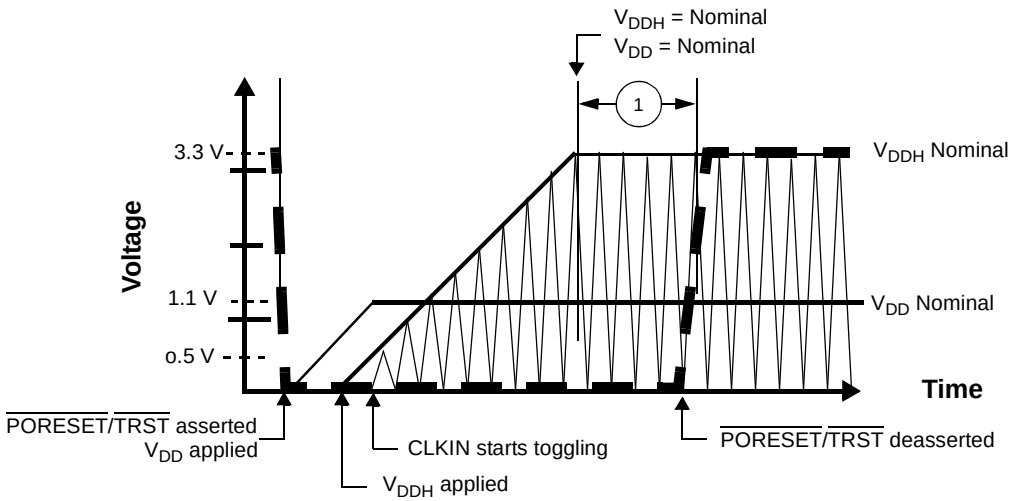


Figure 7. Start-Up Sequence: V_{DD} Raised Before V_{DDH} with CLKIN Started with V_{DDH}

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.

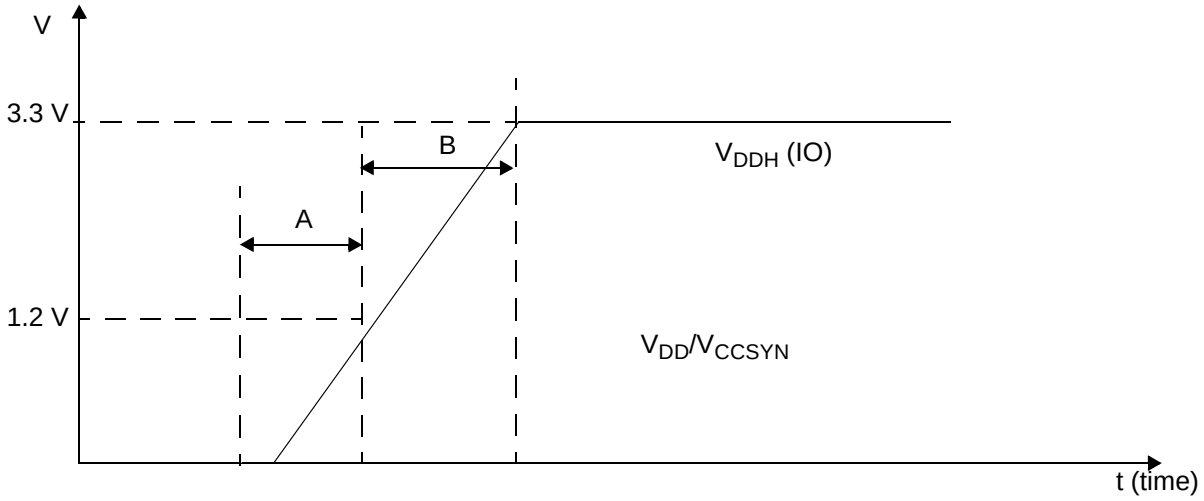


Figure 8. Power-Up Sequence for V_{DDH} and V_{DD}/V_{CCSYN}

The following rules apply:

1. During time interval A, V_{DDH} should always be equal to or less than the V_{DD}/V_{CCSYN} voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	300/400
Reference frequency (REFCLK)	100/133

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz
Internal bus frequency (BLCK)	100/133
DSI clock frequency (HCLKIN) • Core frequency = 300 MHz • Core frequency = 400 MHz	 HCLKIN ≤ (min{70 MHz, CLKOUT}) HCLKIN ≤ (min{100 MHz, CLKOUT})
External clock frequency (CLKIN or CLKOUT)	100/133

Table 8. Clock Frequencies

Characteristics	Symbol	300 MHz Device		400 MHz Device	
		Min	Max	Min	Max
CLKIN frequency	F_{CLKIN}	20	100	20	133.3
BCLK frequency	F_{BCLK}	40	100	40	133.3
Reference clock (REFCLK) frequency	F_{REFCLK}	40	100	40	133.3
Output clock (CLKOUT) frequency	F_{CLKOUT}	40	100	40	133.3
SC140 core clock frequency	F_{CORE}	200	300	200	400
Note: The rise and fall time of external clocks should be 3 ns maximum					

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
Phase jitter between BCLK and CLKIN	—	0.3	ns
CLKIN frequency	20	see **Table 8**	MHz
CLKIN slope	—	3	ns
PLL input clock (after predivider)	20	100	MHz
PLL output frequency (VCO output) • 300 MHz core • 400 MHz core	800	 1200 1600	MHz MHz MHz
CLKOUT frequency jitter[1]	—	200	ps
CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps.	—	500	ps
Notes: **1.** Peak-to-peak. **2.** Not tested. Guaranteed by design.			

2.5.4 Reset Timing

The MSC8113 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8113 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

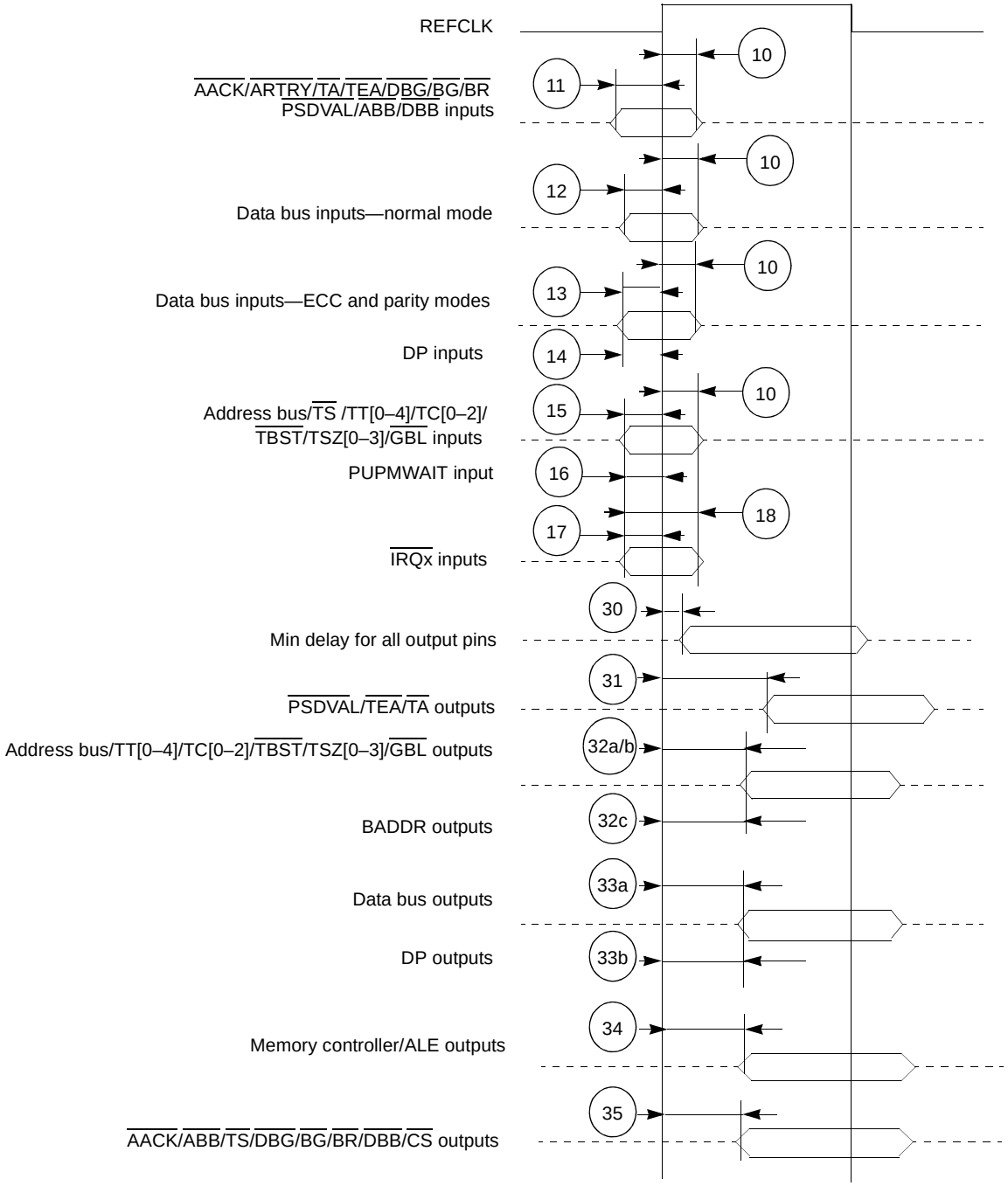


Figure 11. SIU Timing Diagram

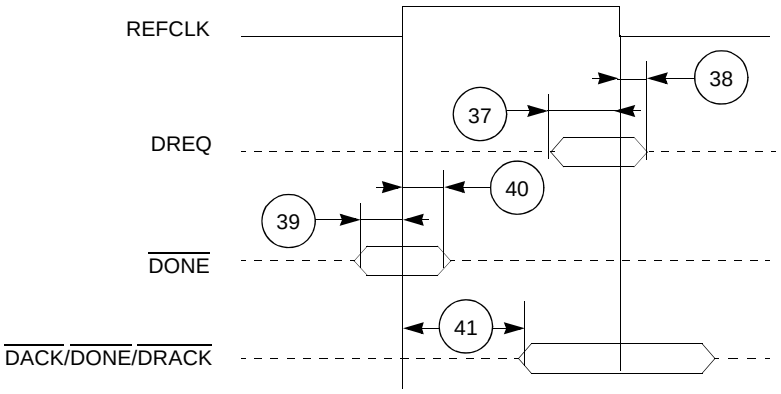


Figure 13. DMA Signals

2.5.6 DSI Timing

The timings in the following sections are based on a 20 pF capacitive load.

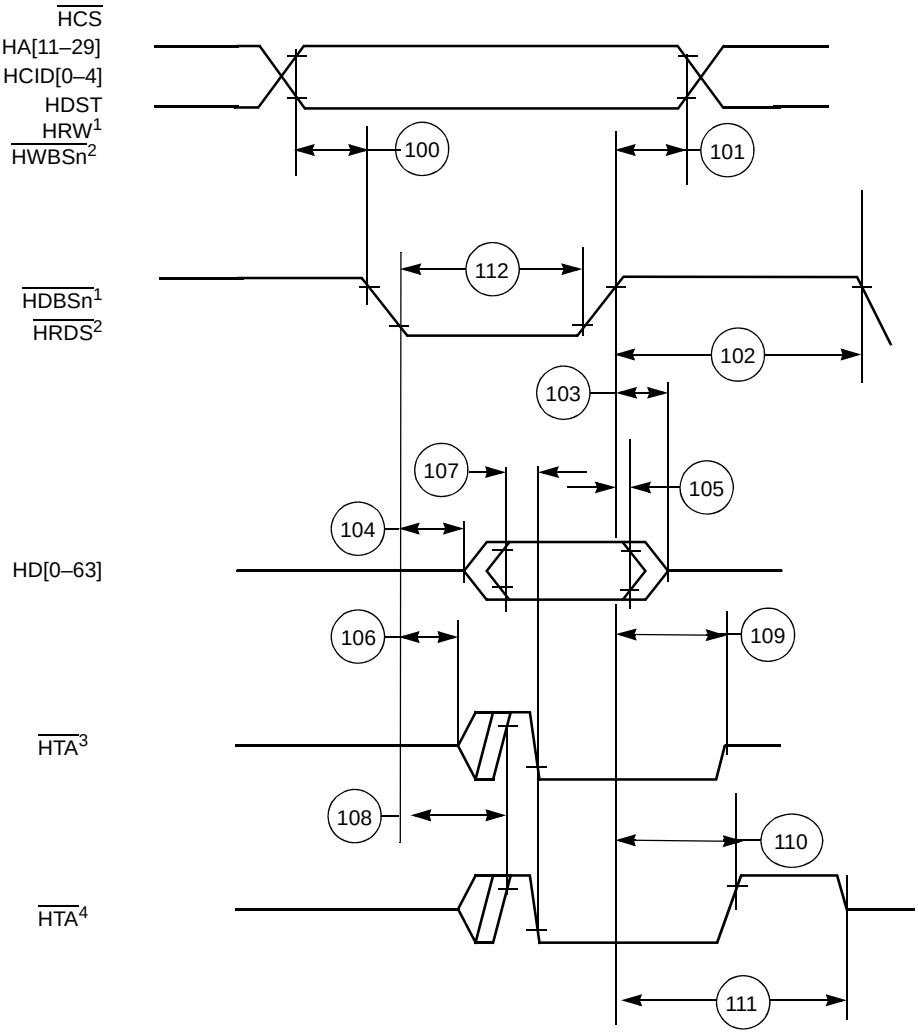
2.5.6.1 DSI Asynchronous Mode

Table 18. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] set-up time before strobe ($\overline{\text{HWBS[n]}}$) assertion	1.5	—	ns
101	Attributes[1] hold time after data strobe deassertion	1.3	—	ns
102	Read/Write data strobe deassertion width: • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	8.5	ns
104	Read data strobe assertion to output data active from high impedance	2.0	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance	2.2	—	ns
107	Output data valid to $\overline{\text{HTA}}$ assertion	3.2	—	ns
108	Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid[2]	—	7.4	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	6.5	ns
111	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input set-up time before write data strobe deassertion	1.0	—	ns
202	Host data input hold time after write data strobe deassertion	1.7	—	ns

Notes:
1. *Attributes* refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.
2. This specification is tested in dual-strobe mode. Timing in single-strobe mode is guaranteed by design.
3. All values listed in this table are tested or guaranteed by design.

Figure 14 shows DSI asynchronous read signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs in Synchronous Mode

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
120	HCLKIN cycle time[1,2]	HTC	10.0	55.6	ns
121	HCLKIN high pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
122	HCLKIN low pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.6	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

Table 20. DSI Outputs in Synchronous Mode

No.	Characteristic	1.1 V Core		Units
		Min	Max	
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	7.6	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	8.3	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.2	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	7.4	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	7.5	ns

2.5.10.4 SMII Mode

Table 27. SMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	—	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	1.5[1]	6.0[2]	ns

Notes: **1.** Measured using a 5 pF load.
2. Measured using a 15 pF load.

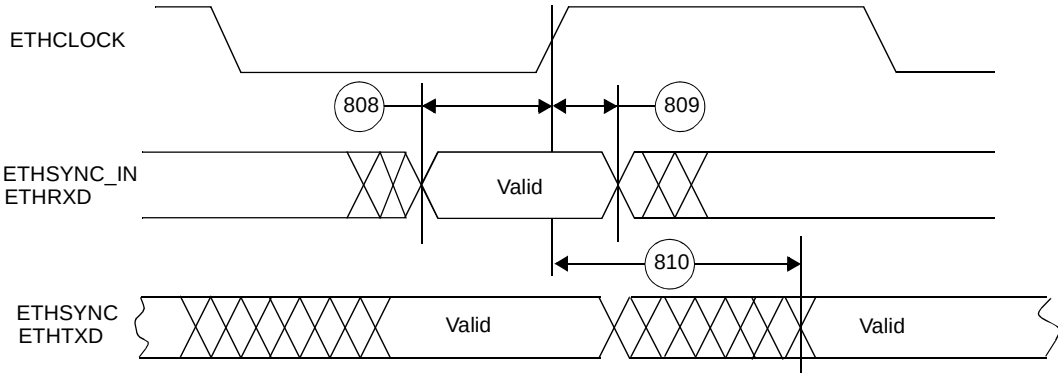


Figure 26. SMII Mode Signal Timing

2.5.11 GPIO Timing

Table 28. GPIO Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	6.1	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.1	—	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	3.5	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	ns

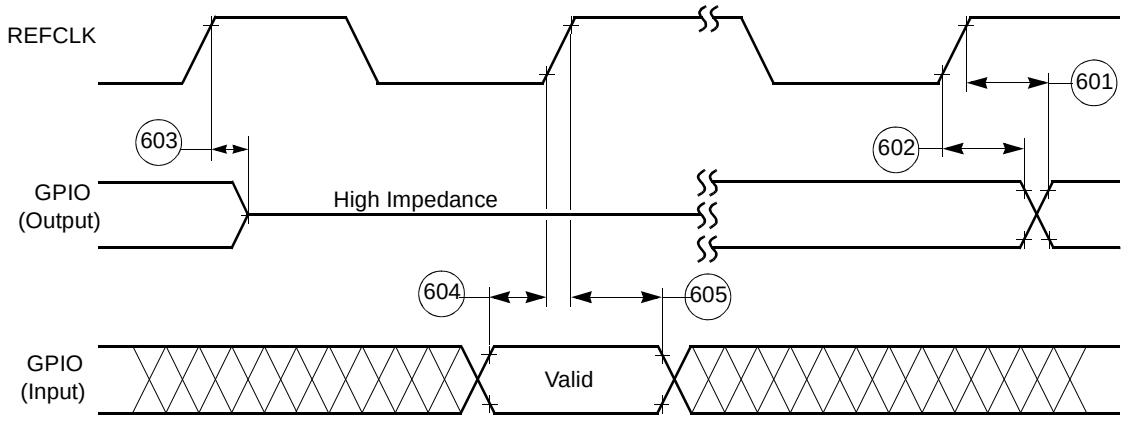


Figure 27. GPIO Timing

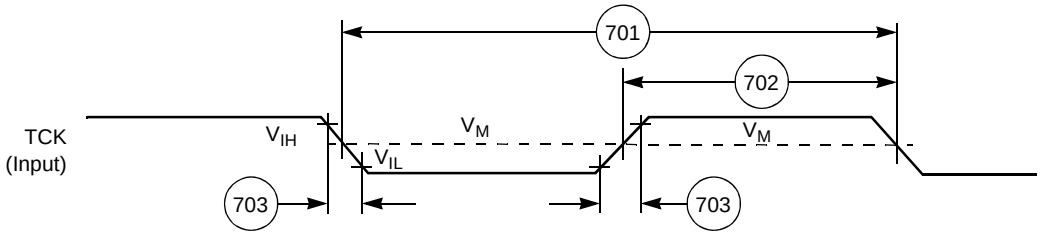


Figure 29. Test Clock Input Timing Diagram

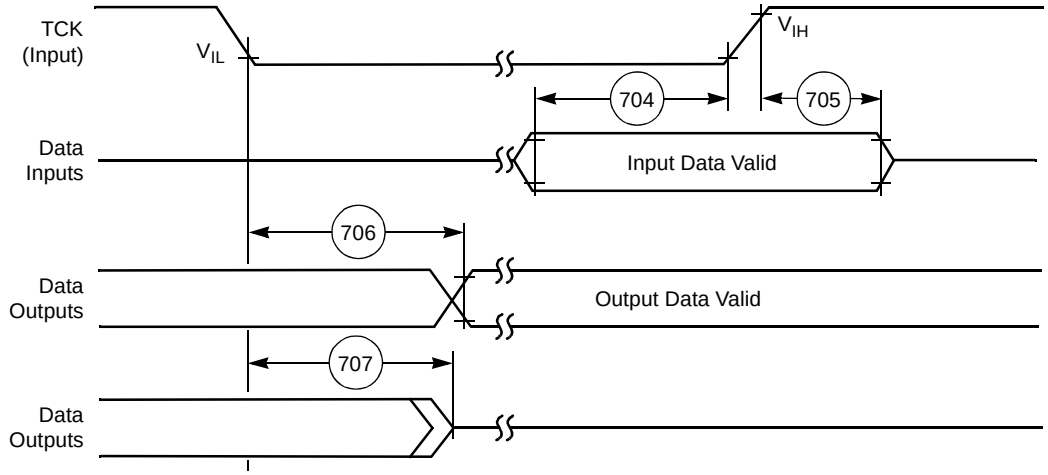


Figure 30. Boundary Scan (JTAG) Timing Diagram

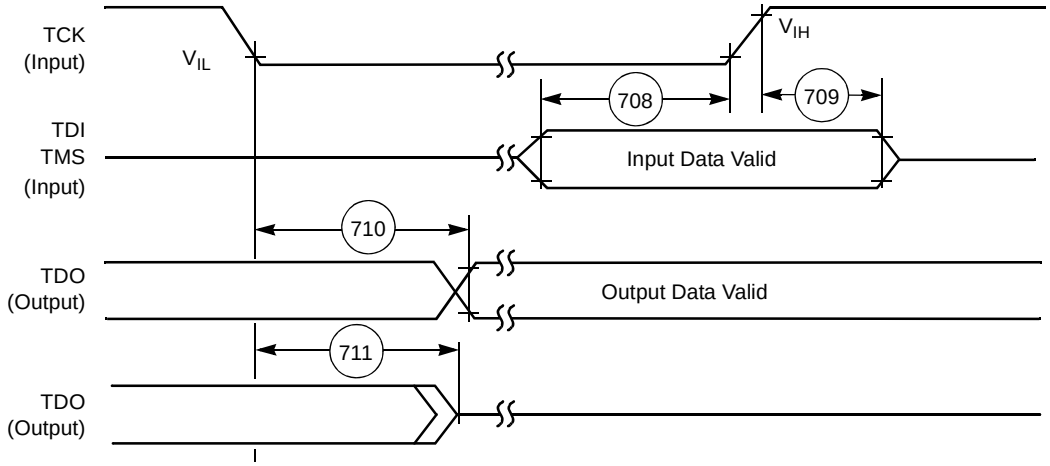


Figure 31. Test Access Port Timing Diagram

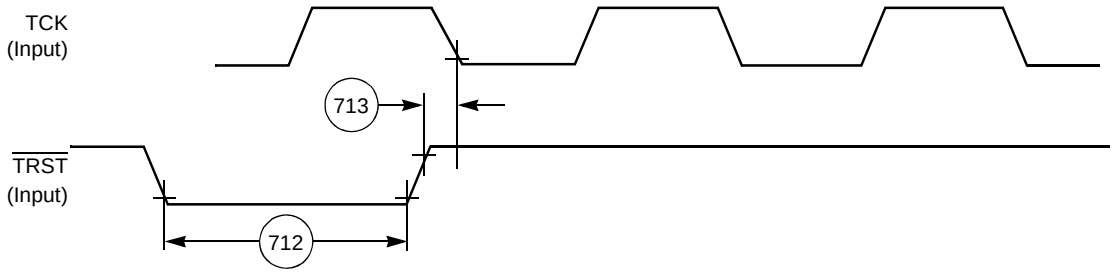


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8113 device is designed into a system.

3.1 Start-up Sequencing Recommendations

Use the following guidelines for start-up and power-down sequences:

- Assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ before applying power and keep the signals driven low until the power reaches the required minimum power levels. This can be implemented via weak pull-down resistors.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{\text{PORESET}}$ and after both power supplies have reached nominal voltage levels.
- If possible, bring up V_{DD}/V_{CCSYN} and V_{DDH} together. If it is not possible, raise V_{DD}/V_{CCSYN} first and then bring up V_{DDH}. V_{DDH} should not exceed V_{DD}/V_{CCSYN} until V_{DD}/V_{CCSYN} reaches its nominal voltage level. Similarly, bring both voltage levels down together. If that is not possible reverse the power-up sequence, with V_{DDH} going down first and then V_{DD}/V_{CCSYN}.

Note: This recommended power sequencing for the MSC8113 is different from the MSC8102.

External voltage applied to any input line must not exceed the I/O supply V_{DDH} by more than 0.8 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule. However, each such input can draw up to 80 mA per input pin per device in the system during start-up.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

3.2 Power Supply Design Considerations

When implementing a new design, use the guidelines described in the *MSC8113 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information.

Figure 33 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.1 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8113 device.

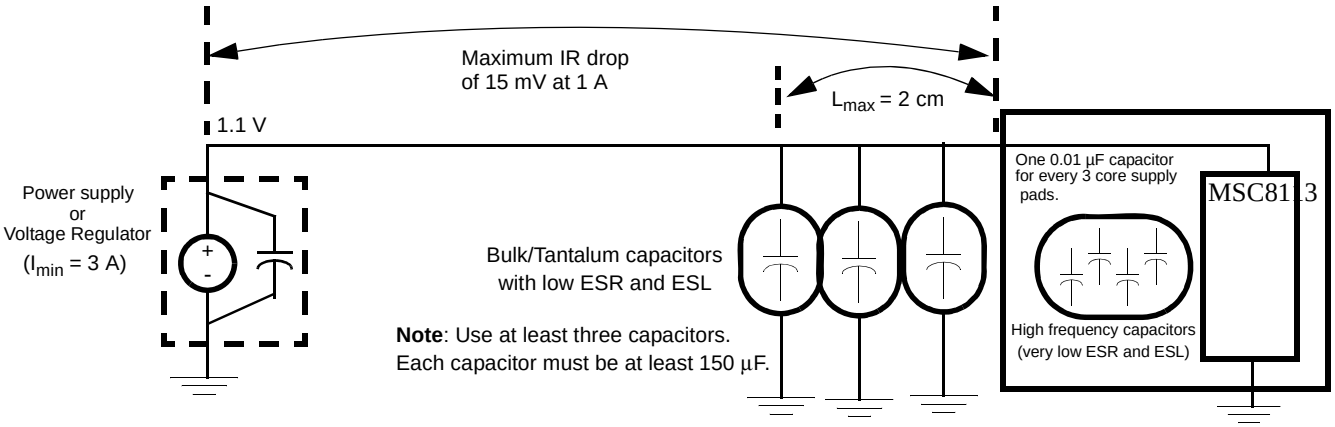


Figure 33. Core Power Supply Decoupling

- If there is an external bus master (BCR[EBM] = 1):
  - $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ must be pulled up.
  - $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{EXT\_BG[2–3]}}$, and $\overline{\text{EXT\_DBG[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be selected as $\overline{\text{IRQ}}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

Note: The MSC8113 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8113 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.

Note: See the Clock chapter in the *MSC8113 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8113 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DDH} or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

Note: For details on configuration, see the *MSC8113 User's Guide* and *MSC8113 Reference Manual*. For additional information, refer to the *MSC8113 Design Checklist* (ANxxxx).

3.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 133 MHz operation, you may have to use 133 or 166 MHz SDRAM. Always perform a detailed timing analysis using the MSC8113 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.

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Document Number: MSC8113
Rev. 1
12/2008

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