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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Ethernet, I²C, TDM, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8113tvt4800v

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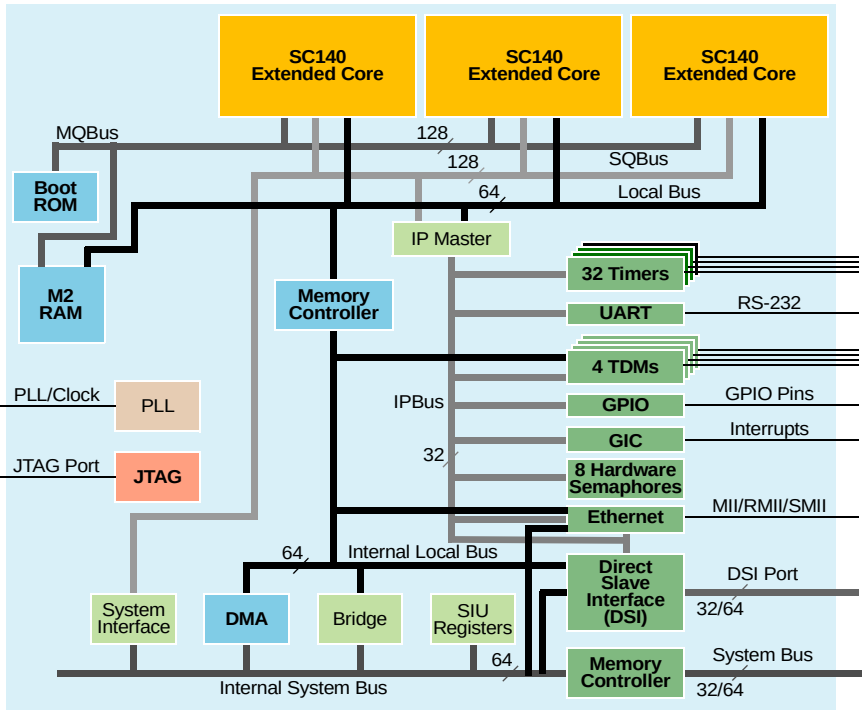
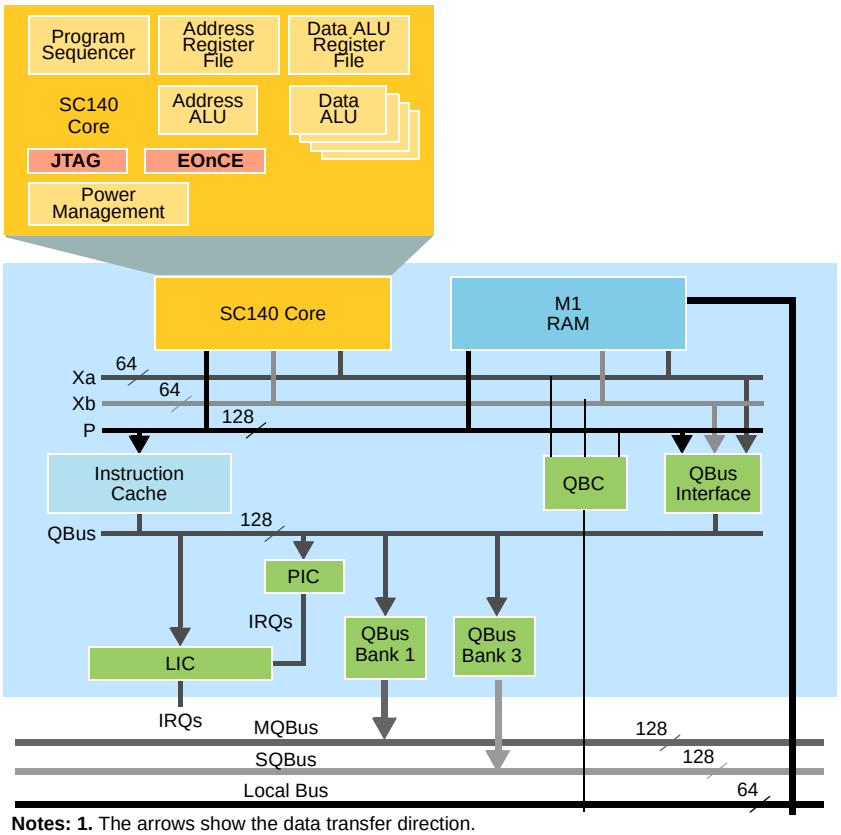


Figure 1. MSC8113 Block Diagram



Notes: **1.** The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore® SC140 DSP Extended Core Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC8113 package ball grid array layouts and pinout allocation tables.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Bottom View

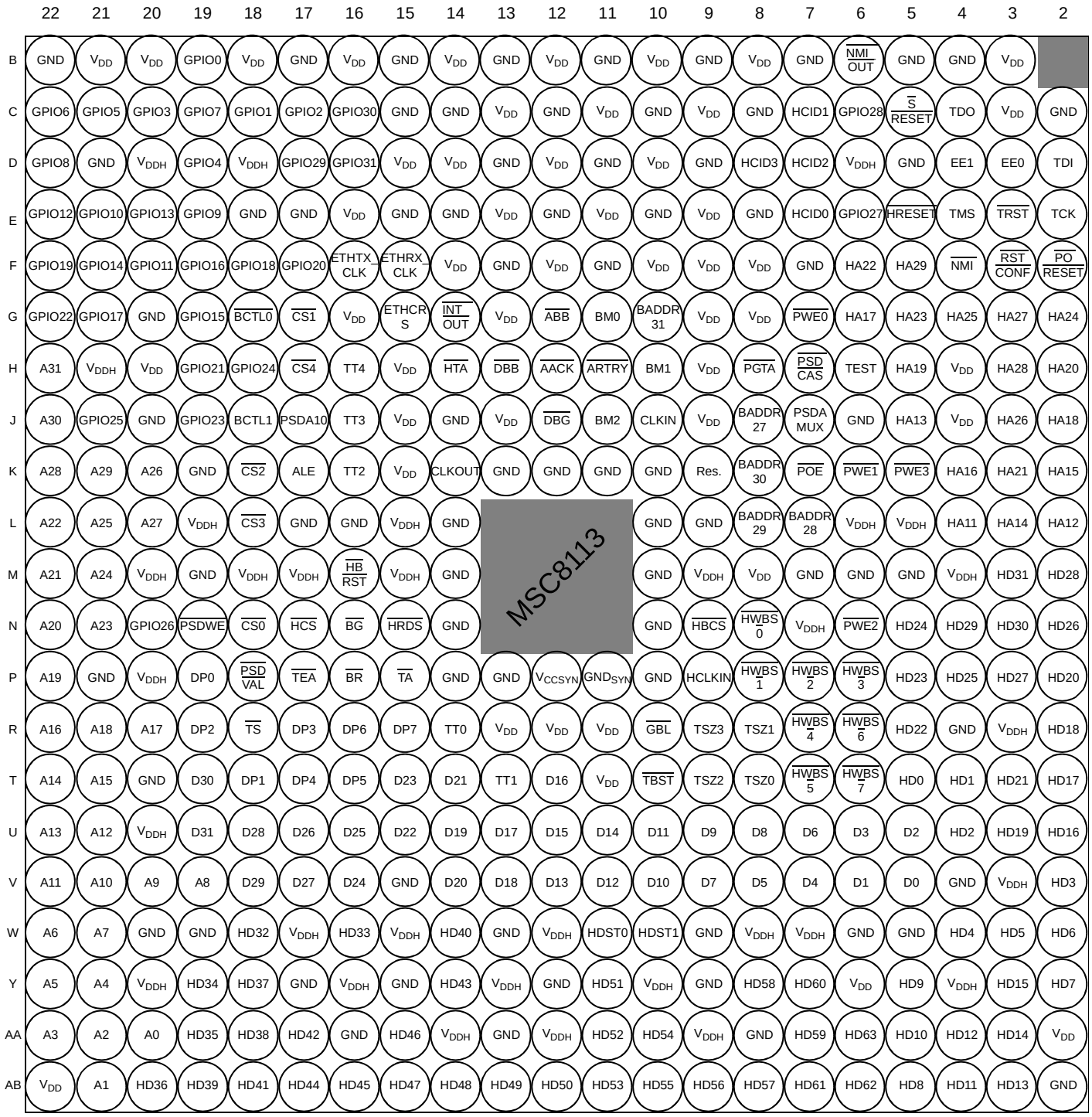


Figure 4. MSC8113 Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents signal list sorted by ball number. -

Table 1. MSC8113 Signal Listing by Ball Designator

Des.	Signal Name	Des.	Signal Name
B3	V_{DD}	C18	GPIO1/TIMER0/CHIP_ID1/$\overline{IRQ5}$/ETHTXD1
B4	GND	C19	GPIO7/TDM3RCLK/$\overline{IRQ5}$/ETHTXD3
B5	GND	C20	GPIO3/TDM3TSYN/$\overline{IRQ1}$/ETHTXD2
B6	$\overline{NMI\_OUT}$	C21	GPIO5/TDM3TDAT/$\overline{IRQ3}$/ETHRXD3
B7	GND	C22	GPIO6/TDM3RSYN/$\overline{IRQ4}$/ETHRXD2
B8	V_{DD}	D2	TDI
B9	GND	D3	EE0
B10	V_{DD}	D4	EE1
B11	GND	D5	GND
B12	V_{DD}	D6	V_{DDH}
B13	GND	D7	HCID2
B14	V_{DD}	D8	HCID3/HA8
B15	GND	D9	GND
B16	V_{DD}	D10	V_{DD}
B17	GND	D11	GND
B18	V_{DD}	D12	V_{DD}
B19	GPIO0/CHIP_ID0/$\overline{IRQ4}$/ETHTXD0	D13	GND
B20	V_{DD}	D14	V_{DD}
B21	V_{DD}	D15	V_{DD}
B22	GND	D16	GPIO31/TIMER3/SCL
C2	GND	D17	GPIO29/CHIP_ID3/ETHTX_EN
C3	V_{DD}	D18	V_{DDH}
C4	TDO	D19	GPIO4/TDM3TCLK/$\overline{IRQ2}$/ETHTX_ER
C5	$\overline{SRESET}$	D20	V_{DDH}
C6	GPIO28/UTXD/DREQ2	D21	GND
C7	HCID1	D22	GPIO8/TDM3RDAT/$\overline{IRQ6}$/ETHCOL
C8	GND	E2	TCK
C9	V_{DD}	E3	$\overline{TRST}$
C10	GND	E4	TMS
C11	V_{DD}	E5	$\overline{HRESET}$
C12	GND	E6	GPIO27/URXD/DREQ1
C13	V_{DD}	E7	HCID0
C14	GND	E8	GND
C15	GND	E9	V_{DD}
C16	GPIO30/TIMER2/TMCLK/SDA	E10	GND
C17	GPIO2/TIMER1/CHIP_ID2/$\overline{IRQ6}$	E11	V_{DD}

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7	U21	A12
T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	TBST	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	IRQ5/DP5/DACK4/EXT_BG3	V10	D10
T17	IRQ4/DP4/DACK3/EXT_DBG3	V11	D12
T18	IRQ1/DP1/DACK1/EXT_BG2	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

Table 1. MSC8113 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
W15	V_{DDH}	AA9	V_{DDH}
W16	HD33/D33/reserved	AA10	HD54/D54/ETHTX_EN
W17	V_{DDH}	AA11	HD52/D52
W18	HD32/D32/reserved	AA12	V_{DDH}
W19	GND	AA13	GND
W20	GND	AA14	V_{DDH}
W21	A7	AA15	HD46/D46/ETHTXT0
W22	A6	AA16	GND
Y2	HD7	AA17	HD42/D42/ETHRXD2/reserved
Y3	HD15	AA18	HD38/D38/reserved
Y4	V_{DDH}	AA19	HD35/D35/reserved
Y5	HD9	AA20	A0
Y6	V_{DD}	AA21	A2
Y7	HD60/D60/ETHCOL/reserved	AA22	A3
Y8	HD58/D58/ETHMDC	AB2	GND
Y9	GND	AB3	HD13
Y10	V_{DDH}	AB4	HD11
Y11	HD51/D51	AB5	HD8
Y12	GND	AB6	HD62/D62
Y13	V_{DDH}	AB7	HD61/D61
Y14	HD43/D43/ETHRXD3/reserved	AB8	HD57/D57/ETHRX_ER
Y15	GND	AB9	HD56/D56/ETHRX_DV/ETHCRS_DV
Y16	V_{DDH}	AB10	HD55/D55/ETHTX_ER/reserved
Y17	GND	AB11	HD53/D53
Y18	HD37/D37/reserved	AB12	HD50/D50
Y19	HD34/D34/reserved	AB13	HD49/D49/ETHTXD3/reserved
Y20	V_{DDH}	AB14	HD48/D48/ETHTXD2/reserved
Y21	A4	AB15	HD47/D47/ETHTXD1
Y22	A5	AB16	HD45/D45
AA2	V_{DD}	AB17	HD44/D44
AA3	HD14	AB18	HD41/D41/ETHRXD1
AA4	HD12	AB19	HD39/D39/reserved
AA5	HD10	AB20	HD36/D36/reserved
AA6	HD63/D63	AB21	A1
AA7	HD59/D59/ETHMDIO	AB22	V_{DD}
AA8	GND		

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8113 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8113.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core and PLL supply voltage	V_{DD}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	–0.2 to 4.0	V
Maximum operating temperature:	T_J	105	°C
Minimum operating temperature	T_J	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).

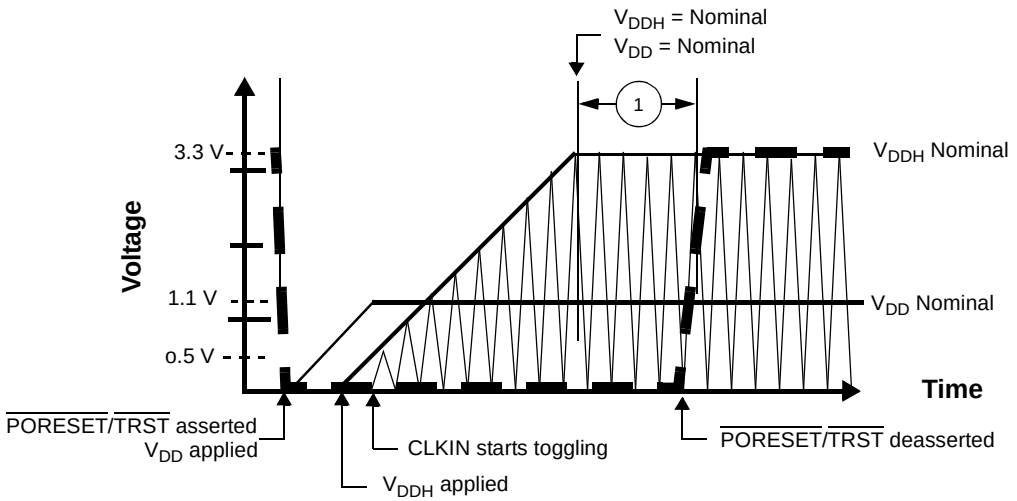


Figure 7. Start-Up Sequence: V_{DD} Raised Before V_{DDH} with CLKIN Started with V_{DDH}

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.

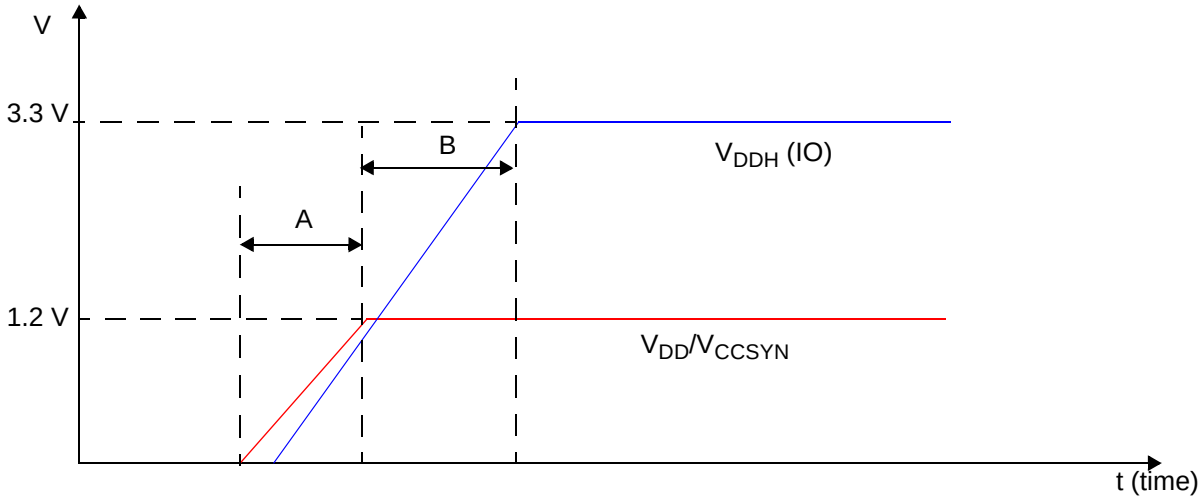


Figure 8. Power-Up Sequence for V_{DDH} and V_{DD}/V_{CCSYN}

The following rules apply:

1. During time interval A, V_{DDH} should always be equal to or less than the V_{DD}/V_{CCSYN} voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	300/400
Reference frequency (REFCLK)	100/133

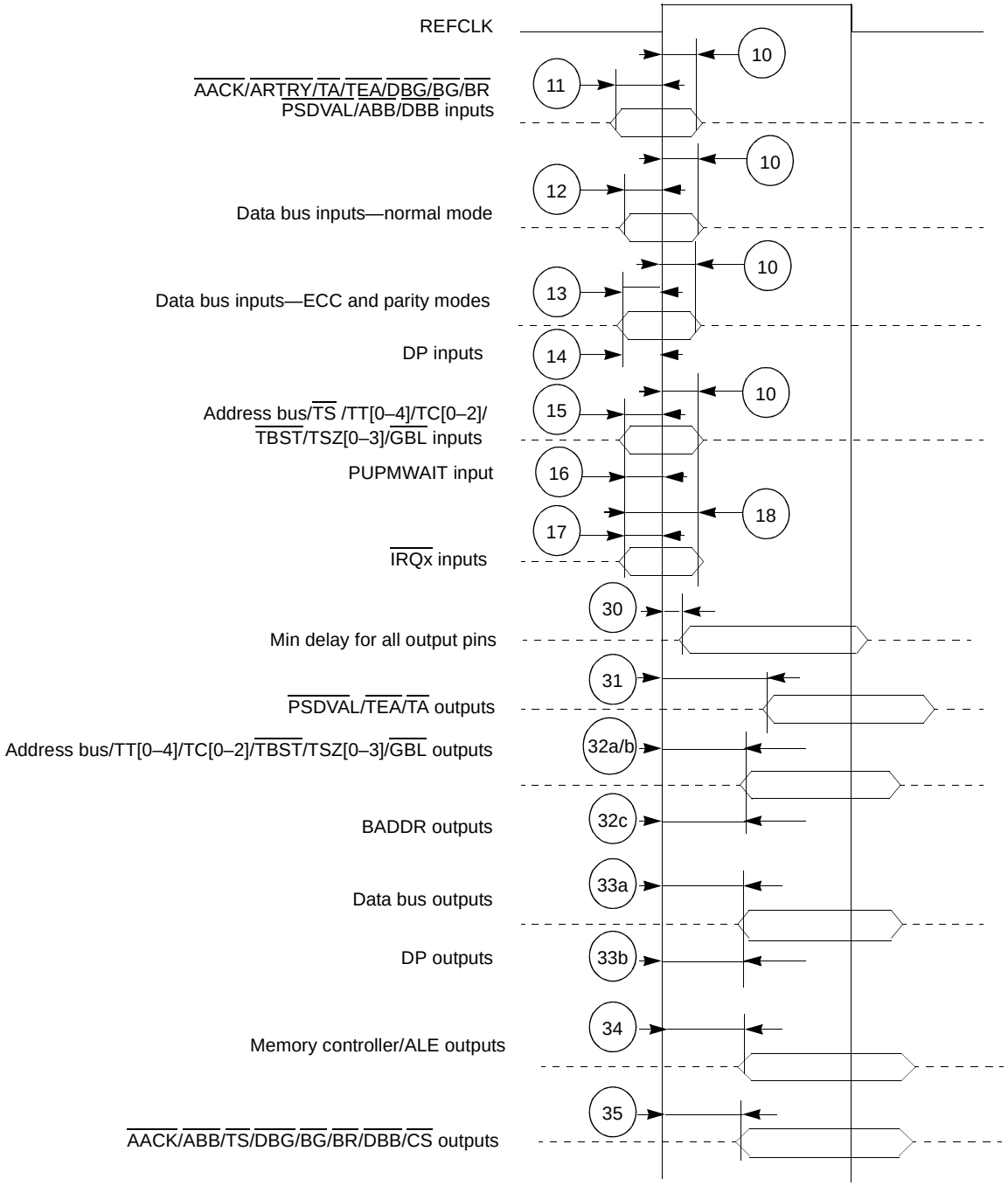
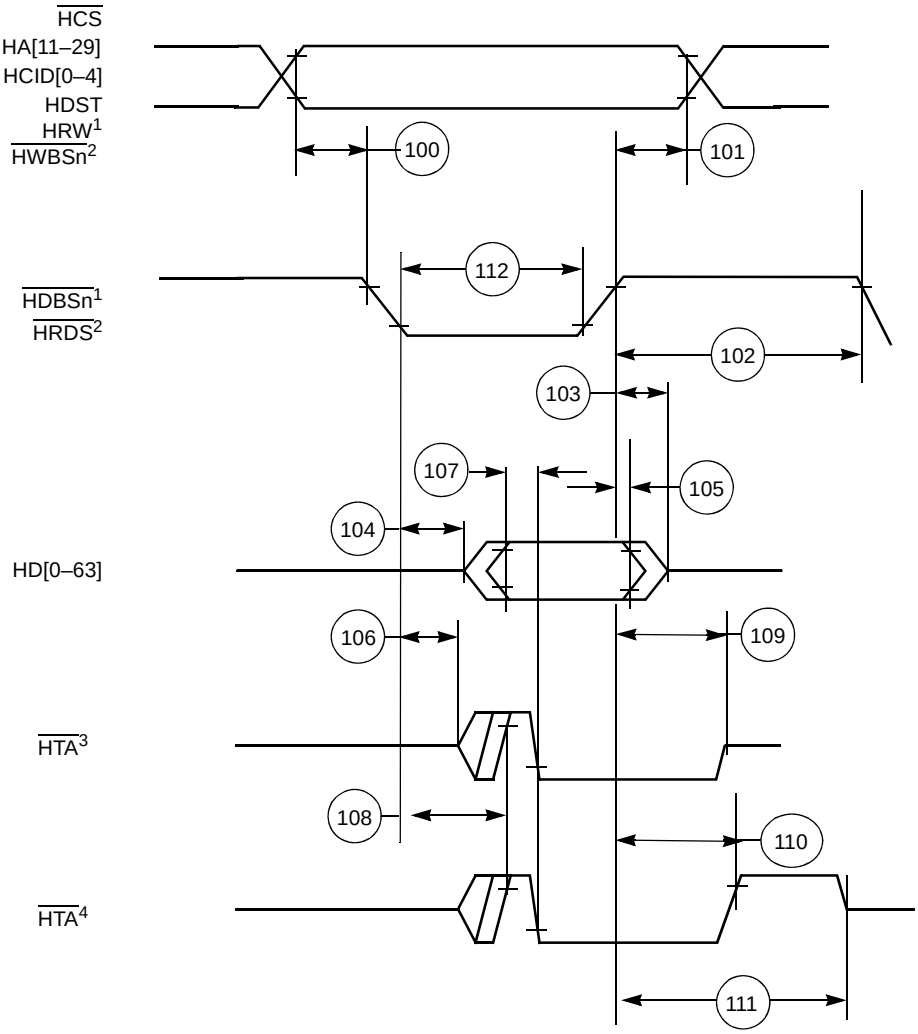


Figure 11. SIU Timing Diagram

Figure 14 shows DSI asynchronous read signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs in Synchronous Mode

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
120	HCLKIN cycle time[1,2]	HTC	10.0	55.6	ns
121	HCLKIN high pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
122	HCLKIN low pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.6	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

Table 20. DSI Outputs in Synchronous Mode

No.	Characteristic	1.1 V Core		Units
		Min	Max	
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	7.6	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	8.3	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.2	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	7.4	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	7.5	ns

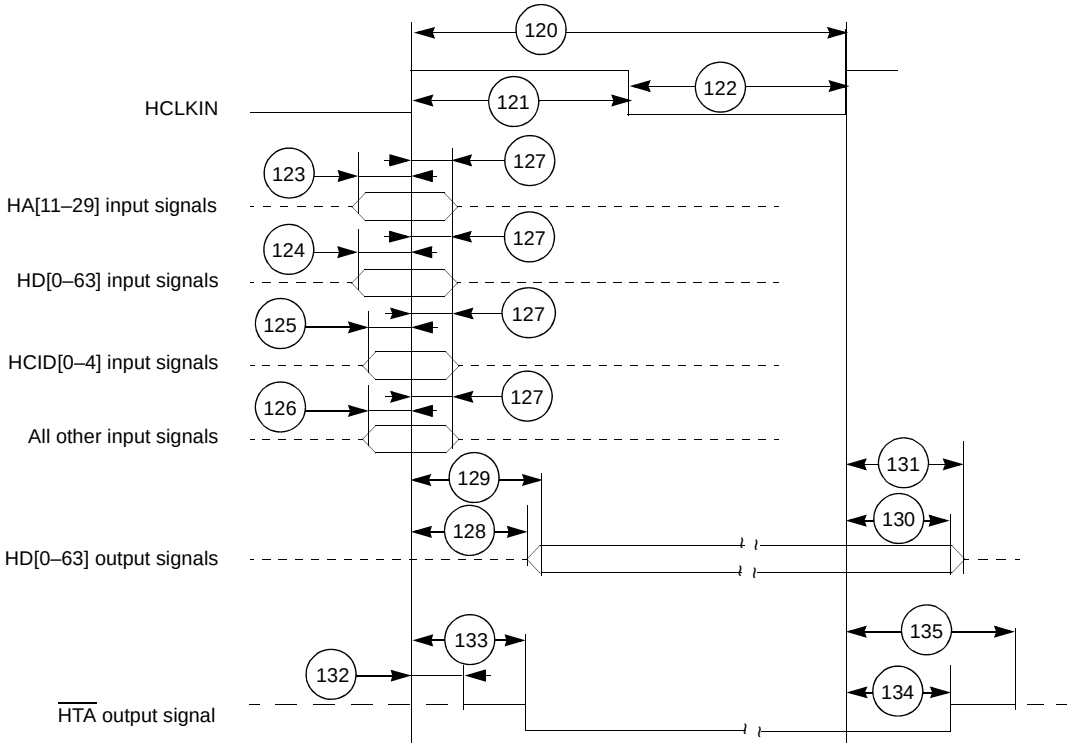


Figure 17. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 21. TDM Timing

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
300	TDMxRCLK/TDMxTCLK	TC[1]	16	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ± 0.1) × TC	7	—	ns
302	TDMxRCLK/TDMxTCLK low pulse width	(0.5 ± 0.1) × TC	7	—	ns
303	TDM receive all input set-up time		1.3	—	ns
304	TDM receive all input hold time		1.0	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		2.8	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output		—	10.0	ns
307	All output hold time[4]		2.5	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	10.7	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	9.7	ns
310	TDMxTSYN output hold time[4]		2.5	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz. Devices operating at 300 MHz are limited to a maximum TDMxRCLK/TDMxTCLK frequency of 50 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8113 Reference Manual* for details.
4. Values are based on 10 pF capacitive load.

2.5.10.2 MII Mode Timing

Table 25. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	14.6	ns

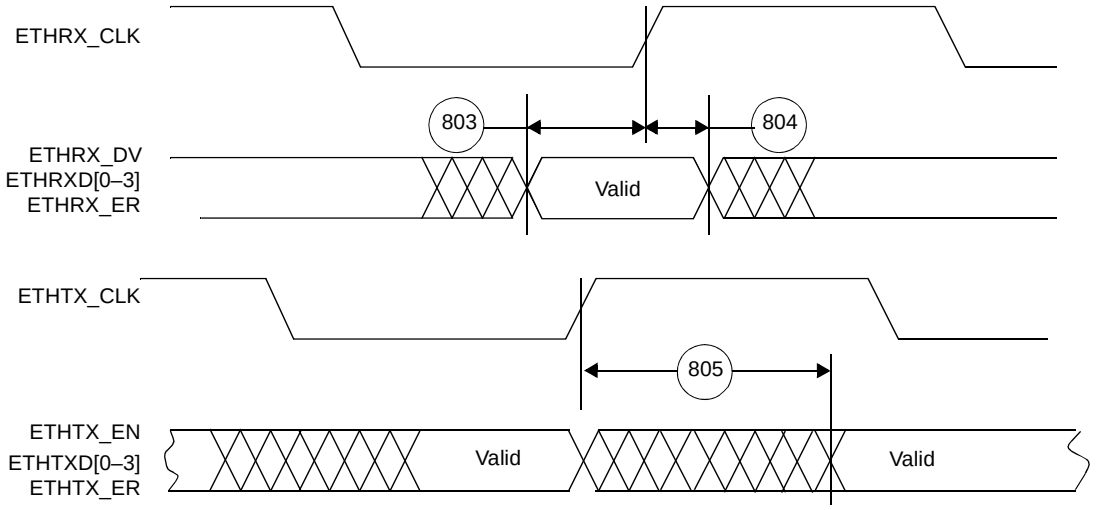


Figure 24. MII Mode Signal Timing

2.5.10.3 RMII Mode

Table 26. RMII Mode Signal Timing

No.	Characteristics	1.1 V Core		Unit
		Min	Max	
806	ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time	1.6	—	ns
807	ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time	1.6	—	ns
811	ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay.	3	12.5	ns

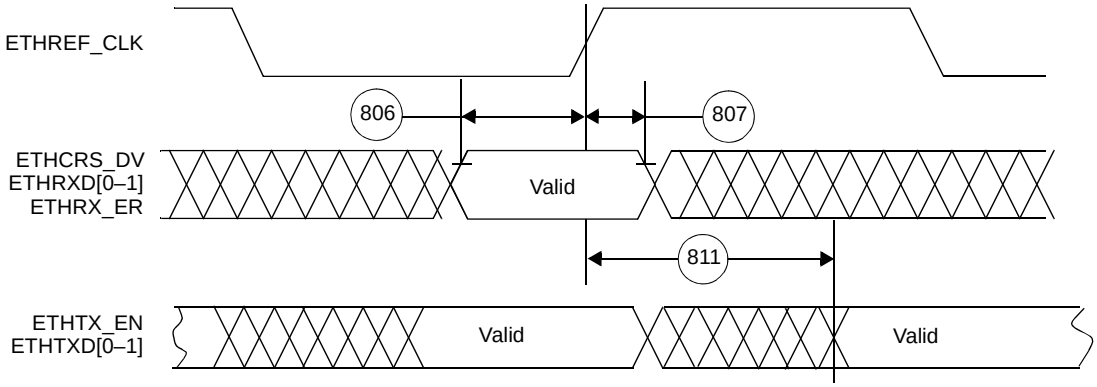


Figure 25. RMII Mode Signal Timing

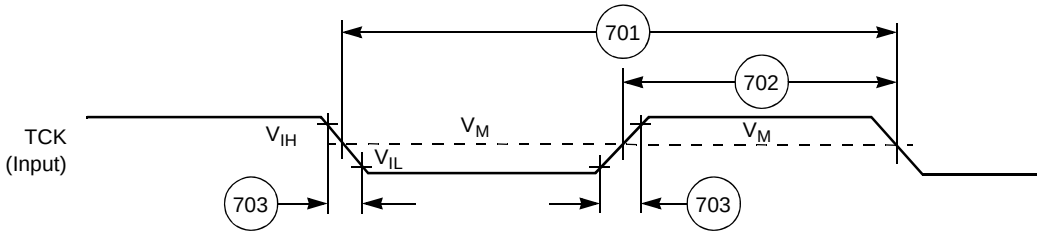


Figure 29. Test Clock Input Timing Diagram

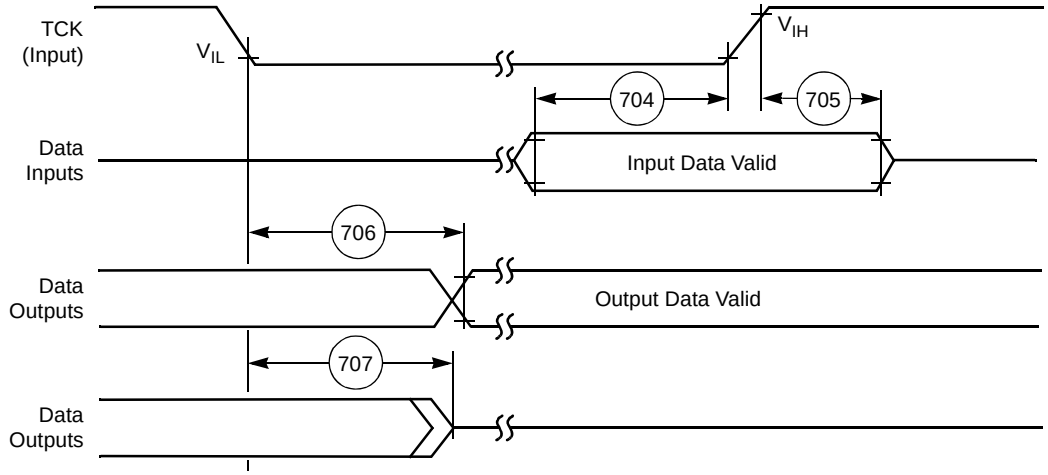


Figure 30. Boundary Scan (JTAG) Timing Diagram

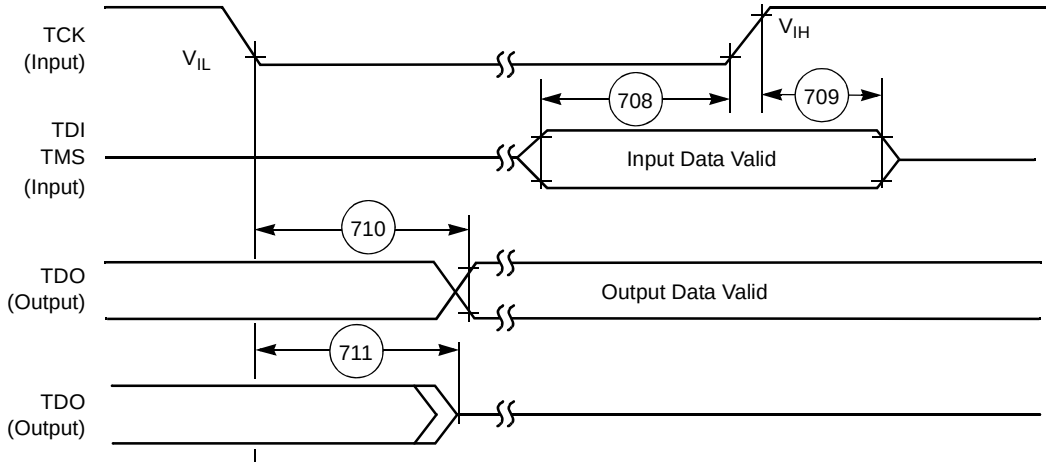


Figure 31. Test Access Port Timing Diagram

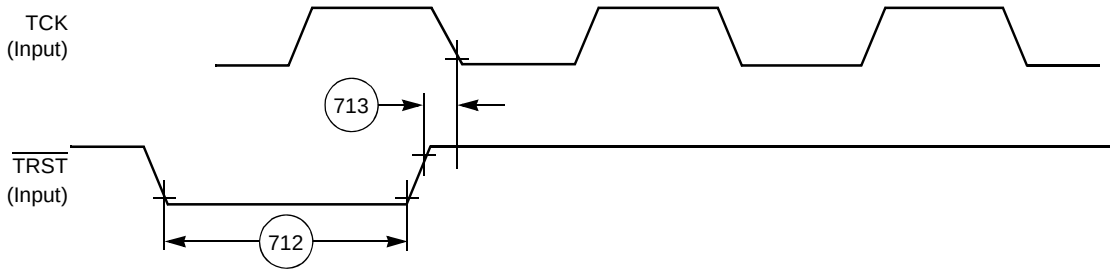


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

Each V_{CC} and V_{DD} pin on the MSC8113 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8113 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in **Figure 34**. For optimal noise filtering, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct. Provide an extremely low impedance path to the ground plane for GND_{SYN}. Bypass GND_{SYN} to V_{CCSYN} by a 0.01-µF capacitor located as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8113 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

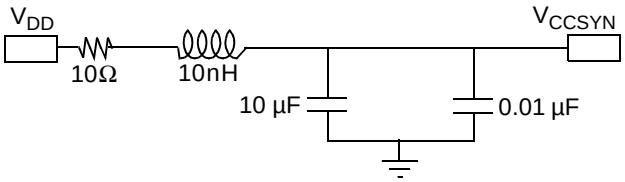


Figure 34. V_{CCSYN} Bypass

3.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to V_{DDH} or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, $\overline{\text{HTA}}$ should be pulled either up or down, depending on design requirements.
- $\overline{\text{HDST}}$ can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be pulled up.
- When the DSI is in asynchronous mode, $\overline{\text{HBRST}}$ and HCLKIN should either be disconnected or pulled up.
- The following signals must be pulled up: $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, and $\overline{\text{AACK}}$.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ can be left unconnected.
  - $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, and $\overline{\text{GBL}}$ can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - $\overline{\text{BR}}$ must be pulled up.
  - $\overline{\text{EXT\_BR[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.

3.5 Thermal Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8113 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8113 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D) \quad \textit{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

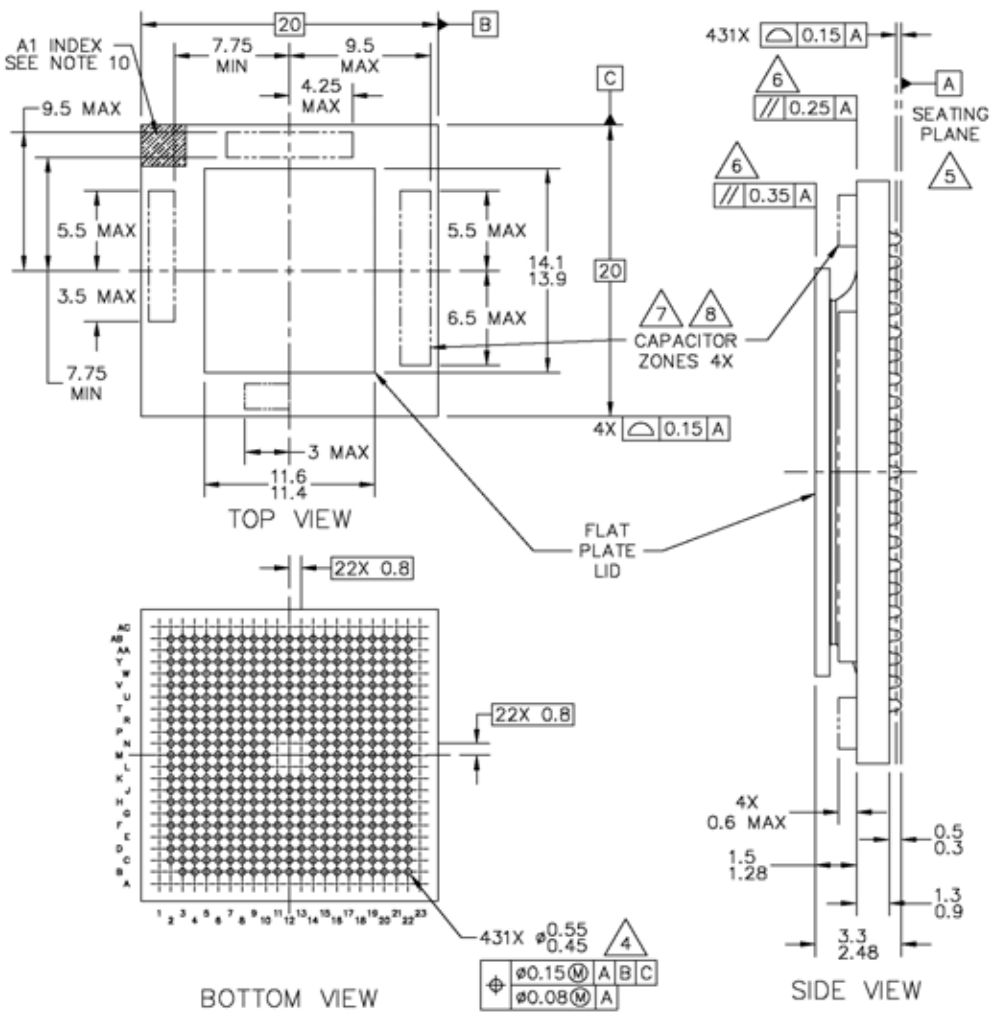
Note: See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number	
					Lead-Free	Lead-Bearing
MSC8113	Flip Chip Plastic Ball Grid Array (FC-PBGA)	1.1 V	–40° to 105°C	300	MSC8113TVT3600V	MSC8113TMP3600V
				400	MSC8113TVT4800V	MSC8113TMP4800V

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Features are symmetrical about the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to Datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.
7. Capacitors may not be present on all devices.
8. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
9. FC CBGA (Ceramic) package code: 5238.
   FC PBGA (Plastic) package code: 5263.
10. Pin 1 indicator can be in the form of number 1 marking or an "L" shape marking.

Figure 35. MSC8113 Mechanical Information, 431-pin FC-PBGA Package

6 Product Documentation

- *MSC8113 Technical Data Sheet* (MSC8113). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8113 device.
- *MSC8113 Reference Manual* (MSC8113RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8113 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.