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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

Product Status	Obsolete
Туре	SC140 Core
Interface	Ethernet, I²C, TDM, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8113tmp4800v

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. StarCore[®] SC140 DSP Extended Core Block Diagram

Des.	Signal Name	Des.	Signal Name
H21	V _{DDH}	K15	V _{DD}
H22	A31	K16	TT2/CS5
J2	HA18	K17	ALE
J3	HA26	K18	CS2
J4	V _{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V _{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V _{DDH}
J12	DBG	L6	V _{DDH}
J13	V _{DD}	L7	BADDR28
J14	GND	L8	IRQ5/BADDR29
J15	V _{DD}	L9	GND
J16	TT3/CS6	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	BCTL1/CS5	L15	V _{DDH}
J19	GPIO23/TDM0TDAT/IRQ13	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/IRQ15	L18	CS3
J22	A30	L19	V _{DDH}
K2	HA15	L20	A27
К3	HA21	L21	A25
K4	HA16	L22	A22
K5	PWE3/PSDDQM3/PBS3	M2	HD28
K6	PWE1/PSDDQM1/PBS1	M3	HD31
K7	POE/PSDRAS/PGPL2	M4	V _{DDH}
K8	IRQ2/BADDR30	M5	GND
К9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V _{DD}
K12	GND	M9	V _{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND



Des.	Signal Name	Des.	Signal Name
M15	V _{DDH}	P12	V _{CCSYN}
M16	HBRST	P13	GND
M17	V _{DDH}	P14	GND
M18	V _{DDH}	P15	TĀ
M19	GND	P16	BR
M20	V _{DDH}	P17	TEA
M21	A24	P18	PSDVAL
M22	A21	P19	DP0/DREQ1/EXT_BR2
N2	HD26	P20	V _{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	PWE2/PSDDQM2/PBS2	R3	V _{DDH}
N7	V _{DDH}	R4	GND
N8	HWBS0/HDBS0/HWBE0/HDBE0	R5	HD22
N9	HBCS	R6	HWBS6/HDBS6/HWBE6/HDBE6/PWE6/PSDDQM6/PBS6
N10	GND	R7	HWBS4/HDBS4/HWBE4/HDBE4/PWE4/PSDDQM4/PBS4
N14	GND	R8	TSZ1
N15	HRDS/HRW/HRDE	R9	TSZ3
N16	BG	R10	IRQ1/GBL
N17	HCS	R11	V _{DD}
N18	CSO	R12	V _{DD}
N19	PSDWE/PGPL1	R13	V _{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	IRQ7/DP7/DREQ4
N22	A20	R16	IRQ6/DP6/DREQ3
P2	HD20	R17	IRQ3/DP3/DREQ2/EXT_BR3
P3	HD27	R18	TS
P4	HD25	R19	IRQ2/DP2/DACK2/EXT_DBG2
P5	HD23	R20	A17
P6	HWBS3/HDBS3/HWBE3/HDBE3	R21	A18
P7	HWBS2/HDBS2/HWBE2/HDBE2	R22	A16
P8	HWBS1/HDBS1/HWBE1/HDBE1	T2	HD17
P9	HCLKIN	Т3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND _{SYN}	T5	HD0/SWTE



Des.	Signal Name	Des.	Signal Name
T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7	U21	A12
T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5	U22	A13
Т8	TSZ0	V2	HD3/MODCK1
Т9	TSZ2	V3	V _{DDH}
T10	TBST	V4	GND
T11	V _{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	IRQ5/DP5/DACK4/EXT_BG3	V10	D10
T17	IRQ4/DP4/DACK3/EXT_DBG3	V11	D12
T18	IRQ1/DP1/DACK1/EXT_BG2	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V _{DDH}
U14	D19	W8	V _{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V _{DDH}
U19	D31	W13	GND
U20	V _{DDH}	W14	HD40/D40/ETHRXD0



Des.	Signal Name	Des.	Signal Name
W15	V _{DDH}	AA9	V _{DDH}
W16	HD33/D33/reserved	AA10	HD54/D54/ETHTX_EN
W17	V _{DDH}	AA11	HD52/D52
W18	HD32/D32/reserved	AA12	V _{DDH}
W19	GND	AA13	GND
W20	GND	AA14	V _{DDH}
W21	A7	AA15	HD46/D46/ETHTXT0
W22	A6	AA16	GND
Y2	HD7	AA17	HD42/D42/ETHRXD2/reserved
Y3	HD15	AA18	HD38/D38/reserved
Y4	V _{DDH}	AA19	HD35/D35/reserved
Y5	HD9	AA20	A0
Y6	V _{DD}	AA21	A2
Y7	HD60/D60/ETHCOL/reserved	AA22	A3
Y8	HD58/D58/ETHMDC	AB2	GND
Y9	GND	AB3	HD13
Y10	V _{DDH}	AB4	HD11
Y11	HD51/D51	AB5	HD8
Y12	GND	AB6	HD62/D62
Y13	V _{DDH}	AB7	HD61/D61
Y14	HD43/D43/ETHRXD3/reserved	AB8	HD57/D57/ETHRX_ER
Y15	GND	AB9	HD56/D56/ETHRX_DV/ETHCRS_DV
Y16	V _{DDH}	AB10	HD55/D55/ETHTX_ER/reserved
Y17	GND	AB11	HD53/D53
Y18	HD37/D37/reserved	AB12	HD50/D50
Y19	HD34/D34/reserved	AB13	HD49/D49/ETHTXD3/reserved
Y20	V _{DDH}	AB14	HD48/D48/ETHTXD2/reserved
Y21	A4	AB15	HD47/D47/ETHTXD1
Y22	A5	AB16	HD45/D45
AA2	V _{DD}	AB17	HD44/D44
AA3	HD14	AB18	HD41/D41/ETHRXD1
AA4	HD12	AB19	HD39/D39/reserved
AA5	HD10	AB20	HD36/D36/reserved
AA6	HD63/D63	AB21	A1
AA7	HD59/D59/ETHMDIO	AB22	V _{DD}
AA8	GND		



rical Characteristics

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Rating	Symbol	Value	Unit
Core and PLL supply voltage:	V _{DD} V _{CCSYN}	1.07 to 1.13	V
I/O supply voltage	V _{DDH}	3.135 to 3.465	V
Input voltage	V _{IN}	–0.2 to V _{DDH} +0.2	V
Operating temperature range:	TJ	-40 to 105	°C

Table 3. Recommended Operating Conditions

2.3 Thermal Characteristics

 Table 4 describes thermal characteristics of the MSC8113 for the FC-PBGA packages.

Symbol		FC-PBGA 20 × 20 mm⁵	
Symbol	Natural Convection	200 ft/min (1 m/s) airflow	Unit
$R_{ extsf{ heta}JA}$	26	21	°C/W
$R_{ extsf{ heta}JA}$	19	15	°C/W
$R_{\theta JB}$	9		°C/W
R _{θJC}	0.9		°C/W
Ψ_{JT}	1		°C/W
 Notes: 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal. 3. Per JEDEC JESD51-6 with the board horizontal. 4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package. 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). 			
= 	$\frac{R_{\theta JA}}{R_{\theta JB}}$ $\frac{R_{\theta JB}}{\Psi_{JT}}$ $\frac{\Psi_{JT}}{\Psi_{JT}}$ $\frac{\Psi_{TT}}{\Psi_{TT}}$	Natural Convection $R_{\theta,JA}$ 26 $R_{\theta,JA}$ 19 $R_{\theta,JB}$ 9 $R_{\theta,JC}$ 0.9 Ψ_{JT} 1 -chip power dissipation, package thermal er dissipation of other components on the e single layer board horizontal. e top surface as measured by the cold plate e temperature difference between package	Natural Convection200 ft/min (1 m/s) airflow $R_{\theta,JA}$ 2621 $R_{\theta,JA}$ 1915 $R_{\theta,JB}$ 99 $R_{\theta,JC}$ 0.99 Ψ_{JT} 1-chip power dissipation, package thermal resistance, mounting si er dissipation of other components on the board, and board therme single layer board horizontal.e top surface as measured by the cold plate method (MIL SPEC-4)e temperature difference between package top and the junction t

Table 4. Thermal Characteristics for the MSC8113

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8113. The measurements in **Table 5** assume the following system conditions:

- $T_A = 25 \ ^{\circ}C$
- $V_{DD} = 1.1 \text{ V nominal} = 1.07 1.13 \text{ V}_{DC}$
- $V_{\text{DDH}} = 3.3 \text{ V} \pm 5\% \text{ V}_{DC}$
- GND = $0 V_{DC}$

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} .

rical Characteristics

Table 7.	Maximum	Frequencies
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Characteristic	Maximum in MHz
Internal bus frequency (BLCK)	100/133
 DSI clock frequency (HCLKIN) Core frequency = 300 MHz Core frequency = 400 MHz 	HCLKIN ≤ (min{70 MHz, CLKOUT}) HCLKIN ≤ (min{100 MHz, CLKOUT})
External clock frequency (CLKIN or CLKOUT)	100/133

Table 8. Clock Frequencies

	Cumbal	300 MHz Device		400 MHz Device		
Characteristics	Symbol F _{CLKIN} F _{BCLK} F _{REFCLK} F _{CLKOUT} F _{CORE}	Min	Мах	Min	Max	
CLKIN frequency	F _{CLKIN}	20	100	20	133.3	
BCLK frequency	F _{BCLK}	40	100	40	133.3	
Reference clock (REFCLK) frequency	F _{REFCLK}	40	100	40	133.3	
Output clock (CLKOUT) frequency	F _{CLKOUT}	40	100	40	133.3	
SC140 core clock frequency	F _{CORE}	200	300	200	400	
Note: The rise and fall time of external clocks shou	ld be 3 ns maximu	m				

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
Phase jitter between BCLK and CLKIN	CLK and CLKIN — 0.3		ns
CLKIN frequency	20	see Table 8	MHz
CLKIN slope	—	3	ns
PLL input clock (after predivider)	20	100	MHz
PLL output frequency (VCO output)	800		MHz
300 MHz core		1200	MHz
400 MHz core		1600	MHz
CLKOUT frequency jitter ¹	—	200	ps
CLKOUT phase jitter ¹ with CLKIN phase jitter of ±100 ps.	—	500	ps
Notes:1.Peak-to-peak.2.Not tested. Guaranteed by design.			

2.5.4 Reset Timing

The MSC8113 has several inputs to the reset logic:

- Power-on reset (PORESET)
- External hard reset (HRESET)
- External soft reset (SRESET)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8113 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.







2.5.6 DSI Timing

The timings in the following sections are based on a 20 pF capacitive load.

2.5.6.1 DSI Asynchronous Mode

Table 18. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Мах	Unit
100	Attributes ¹ set-up time before strobe (HWBS[n]) assertion	1.5	—	ns
101	Attributes ¹ hold time after data strobe deassertion	1.3	—	ns
102	Read/Write data strobe deassertion width:		—	
	— Consecutive access to the same DSI			ns
	— Different device with DCR[HTADT] = 01	5 + T _{REFCLK}		ns
	— Different device with DCR[HTADT] = 10	$5 + (1.5 \times T_{\text{REFCLK}})$		ns
	— Different device with DCR[HTADT] = 11	5 + ($2.5 \times T_{REFCLK}$)		ns
	• DCR[HTAAD] = 0	1.8 + T _{REFCLK}		ns
103	Read data strobe deassertion to output data high impedance	—	8.5	ns
104	Read data strobe assertion to output data active from high impedance	2.0	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to HTA active from high impedance	2.2	—	ns
107	Output data valid to HTA assertion	3.2	—	ns
108	Read/Write data strobe assertion to HTA valid ²	—	7.4	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	6.5	ns
111	Read/Write data strobe deassertion to output HTA high impedance. (DCR[HTAAD] = 1, HTA at end of access released at logic 1	_		
	 DCR[HTADT] = 01 		5 + T _{REFCLK}	ns
	 DCR[HTADT] = 10 		$5 + (1.5 \times T_{REFCLK})$	ns
	DCR[HTADT] = 11		5 + (2.5 × T _{REFCLK})	ns
112	Read/Write data strobe assertion width	1.8 + T _{REFCLK}	—	ns
201	Host data input set-up time before write data strobe deassertion	1.0	—	ns
202	Host data input hold time after write data strobe deassertion	1.7	—	ns
Notes:	 Attributes refers to the following signals: HCS, HA[11–29], HCID[0–4 This specification is tested in dual-strobe mode. Timing in single-stro All values listed in this table are tested or guaranteed by design. 	4], HDST, HRW, HRDS, bbe mode is guaranteed	and HWBSn. by design.	



Figure 14 shows DSI asynchronous read signals timing.



Notes: 1. Used for single-strobe mode access.

- **2.** Used for dual-strobe mode access.
- **3.** HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
- 4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram



Figure 15 shows DSI asynchronous write signals timing.



Notes: 1. Used for single-strobe mode access.

- 2. Used for dual-strobe mode access.
- 3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
- 4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 15. Asynchronous Single- and Dual-Strobe Modes Write Timing Diagram

Figure 16 shows DSI asynchronous broadcast write signals timing.



Figure 16. Asynchronous Broadcast Write Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs in Synchronous Mo
--

No	Characteristic	Expression	1.1 V	Unite	
NO.	Characteristic	Expression	Min	Max	
120	HCLKIN cycle time ^{1,2}	HTC	10.0	55.6	ns
121	HCLKIN high pulse width	$(0.5\pm0.1) imes$ HTC	4.0	33.3	ns
122	HCLKIN low pulse width	$(0.5\pm0.1) imes$ HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	_	ns
124	HD[0–63] inputs set-up time	—	0.6	_	ns
125	HCID[0-4] inputs set-up time	—	1.3	_	ns
126	All other inputs set-up time	—	1.2	_	ns
127	All inputs hold time	—	1.5	_	ns
Notes:	 Values are based on a frequency range of 18–100 MHz. Refer to Table 7 for HCLKIN frequency limits. 				

Table 20. DSI Outputs in Synchronous Mode

No	Characteristic		1.1 V Core		
NO.	Characteristic	Min	Max	Units	
128	HCLKIN high to HD[0–63] output active	2.0	—	ns	
129	HCLKIN high to HD[0–63] output valid	—	7.6	ns	
130	HD[0–63] output hold time	1.7	—	ns	
131	HCLKIN high to HD[0–63] output high impedance	—	8.3	ns	
132	HCLKIN high to HTA output active	2.2	—	ns	
133	HCLKIN high to HTA output valid	—	7.4	ns	
134	HTA output hold time	1.7	—	ns	
135	HCLKIN high to HTA high impedance	_	7.5	ns	

Electrical Characteristics







2.5.8 UART Timing

No.	Characteristics	Expression	Min	Max	Un it
400	URXD and UTXD inputs high/low duration	$16 imes T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns





Figure 20. UART Input Timing



Figure 21. UART Output Timing

2.5.9 Timer Timing

Table 23. Timer Timing

No.	Characteristics		Ref = CLKIN		
	Characteristics	Min	Max	Unit	
500	TIMERx frequency	10.0	—	ns	
501	TIMERx Input high period	4.0	_	ns	
502	TIMERx Output low period	4.0	_	ns	
503	TIMERx Propagations delay from its clock input	3.1	9.5	ns	







2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10		ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns



Figure 23. MDIO Timing Relationship to MDC



2.5.10.2 MII Mode Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	14.6	ns







2.5.10.3 RMII Mode

Table	26.	RMII	Mode	Signal	Timing
-------	-----	------	------	--------	--------

No	Characteristics	1.1 V Core		Unit	
NO.			Max	Onic	
806	ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time	1.6	—	ns	
807	ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time	1.6	—	ns	
811	ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay.	3	12.5	ns	



Figure 25. RMII Mode Signal Timing



2.5.10.4 SMII Mode

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	_	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	1.5 ¹	6.0 ²	ns
Notes:	 Measured using a 5 pF load. Measured using a 15 pF load. 			





Figure 26. SMII Mode Signal Timing

2.5.11 GPIO Timing

Table 28. GPIO Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	Onit
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	6.1	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.1	_	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	3.5	_	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	_	ns



Figure 27. GPIO Timing



Figure 29. Test Clock Input Timing Diagram







Figure 32. TRST Timing Diagram





5 Package Information



Notes: 1. All dimensions in millimeters.

- 2. Dimonsioning and tolorancing
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Features are symmetrical about the package center lines unless dimensioned otherwise.
- Maximum solder ball diameter measured parallel to Datum A.

Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Parallelism measurement shall exclude any effect of mark on top surface of package.

Capacitors may not be present on all devices.

Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.

FC CBGA (Ceramic) package code: 5238. FC PBGA (Plastic) package code: 5263.

10.Pin 1 indicator can be in the form of number 1 marking or an "L" shape marking.

Figure 35. MSC8113 Mechanical Information, 431-pin FC-PBGA Package

6 **Product Documentation**

- *MSC8113 Technical Data Sheet* (MSC8113). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8113 device.
- *MSC8113 Reference Manual* (MSC8113RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- Application Notes. Cover various programming topics related to the StarCore DSP core and the MSC8113 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.

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