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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071czt7

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3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L071xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

Stop mode with RTC

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L071xx embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4 Reset and supply management

3.4.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the

3.14 Timers and watchdogs

The ultra-low-power STM32L071xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

[Table 9](#) compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.14.1 General-purpose timers (TIM2, TIM3, TIM21 and TIM22)

There are four synchronizable general-purpose timers embedded in the STM32L071xx device (see [Table 9](#) for differences).

TIM2, TIM3

TIM2 and TIM3 are based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2/TIM3 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2/TIM3 have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2/TIM3, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

	1	2	3	4	5	6	7
A	VDD IO2	PA15	PB3	PB5	BOOT0	PB9	VDD
B	PA12	PA14	PB4	PB6	PB8	VDD	PC13
C	PA10	PA13	PB7	PC1	PC0	PC14 OSC32 _IN	PC15 OSC32 _OUT
D	PA8	PA11	PB1	VSS	NRST	PH0 OSC_IN	PH1 OSC_OUT
E	PB15	PA9	PB2	PA1	PA0	VREF+	PC2
F	PB14	PE13	PB11	PA7	PA4	PA2	VDDA
G	PB12	VDD	PB10	PB0	PA6	PA5	PA3

1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.



Table 18. Alternate functions port C

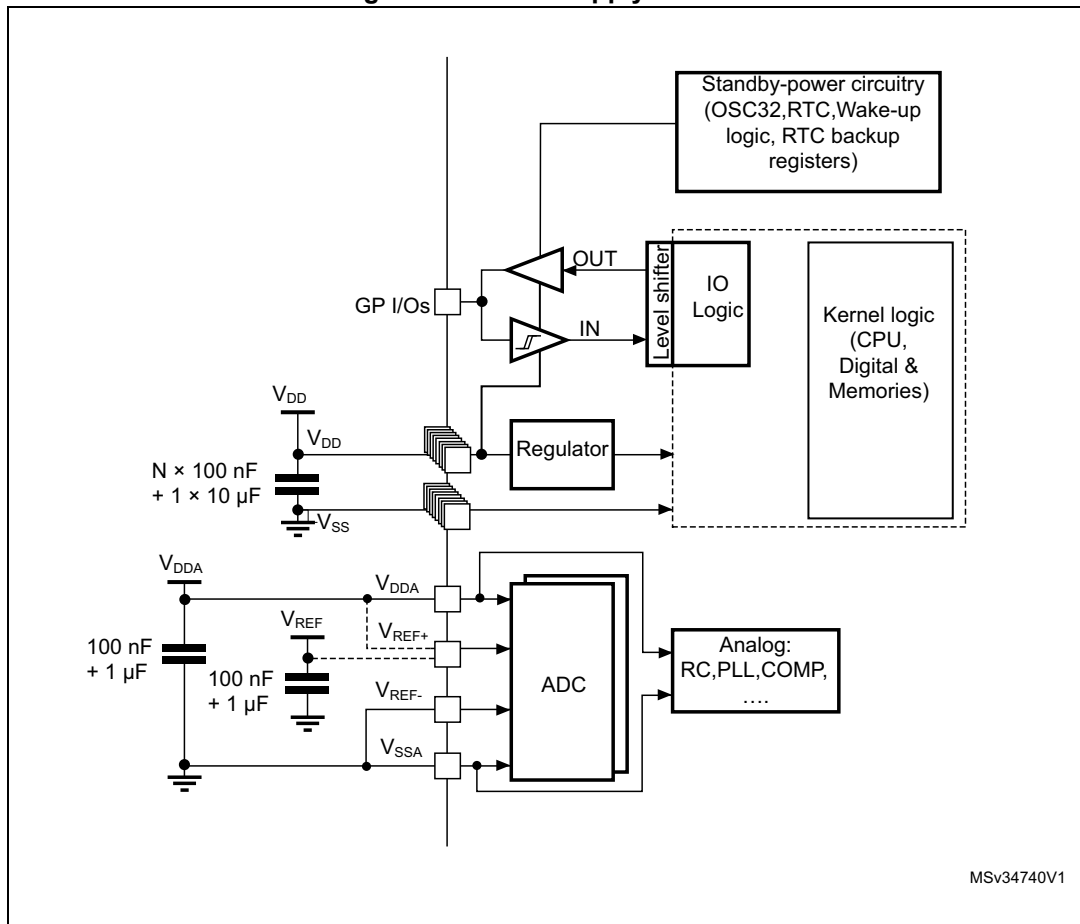
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port C	PC0	LPTIM1_IN1		EVENTOUT				LPUART1_RX	I2C3_SCL
	PC1	LPTIM1_OUT		EVENTOUT				LPUART1_TX	I2C3_SDA
	PC2	LPTIM1_IN2		SPI2_MISO/ I2S2_MCK					
	PC3	LPTIM1_ETR		SPI2_MOSI/ I2S2_SD					
	PC4	EVENTOUT		LPUART1_TX					
	PC5			LPUART1_RX					
	PC6	TIM22_CH1		TIM3_CH1					
	PC7	TIM22_CH2		TIM3_CH2					
	PC8	TIM22_ETR		TIM3_CH3					
	PC9	TIM21_ETR		TIM3_CH4					I2C3_SDA
	PC10	LPUART1_TX						USART4_TX	
	PC11	LPUART1_RX						USART4_RX	
	PC12			USART5_TX				USART4_CK	
	PC13								
	PC14								
	PC15								

Table 21. Alternate functions port H

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/ I2S2/USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2 /I2C1/TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3/ EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/ LPUART1/ COMP1/2/ TIM3
Port H	PH0		-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH9	-	-	-	-	-	-	-	-
	PH10	-	-	-	-	-	-	-	-

6.1.6 Power supply scheme

Figure 14. Power supply scheme



6.1.7 Current consumption measurement

Figure 15. Current consumption measurement scheme

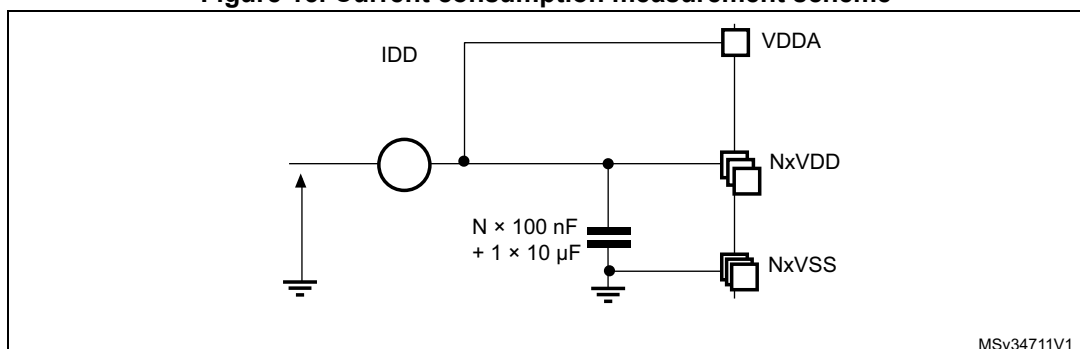


Table 25. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T _A	Temperature range	Maximum power dissipation (range 6)	−40	85	°C
		Maximum power dissipation (range 7)	−40	105	
		Maximum power dissipation (range 3)	−40	125	
T _J	Junction temperature range (range 6)	$-40\text{ °C} \leq T_A \leq 85\text{ °}$	−40	105	
	Junction temperature range (range 7)	$-40\text{ °C} \leq T_A \leq 105\text{ °C}$	−40	125	
	Junction temperature range (range 3)	$-40\text{ °C} \leq T_A \leq 125\text{ °C}$	−40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see [Table 24: Thermal characteristics on page 56](#)).

Table 31. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Condition		f _{HCLK} (MHz)	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from RAM)	Supply current in Run mode code executed from RAM, Flash memory switched off	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range3, V _{core} =1.2 V VOS[1:0]=11	1	175	230	μA
				2	315	360	
				4	570	630	
			Range2, V _{core} =1.5 V VOS[1:0]=10	4	0,71	0,78	mA
				8	1,35	1,6	
				16	2,7	3	
			Range1, V _{core} =1.8 V VOS[1:0]=01	8	1,7	1,9	
				16	3,2	3,7	
				32	6,65	7,1	
		MSI clock	Range3, V _{core} =1.2 V VOS[1:0]=11	0,065	38	98	μA
				0,524	105	160	
				4,2	615	710	
		HSI clock source (16 MHz)	Range2, V _{core} =1.5 V VOS[1:0]=10	16	2,85	3	mA
			Range1, V _{core} =1.8 V VOS[1:0]=01	32	6,85	7,3	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

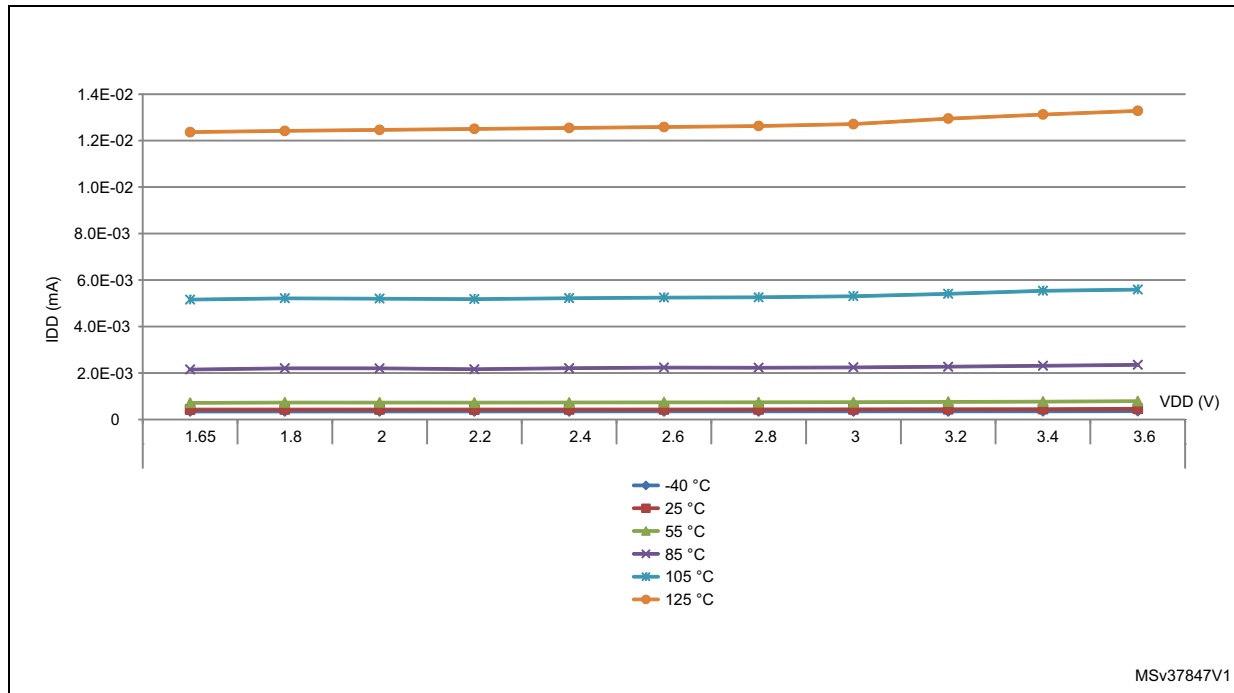
Table 32. Current consumption in Run mode vs code type, code with data processing running from RAM⁽¹⁾

Symbol	Parameter	Conditions			f _{HCLK}	Typ	Unit
I _{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash memory switched off	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL on) ⁽²⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	570	μA
				CoreMark		670	
				Fibonacci		410	
				while(1)		375	
		Range 1, V _{CORE} =1.8 V, VOS[1:0]=01		Dhrystone	32 MHz	6,65	mA
				CoreMark		6,95	
				Fibonacci		5,9	
				while(1)		5,2	

1. Guaranteed by characterization results, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Figure 20. I_{DD} vs V_{DD} , at $T_A = 25/55/85/105/125\text{ }^{\circ}\text{C}$, Stop mode with RTC disabled, all clocks off



MSv37847V1

Table 37. Typical and maximum current consumptions in Standby mode

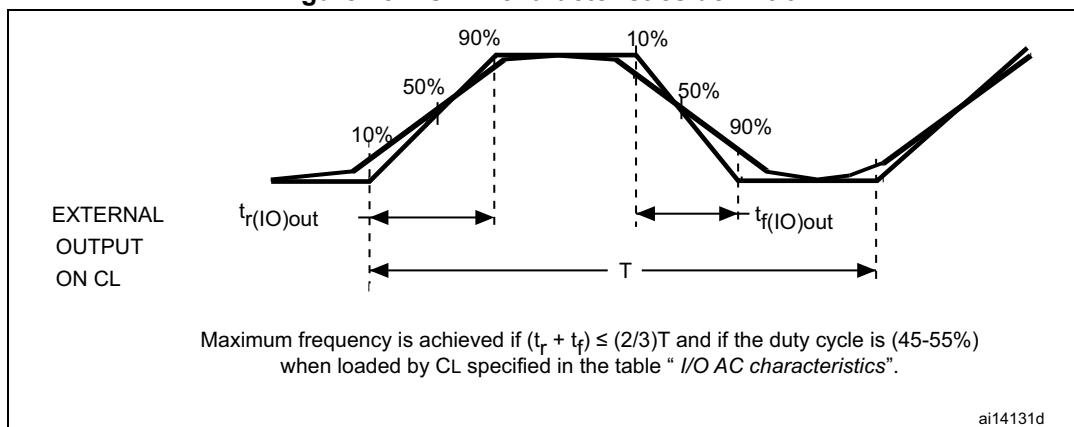
Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
I_{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	$T_A = -40\text{ to }25\text{ }^{\circ}\text{C}$	0,855	1,70	μA
			$T_A = 55\text{ }^{\circ}\text{C}$	-	2,90	
			$T_A = 85\text{ }^{\circ}\text{C}$	-	3,30	
			$T_A = 105\text{ }^{\circ}\text{C}$	-	4,10	
			$T_A = 125\text{ }^{\circ}\text{C}$	-	8,50	
		Independent watchdog and LSI off	$T_A = -40\text{ to }25\text{ }^{\circ}\text{C}$	0,29	0,60	
			$T_A = 55\text{ }^{\circ}\text{C}$	0,32	1,20	
			$T_A = 85\text{ }^{\circ}\text{C}$	0,5	2,30	
			$T_A = 105\text{ }^{\circ}\text{C}$	0,94	3,00	
			$T_A = 125\text{ }^{\circ}\text{C}$	2,6	7,00	

1. Guaranteed by characterization results at $125\text{ }^{\circ}\text{C}$, unless otherwise specified

Table 41. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	5.0	8	μs
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	7.3	13	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	13	23	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	28	38	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	51	65	
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	100	120	
		$f_{HCLK} = f_{MSI} = 65 \text{ kHz}$	190	260	
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	7.9	10	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	65	130	ms
	Wakeup from Standby mode FWU bit = 0	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	2.2	3	

Figure 28. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see [Table 61](#)).

Unless otherwise specified, the parameters given in [Table 61](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 25](#).

Table 61. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}^{(1)}$	NRST output low level voltage	$I_{OL} = 2 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	-	-	0.4	
		$I_{OL} = 1.5 \text{ mA}$ $1.65 \text{ V} < V_{DD} < 2.7 \text{ V}$	-	-		
$V_{hys(NRST)}^{(1)}$	NRST Schmitt trigger voltage hysteresis	-	-	$10\%V_{DD}^{(2)}$	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽³⁾	$V_{IN} = V_{SS}$	30	45	60	kΩ
$V_{F(NRST)}^{(1)}$	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}^{(1)}$	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.

2. 200 mV minimum value

3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline

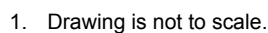
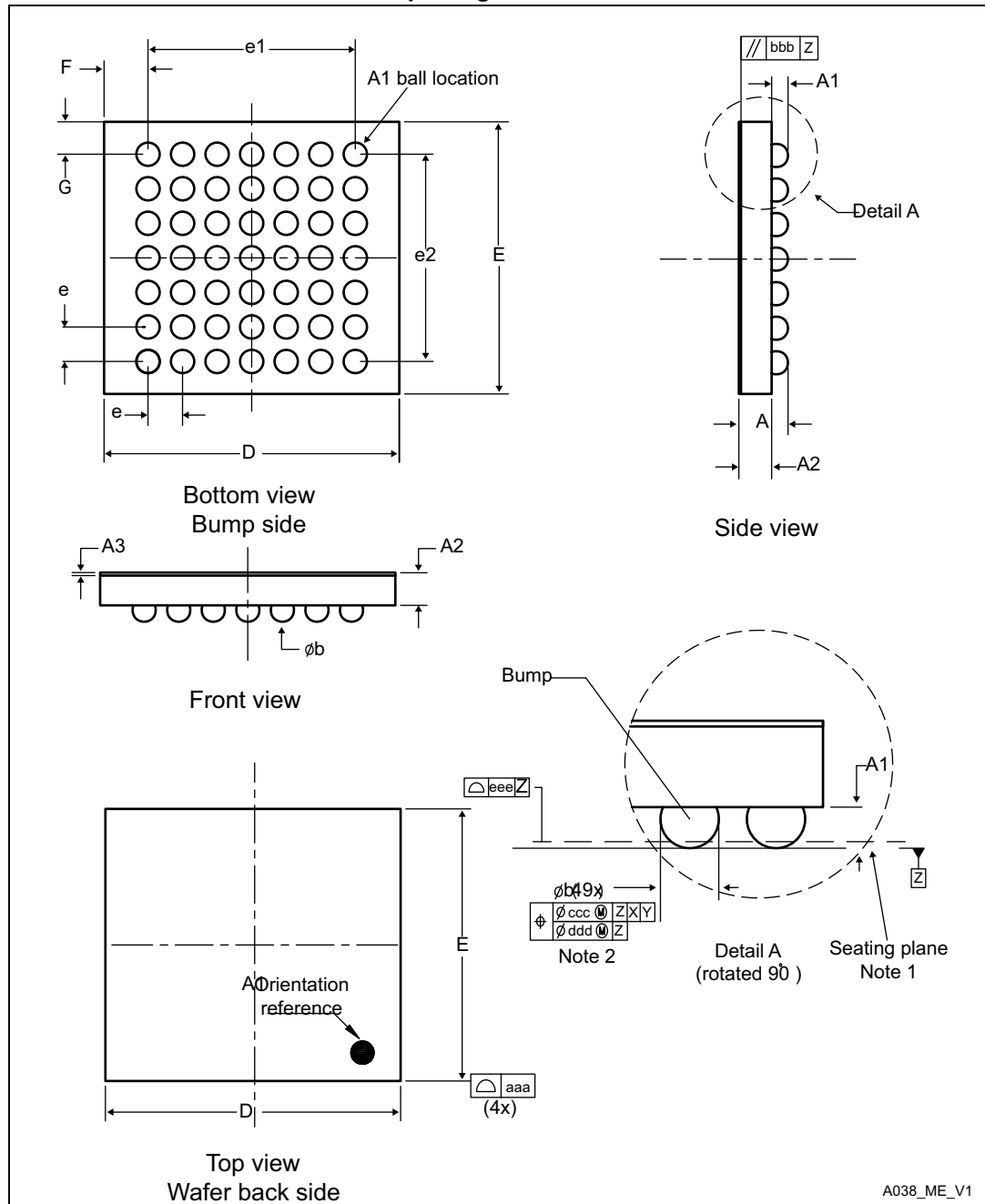


Table 77. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

7.5 WLCSP49 package information

Figure 50. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale package outline

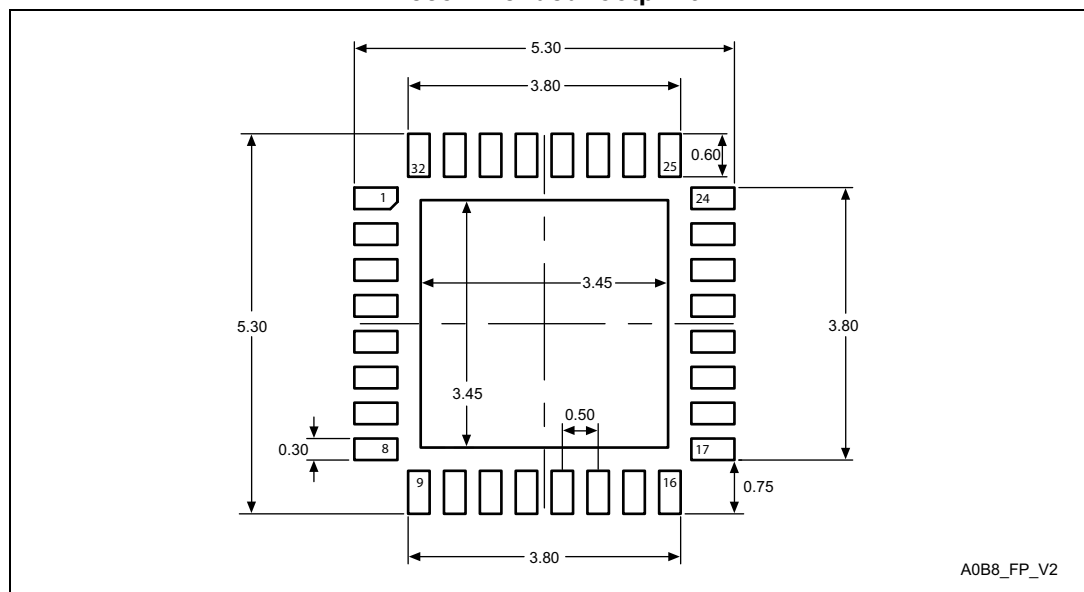


1. Drawing is not to scale.

Table 86. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 60. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint

1. Dimensions are expressed in millimeters.

7.9 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 87. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	36	°C/W
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	54	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	48	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	64	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm / 0.5 mm pitch	57	

8 Part numbering

Table 88. STM32L071xx ordering information scheme

Example:	STM32	L	071	R	8	T	6	D	TR									
Device family																		
STM32 = ARM-based 32-bit microcontroller																		
Product type																		
L = Low power																		
Device subfamily																		
071 = Access line																		
Pin count																		
K = 32 pins																		
C = 48/49 pins																		
R = 64 pins																		
V = 100 pins																		
Flash memory size																		
8 = 64 Kbytes																		
B = 128 Kbytes																		
Z = 192 Kbytes																		
Package																		
T = LQFP																		
H = TFBGA																		
I = UFBGA																		
U = UFQFPN																		
Y = WLCSP pins																		
Temperature range																		
6 = Industrial temperature range, −40 to 85 °C																		
7 = Industrial temperature range, −40 to 105 °C																		
3 = Industrial temperature range, −40 to 125 °C																		
Options																		
No character = V _{DD} range: 1.8 to 3.6 V and BOR enabled																		
D = V _{DD} range: 1.65 to 3.6 V and BOR disabled																		
Packing																		
TR = tape and reel																		
No character = tray or tube																		

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.