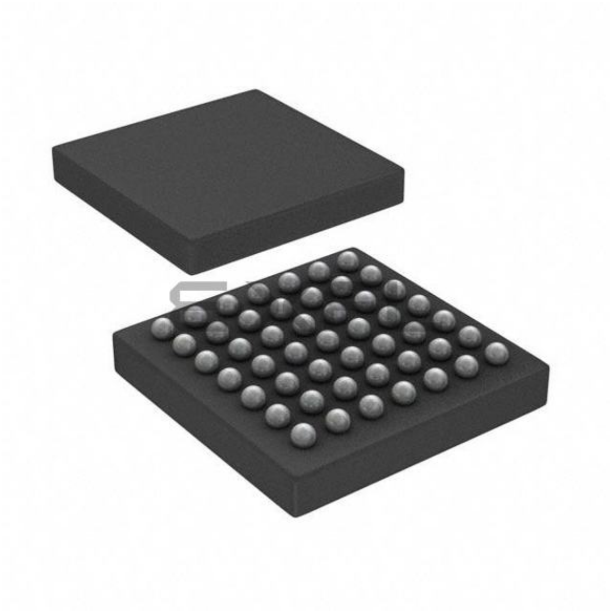


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.29x3.26)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071czy6tr

2.1 Device overview

Table 2. Ultra-low-power STM32L071xx device features and peripheral counts

Peripheral		STM32L 071K8	STM32L 071C8	STM32L 071V8	STM32L 071KB	STM32L 071CB	STM32L 071VB	STM32L 071RB	STM32L 071KZ	STM32L 071CZ	STM32L 071VZ	STM32L 071RZ
Flash (Kbytes)		64 Kbytes			128 Kbytes				192 Kbytes			
Data EEPROM (Kbytes)		3 Kbytes			6 Kbytes							
RAM (Kbytes)		20 Kbytes										
Timers	**General-purpose**	4										
	Basic	2										
	LPTIMER	1										
RTC/SYSTICK/IWDG /WWDG		1/1/1/1										
Com. interfaces	**SPI/I2S**	4(3)(1)/0	6(4)(2)/1		4(3)(1)/0	6(4)(2)/1			4(3)(1)/0	6(4)(2)/1		
	I^{2}C	2	3		2	3			2	3		
	USART	3	4		3	4			3	4		
	LPUART	1										
GPIOs		23	37	84	25(3)	40(4)	84	51(5)	25(3)	40(4)	84	51(5)
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1										
12-bit synchronized ADC Number of channels		1 10	1 13	1 16	1 10	1 13(4)	1 16	1 16(5)	1 10	1 13(4)	1 16	1 16(5)
Comparators		2										
Max. CPU frequency		32 MHz										
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option										
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C										
Packages		UFQFPN 32	LQFP48	LQFP/ UFBGA 100	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64

1. 3 SPI interfaces are USARTs operating in SPI master mode.
2. 4 SPI interfaces are USARTs operating in SPI master mode.
3. UFQFPN32 has 2 GPIOs less than LQFP32.
4. LQFP48 has three GPIOs less than WLCSP49.
5. TFBGA64 has one GPIO, one ADC input less than LQFP64.

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(3)		--	

Table 6. STM32L0xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L071xx are compatible with all ARM tools and software.

Figure 2. Clock tree

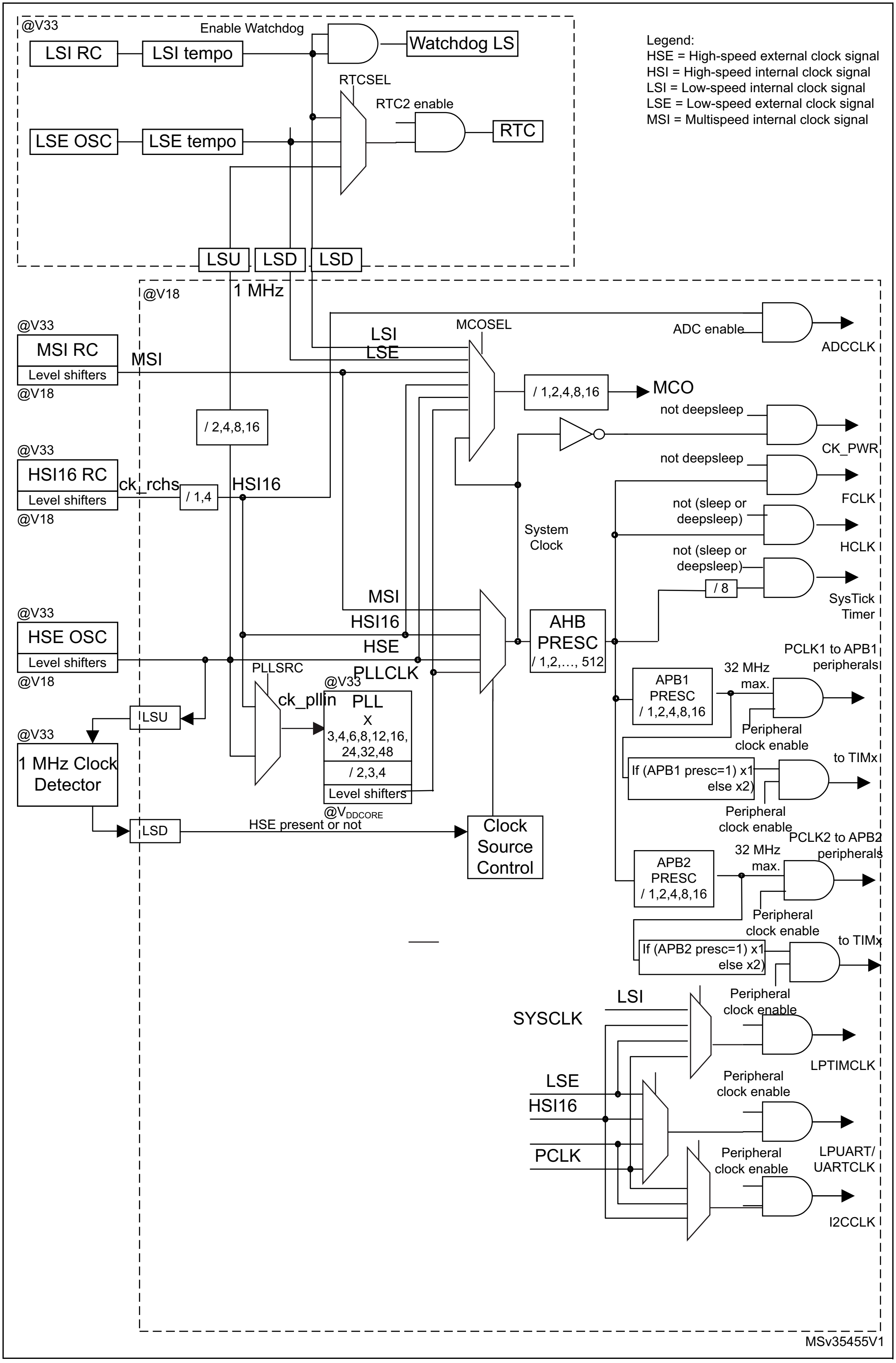
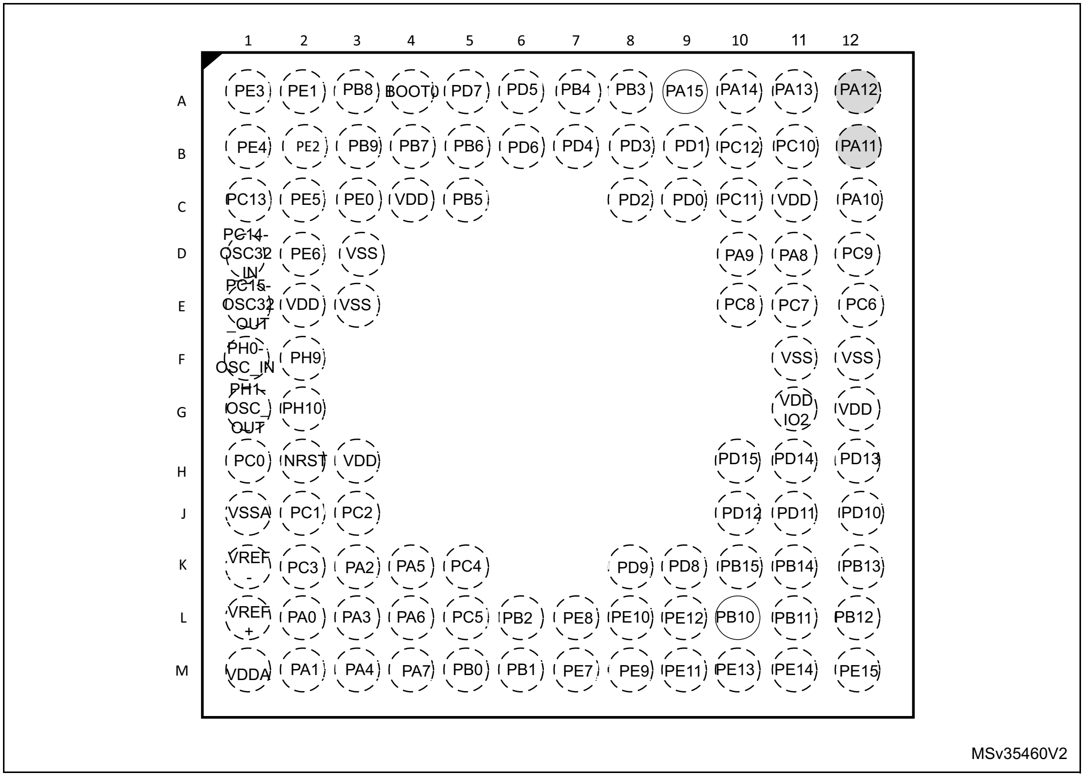
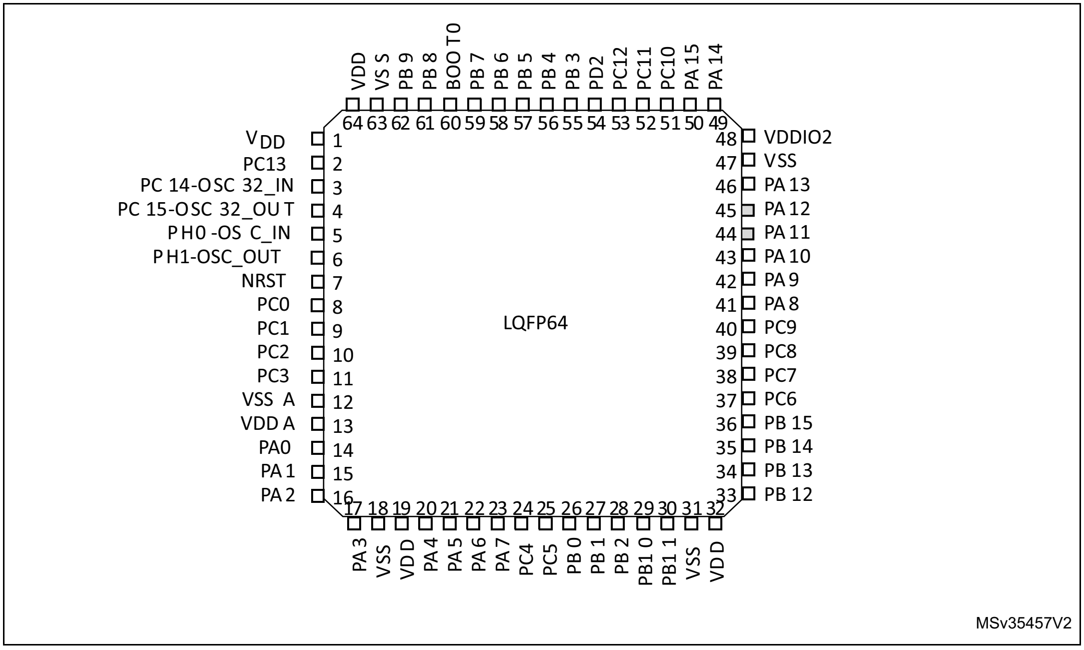


Figure 4. STM32L071xx UFBGA100 ballout - 7x 7 mm



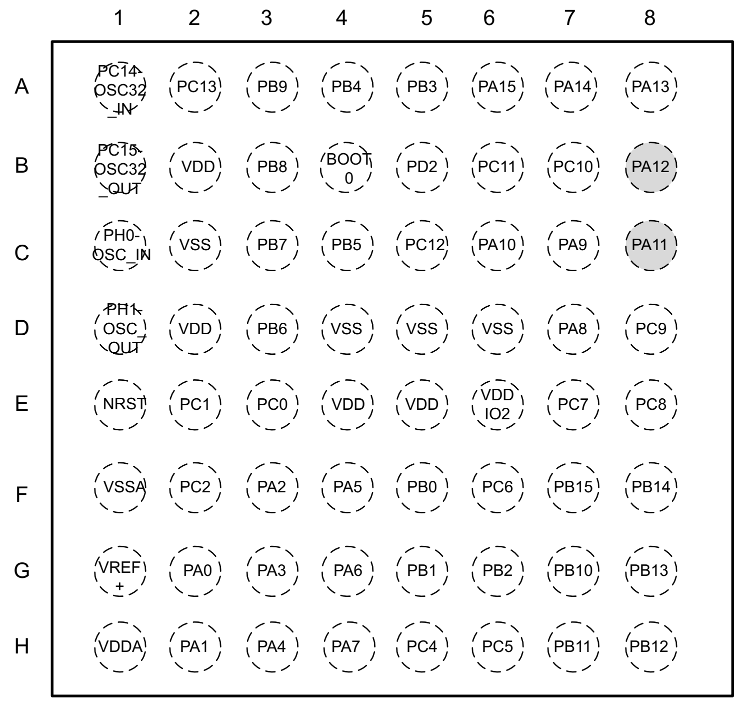
1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Figure 5. STM32L071xx LQFP64 pinout - 10 x 10 mm



1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Figure 6. STM32L071xx TFBGA64 ballout - 5x 5 mm



	1	2	3	4	5	6	7	8
A	PC14-OSC32_IN	PC13	PB9	PB4	PB3	PA15	PA14	PA13
B	PC15-OSC32_OUT	VDD	PB8	BOOT0	PD2	PC11	PC10	PA12
C	PH0-OSC_IN	VSS	PB7	PB5	PC12	PA10	PA9	PA11
D	PH1-OSC_OUT	VDD	PB6	VSS	VSS	VSS	PA8	PC9
E	NRST	PC1	PC0	VDD	VDD	VDDIO2	PC7	PC8
F	VSSA	PC2	PA2	PA5	PB0	PC6	PB15	PB14
G	VREF+	PA0	PA3	PA6	PB1	PB2	PB10	PB13
H	VDDA	PA1	PA4	PA7	PC4	PC5	PB11	PB12

MSv35458V2

1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Table 15. STM32L071xxx pin definition

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	1	B2	PE2	I/O	FT	-	TIM3_ETR	-
-	-	-	-	-	-	2	A1	PE3	I/O	FT	-	TIM22_CH1, TIM3_CH1	-
-	-	-	-	-	-	3	B1	PE4	I/O	FT	-	TIM22_CH2, TIM3_CH2	-
-	-	-	-	-	-	4	C2	PE5	I/O	FT	-	TIM21_CH1, TIM3_CH3	-
-	-	-	-	-	-	5	D2	PE6	I/O	FT	-	TIM21_CH2, TIM3_CH4	RTC_TAMP3/WKUP3
1	-	1	1	B2	B6	6	E2	VDD	S		-	-	-
-	-	2	2	A2	B7	7	C1	PC13	I/O	FT	-	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/WKUP2
2	1	3	3	A1	C6	8	D1	PC14- OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
3	2	4	4	B1	C7	9	E1	PC15- OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
-	-	-	-	-	-	10	F2	PH9	I/O	FT	-	-	-
-	-	-	-	-	-	11	G2	PH10	I/O	FT	-	-	-
-	-	5	5	C1	D6	12	F1	PH0-OSC_IN (PH0)	I/O	TC	-	-	OSC_IN
-	-	6	6	D1	D7	13	G1	PH1- OSC_OUT (PH1)	I/O	TC	-	-	OSC_OUT
4	3	7	7	E1	D5	14	H2	NRST	I/O	-	-	-	-
-	-	-	8	E3	C5	15	H1	PC0	I/O	FTf	-	LPTIM1_IN1, EVENTOUT, LPUART1_RX, I2C3_SCL	ADC_IN10
-	-	-	9	E2	C4	16	J2	PC1	I/O	FTf	-	LPTIM1_OUT, EVENTOUT, LPUART1_TX, I2C3_SDA	ADC_IN11
-	-	-	10	F2	E7	17	J3	PC2	I/O	FTf	-	LPTIM1_IN2, SPI2_MISO/I2S2_MCK	ADC_IN12

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	-	-	54	B5	-	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, TIM3_ETR, USART5_RX	-
-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, SPI2_MISO/I2S2_MCK	-
-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS_DE, SPI2_MOSI/I2S2_SD	-
-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX	-
-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX	-
-	-	-	-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, TIM21_CH2	-
26	-	39	55	A5	A3	89	A8	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT, USART1_RTS_DE, USART5_TX	COMP2_INM
27	26	40	56	A4	B3	90	A7	PB4	I/O	FTf	-	SPI1_MISO, TIM3_CH1, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
28	27	41	57	C4	A4	91	C5	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_RTS_DE	COMP2_INP
29	28	42	58	D3	B4	92	B5	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR,	COMP2_INP

Figure 16. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS

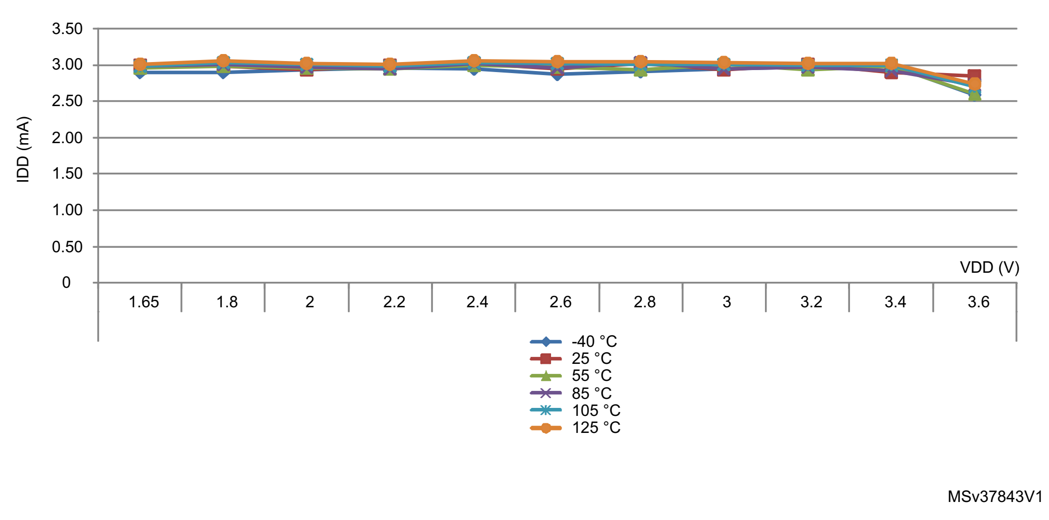


Figure 17. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS

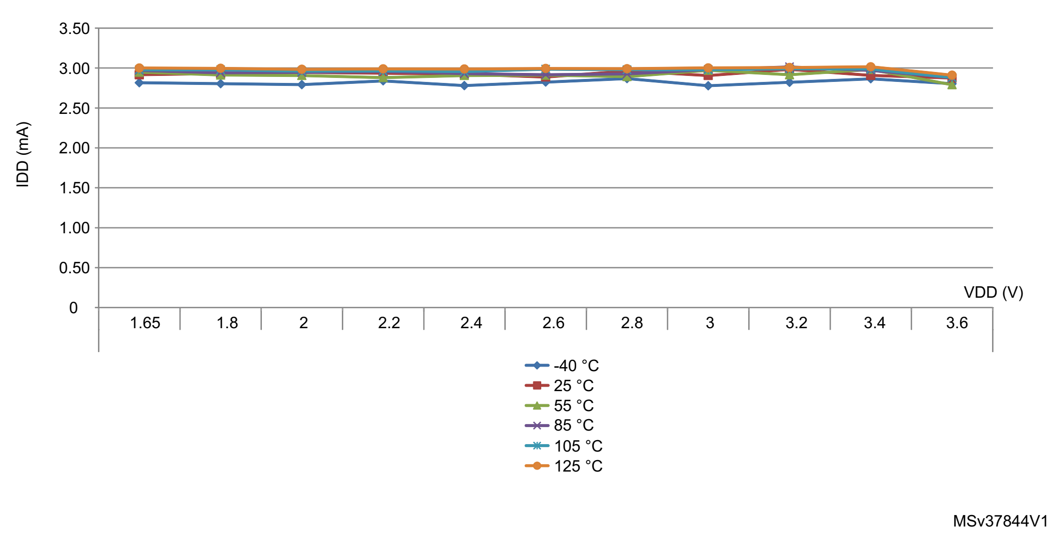


Table 39. Peripheral current consumption in Run or Sleep mode[1] (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOE	8	6	5	6	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0[3]	0[3]	0[3]	0[3]	
	DMA1	10	8	6.5	8.5	
All enabled		204	162	130	202	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 µA.

Table 41. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	f_{HCLK} = f_{MSI} = 4.2 MHz	5.0	8	µs
		f_{HCLK} = f_{HSI} = 16 MHz	4.9	7	
		f_{HCLK} = f_{HSI}/4 = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	f_{HCLK} = f_{MSI} = 4.2 MHz Voltage range 1	5.0	8	
		f_{HCLK} = f_{MSI} = 4.2 MHz Voltage range 2	5.0	8	
		f_{HCLK} = f_{MSI} = 4.2 MHz Voltage range 3	5.0	8	
		f_{HCLK} = f_{MSI} = 2.1 MHz	7.3	13	
		f_{HCLK} = f_{MSI} = 1.05 MHz	13	23	
		f_{HCLK} = f_{MSI} = 524 kHz	28	38	
		f_{HCLK} = f_{MSI} = 262 kHz	51	65	
		f_{HCLK} = f_{MSI} = 131 kHz	100	120	
		f_{HCLK} = MSI = 65 kHz	190	260	
		f_{HCLK} = f_{HSI} = 16 MHz	4.9	7	
		f_{HCLK} = f_{HSI}/4 = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	f_{HCLK} = f_{HSI} = 16 MHz	4.9	7	
		f_{HCLK} = f_{HSI}/4 = 4 MHz	7.9	10	
		f_{HCLK} = f_{MSI} = 4.2 MHz	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	65	130	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.2	3	ms

Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$I_{DD(MSI)}$[2]	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}$[2]	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range at 32 MHz	Unit
S_{EMI}	Peak level	$V_{DD} = 3.6$ V, $T_A = 25$ °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-7	dBµV
			30 to 130 MHz	14	
			130 MHz to 1 GHz	9	
			EMI Level	2	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 56. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 25*.

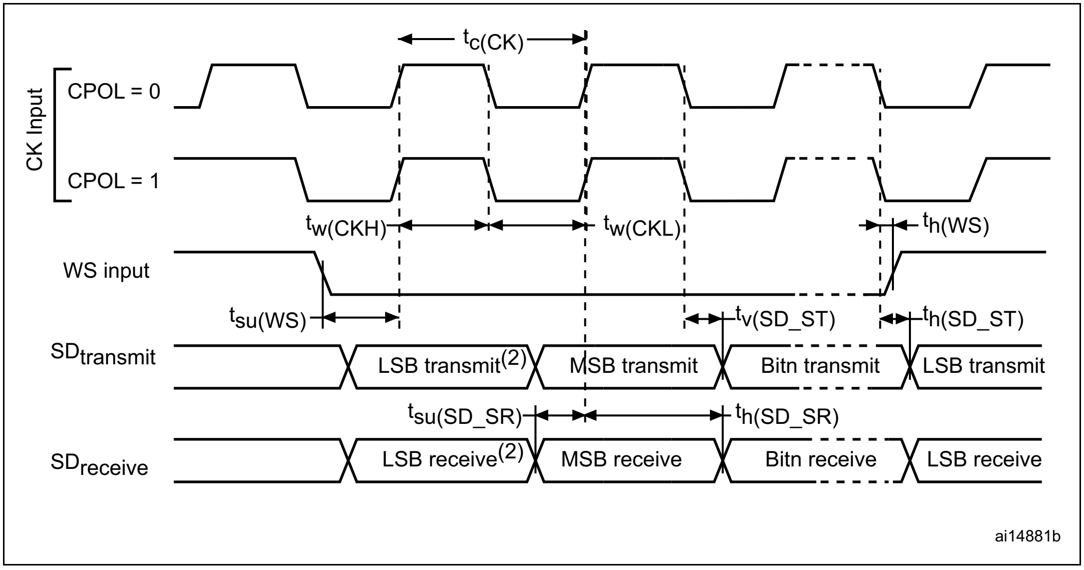
Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 72. SPI characteristics in voltage Range 1 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71<V_{DD}<3.6V$	-	-	12(2)	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$	-	-	16(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	3.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.65\ V<V_{DD}<3.6\ V$	-	18	41	
		Slave mode $2.7\ V<V_{DD}<3.6\ V$	-	18	25	
$t_{v(MO)}$		Master mode	-	4	7	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

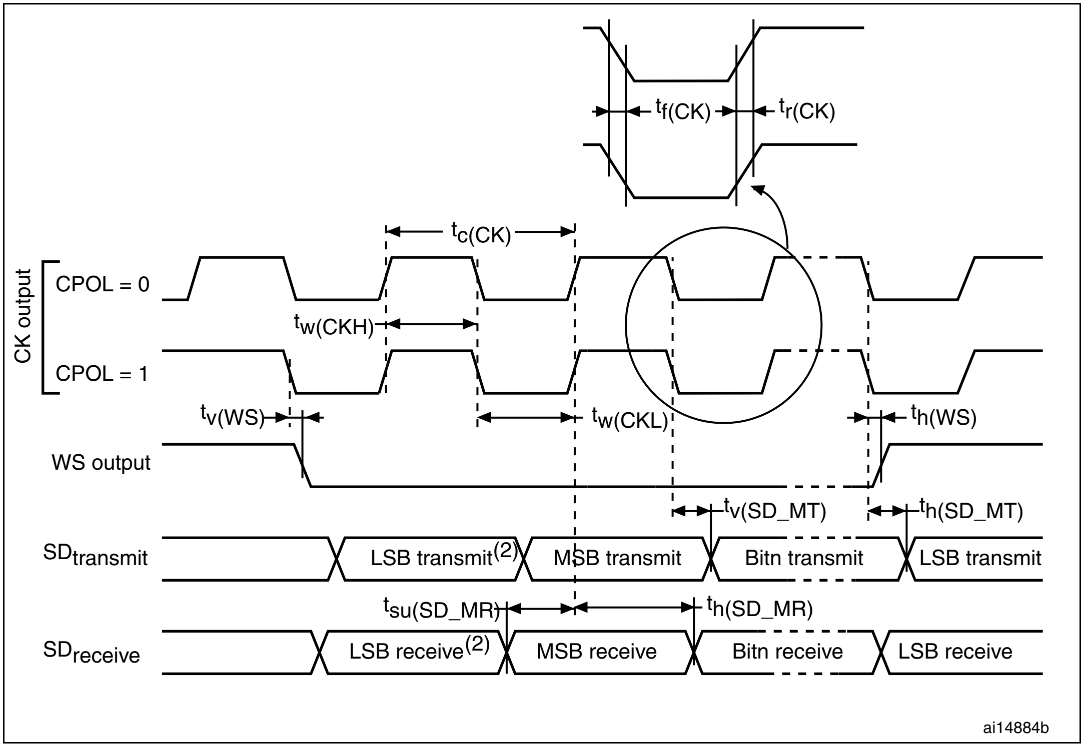
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while $Duty_{(SCK)} = 50\%$.

Figure 37. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: 0.3 × V_{DD} and 0.7 × V_{DD}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 38. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

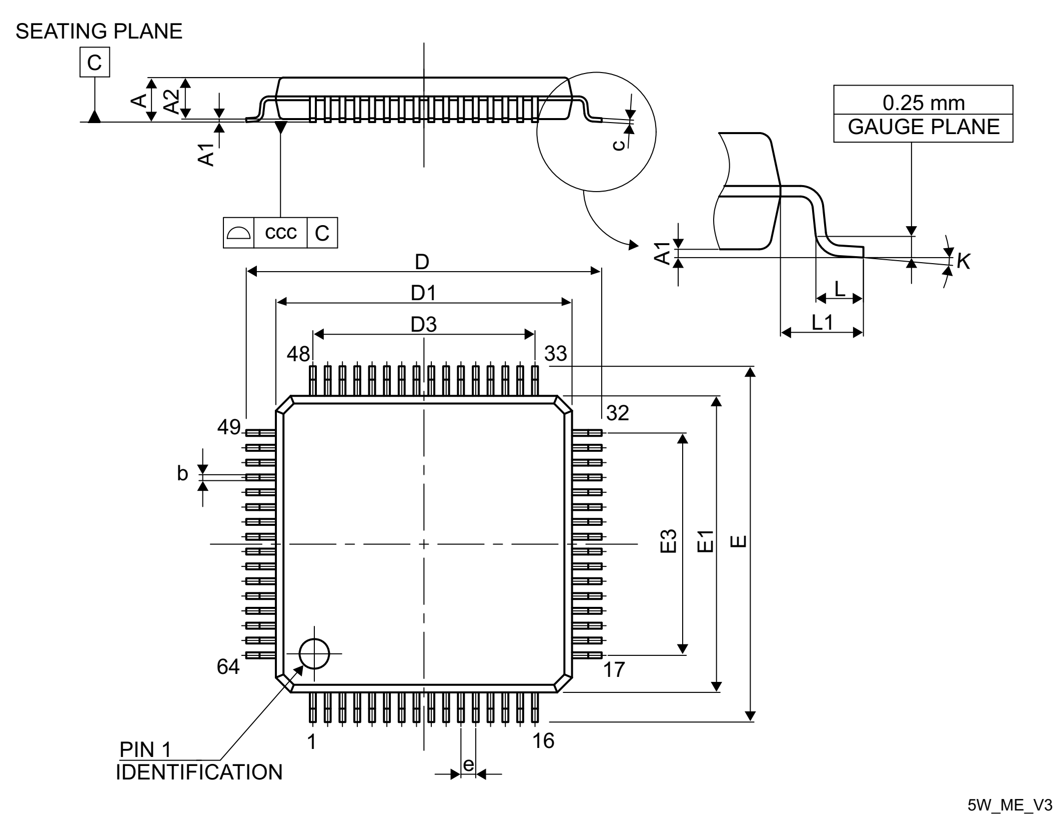
Table 76. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 LQFP64 package information

Figure 44. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline

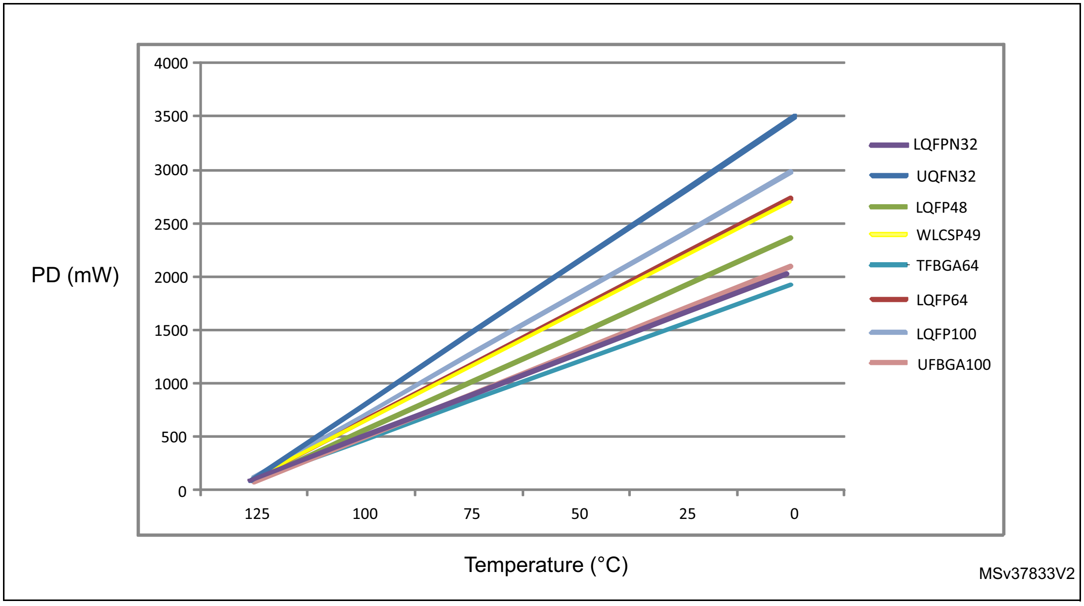


1. Drawing is not to scale.

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Figure 62. Thermal resistance



7.9.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

9 Revision history

Table 89. Document revision history

Date	Revision	Changes
02-Sep-2015	1	Initial release
26-Oct-2015	2	Changed confidentiality level to public. Updated datasheet status to “production data”. Modified ultra-low-power platform features on cover page. In *Table 15: STM32L071xxx pin definition*: – changed pin name to VDDIO2 for the following pins: UFQFPN32 pin 24, LQFP48 pin 36, LQFP64 pin 48, UFBGA64 pin E5, WLCSP49 pin A1, LQFP100 pin 75 and UFBGA100 pin G11. – Added note related to UFQFPN32. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated $\|\Delta V_{SS}\|$ definition to include V_{REF-} in *Table 22: Voltage characteristics*. Updated f_{TRIG} and V_{AIN} maximum value, added V_{REF+} and V_{REF-} in *Table 62: ADC characteristics*. Added *Section : Device marking for LQFP100*. Updated *Figure 42: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 76: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*. Added *Section : Device marking for LQFP100*, *Section : Device marking for LQFP64*, *Section : Device marking for TFBGA64* and *Section : Device marking for WLCSP49*. Updated *Figure 55: LQFP48 marking example (package top view)*.