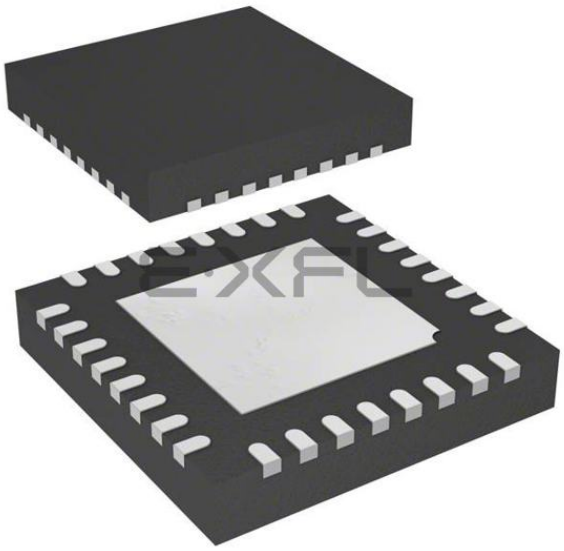

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071k8u3

2.1 Device overview

Table 2. Ultra-low-power STM32L071xx device features and peripheral counts

Peripheral		STM32L 071K8	STM32L 071C8	STM32L 071V8	STM32L 071KB	STM32L 071CB	STM32L 071VB	STM32L 071RB	STM32L 071KZ	STM32L 071CZ	STM32L 071VZ	STM32L 071RZ
Flash (Kbytes)		64 Kbytes			128 Kbytes				192 Kbytes			
Data EEPROM (Kbytes)		3 Kbytes			6 Kbytes							
RAM (Kbytes)		20 Kbytes										
Timers	General-purpose	4										
	Basic	2										
	LPTIMER	1										
RTC/SYSTICK/IWDG /WWDG		1/1/1/1										
Com. interfaces	SPI/I2S	4(3)[1]/0	6(4)[2]/1		4(3)[1]/0	6(4)[2]/1			4(3)[1]/0	6(4)[2]/1		
	I^2C	2	3		2	3			2	3		
	USART	3	4		3	4			3	4		
	LPUART	1										
GPIOs		23	37	84	25[3]	40[4]	84	51[5]	25[3]	40[4]	84	51[5]
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1										
12-bit synchronized ADC Number of channels		1 10	1 13	1 16	1 10	1 13[4]	1 16	1 16[5]	1 10	1 13[4]	1 16	1 16[5]
Comparators		2										
Max. CPU frequency		32 MHz										
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option										
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C										
Packages		UFQFPN 32	LQFP48	LQFP/ UFBGA 100	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64

1. 3 SPI interfaces are USARTs operating in SPI master mode.
2. 4 SPI interfaces are USARTs operating in SPI master mode.
3. UFQFPN32 has 2 GPIOs less than LQFP32.
4. LQFP48 has three GPIOs less than WLCSP49.
5. TFBGA64 has one GPIO, one ADC input less than LQFP64.

Table 3. Functionalities depending on the operating power supply range (continued)

Operating power supply range	Functionalities depending on the operating power supply range		
	ADC operation	Dynamic voltage scaling range	I/O operation
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

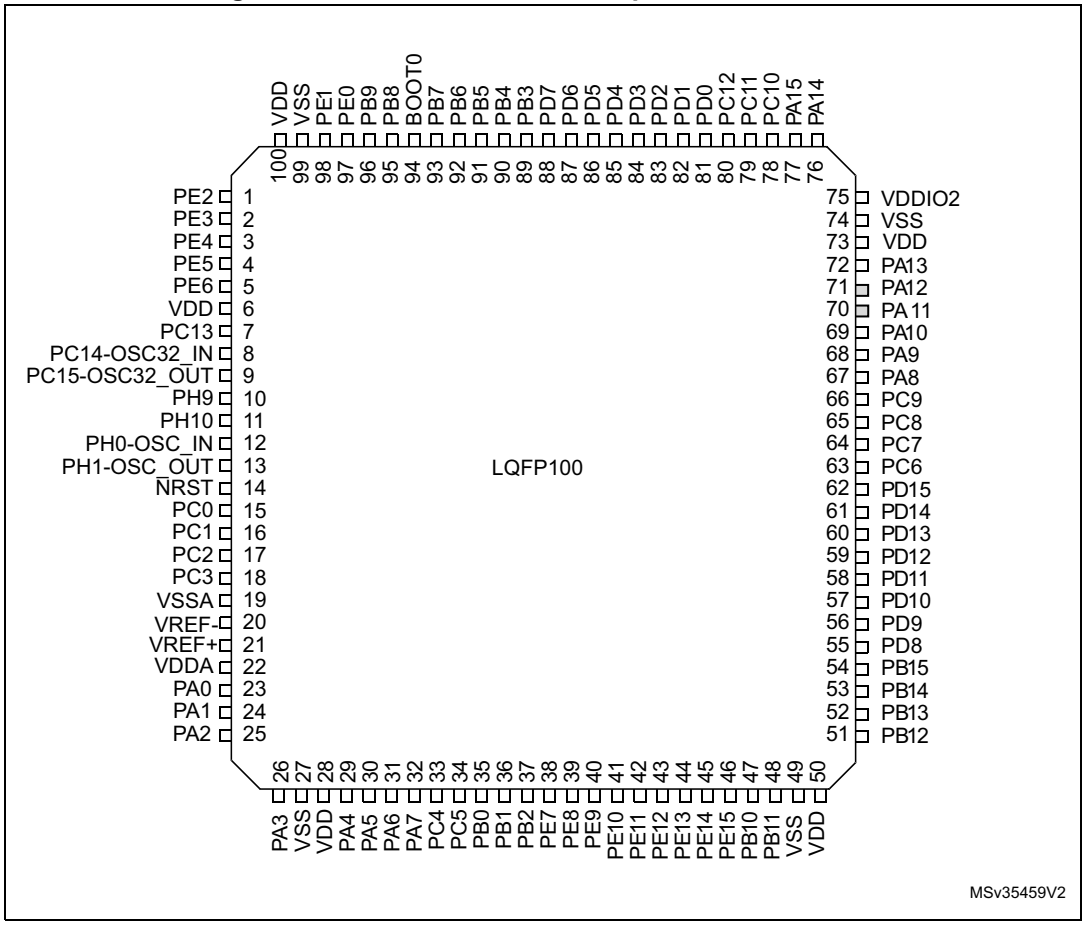
CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(3)		--	

4 Pin descriptions

Figure 3. STM32L071xx LQFP100 pinout - 14 x 14 mm



1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	11	-	-	18	K2	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD	ADC_IN13
-	4	8	12	F1	-	19	J1	VSSA	S		-	-	-
-	-	-	-	-	-	20	K1	VREF-	S		-	-	-
-	-	-	-	G1	E6	21	L1	VREF+	S		-	-	-
5	5	9	13	H1	F7	22	M1	VDDA	S		-	-	-
6	6	10	14	G2	E5	23	L2	PA0	I/O	TTa	-	TIM2_CH1, USART2_CTS, TIM2_ETR, USART4_TX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1
7	7	11	15	H2	E4	24	M2	PA1	I/O	FT	-	EVENTOUT, TIM2_CH2, USART2_RTS_DE, TIM21_ETR, USART4_RX	COMP1_INP, ADC_IN1
8	8	12	16	F3	F6	25	K3	PA2	I/O	FT	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2
9	9	13	17	G3	G7	26	L3	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
-	-	-	18	C2	-	27	D3	VSS	S	-	-	-	-
-	-	-	19	D2	-	28	H3	VDD	S	-	-	-	-
10	10	14	20	H3	F5	29	M3	PA4	I/O	TC	-	SPI1_NSS, USART2_CK, TIM22_ETR	COMP1_INM, COMP2_INM, ADC_IN4
11	11	15	21	F4	G6	30	K4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	39	E8	-	65	E10	PC8	I/O	FT	-	TIM22_ETR, TIM3_CH3	-
-	-	-	40	D8	-	66	D12	PC9	I/O	FTf	-	TIM21_ETR, TIM3_CH4, I2C3_SDA	-
18	18	29	41	D7	D1	67	D11	PA8	I/O	FTf	-	MCO, EVENTOUT, USART1_CK, I2C3_SCL	-
19	19	30	42	C7	E2	68	D10	PA9	I/O	FTf	-	MCO, USART1_TX, I2C1_SCL, I2C3_SMBA	-
20	20	31	43	C6	C1	69	C12	PA10	I/O	FTf	-	USART1_RX, I2C1_SDA	-
21	21	32	44	C8	D2	70	B12	PA11	I/O	FT	-	SPI1_MISO, EVENTOUT, USART1_CTS, COMP1_OUT	-
22	22	33	45	B8	B1	71	A12	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART1_RTS_DE, COMP2_OUT	-
23	23	34	46	A8	C2	72	A11	PA13	I/O	FT	-	SWDIO, LPUART1_RX	-
-	-	-	-	-	-	73	C11	VDD	S		-	-	-
-	-	35	47	D5	-	74	F11	VSS	S		-	-	-
-	24	36	48	E5	A1	75	G11	VDDIO2	S		-	-	-
24	25	37	49	A7	B2	76	A10	PA14	I/O	FT	-	SWCLK, USART2_TX, LPUART1_TX	-
25	-	38	50	A6	A2	77	A9	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE	-
-	-	-	51	B7	-	78	B11	PC10	I/O	FT	-	LPUART1_TX, USART4_TX	-
-	-	-	52	B6	-	79	C10	PC11	I/O	FT	-	LPUART1_RX, USART4_RX	-
-	-	-	53	C5	-	80	B10	PC12	I/O	FT	-	USART5_TX, USART4_CK	-

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	-	-	54	B5	-	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, TIM3_ETR, USART5_RX	-
-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, SPI2_MISO/I2S2_MCK	-
-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS_DE, SPI2_MOSI/I2S2_SD	-
-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX	-
-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX	-
-	-	-	-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, TIM21_CH2	-
26	-	39	55	A5	A3	89	A8	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT, USART1_RTS_DE, USART5_TX	COMP2_INM
27	26	40	56	A4	B3	90	A7	PB4	I/O	FTf	-	SPI1_MISO, TIM3_CH1, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
28	27	41	57	C4	A4	91	C5	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_RTS_DE	COMP2_INP
29	28	42	58	D3	B4	92	B5	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR,	COMP2_INP

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
30	29	43	59	C3	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	60	B4	A5	94	A4	BOOT0	I		-	-	-
-	-	45	61	B3	B5	95	A3	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	46	62	A3	A6	96	B3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	31	47	63	D4	-	99	D3	VSS	S		-	-	-
-	32	48	64	E4	A7	100	C4	VDD	S		-	-	-

1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.

Table 18. Alternate functions port C

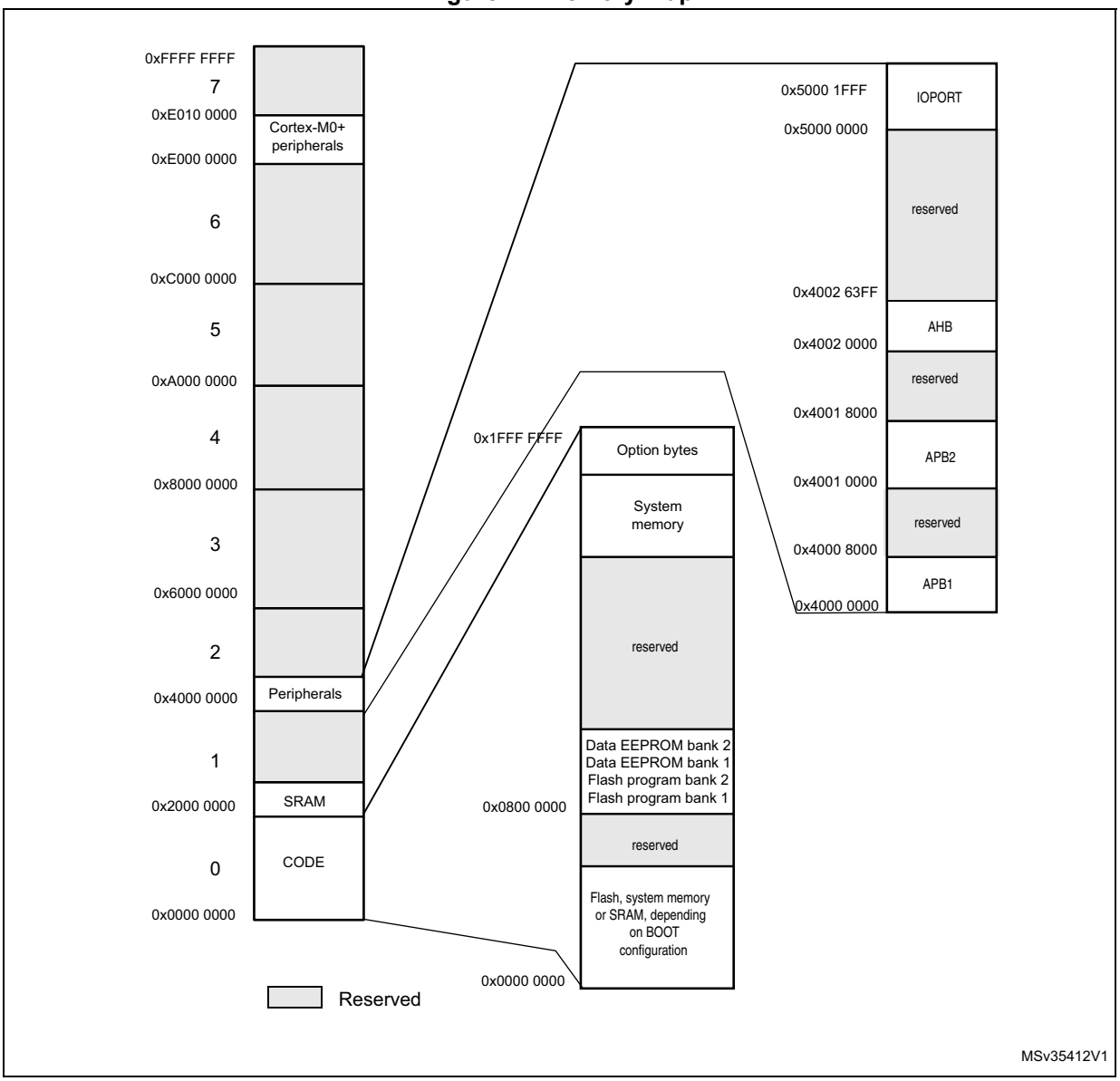
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port C	PC0	LPTIM1_IN1		EVENTOUT				LPUART1_RX	I2C3_SCL
	PC1	LPTIM1_OUT		EVENTOUT				LPUART1_TX	I2C3_SDA
	PC2	LPTIM1_IN2		SPI2_MISO/ I2S2_MCK					
	PC3	LPTIM1_ETR		SPI2_MOSI/ I2S2_SD					
	PC4	EVENTOUT		LPUART1_TX					
	PC5			LPUART1_RX					
	PC6	TIM22_CH1		TIM3_CH1					
	PC7	TIM22_CH2		TIM3_CH2					
	PC8	TIM22_ETR		TIM3_CH3					
	PC9	TIM21_ETR		TIM3_CH4					I2C3_SDA
	PC10	LPUART1_TX						USART4_TX	
	PC11	LPUART1_RX						USART4_RX	
	PC12			USART5_TX				USART4_CK	
	PC13								
	PC14								
	PC15								

Table 19. Alternate functions port D

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Port D	PD0	TIM21_CH1	SPI2_NSS/I2S2_WS	-	-	-	-	-	-
	PD1	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-
	PD2	LPUART1_RTS_ DE		TIM3_ETR	-	-	-	USART5_RX	-
	PD3	USART2_CTS		SPI2_MISO/ I2S2_MCK	-	-	-	-	-
	PD4	USART2_RTS_D E	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-
	PD5	USART2_TX	-	-	-	-	-	-	-
	PD6	USART2_RX	-	-	-	-	-	-	-
	PD7	USART2_CK	TIM21_CH2	-	-	-	-	-	-
	PD8	LPUART1_TX		-	-	-	-	-	-
	PD9	LPUART1_RX		-	-	-	-	-	-
	PD10	-		-	-	-	-	-	-
	PD11	LPUART1_CTS		-	-	-	-	-	-
	PD12	LPUART1_RTS_ DE		-	-	-	-	-	-
	PD13	-		-	-	-	-	-	-
	PD14	-		-	-	-	-	-	-
	PD15			-	-	-	-	-	-

5 Memory mapping

Figure 11. Memory map



1. Refer to the STM32L071xx reference manual for details on the Flash memory organization for each memory size.

Table 31. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Condition		f_{HCLK} (MHz)	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode code executed from RAM, Flash memory switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	175	230	µA
				2	315	360	
				4	570	630	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	0,71	0,78	mA
				8	1,35	1,6	
				16	2,7	3	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	1,7	1,9	
				16	3,2	3,7	
				32	6,65	7,1	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	38	98	µA
				0,524	105	160	
				4,2	615	710	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	2,85	3	mA
			Range1, Vcore=1.8 V VOS[1:0]=01	32	6,85	7,3	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 32. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash memory switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL on)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	570	µA
				CoreMark		670	
				Fibonacci		410	
				while(1)		375	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6,65	mA
				CoreMark		6,95	
				Fibonacci		5,9	
				while(1)		5,2	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 39. Peripheral current consumption in Run or Sleep mode(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	CRS	2.5	2	2	2	µA/MHz (f_{HCLK})
	I2C1	11	9.5	7.5	9	
	I2C3	11	9	7	9	
	LPTIM1	10	8.5	6.5	8	
	LPUART1	8	6.5	5.5	6	
	SPI2	9	4.5	3.5	4	
	USART2	14.5	12	9.5	11	
	USART4	5	4	3	5	
	USART5	5	4	3	5	
	TIM2	10.5	8.5	7	9	
	TIM3	12	10	8	11	
	TIM6	3.5	3	2.5	2	
	TIM7	3.5	3	2.5	2	
	WWDG	3	2	2	2	
APB2	ADC1(2)	5.5	5	3.5	4	µA/MHz (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

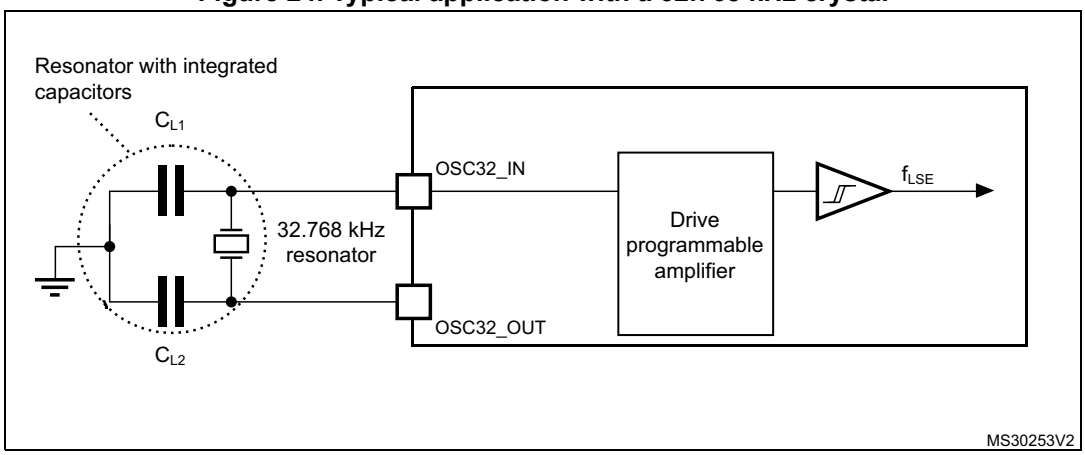
Table 45. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 24. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 PLL characteristics

The parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

Table 49. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-		±600	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}	-	220	450	µA
I_{DD}(PLL)	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

RAM memory

Table 50. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 51. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 53*. They are based on the EMS levels and classes defined in application note AN1709.

Table 53. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 63. R_{AIN} max for f_{ADC} = 16 MHz(1)

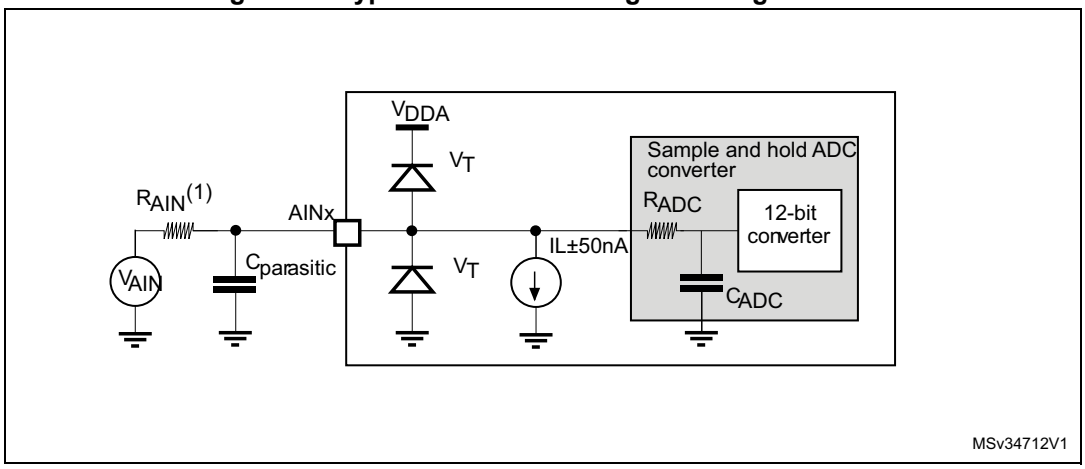
T_S (cycles)	t_S (µs)	R_{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (kΩ)						
			V_{DD} > 2.7 V	V_{DD} > 2.4 V	V_{DD} > 2.0 V	V_{DD} > 1.8 V	V_{DD} > 1.75 V	V_{DD} > 1.65 V and T_A > –10 °C	V_{DD} > 1.65 V and T_A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 64. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} = V_{REF+}< 3.6 V, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(4)		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(4)		70	76	-	
THD	Total harmonic distortion		-	-85	-73	

Figure 31. Typical connection diagram using the ADC

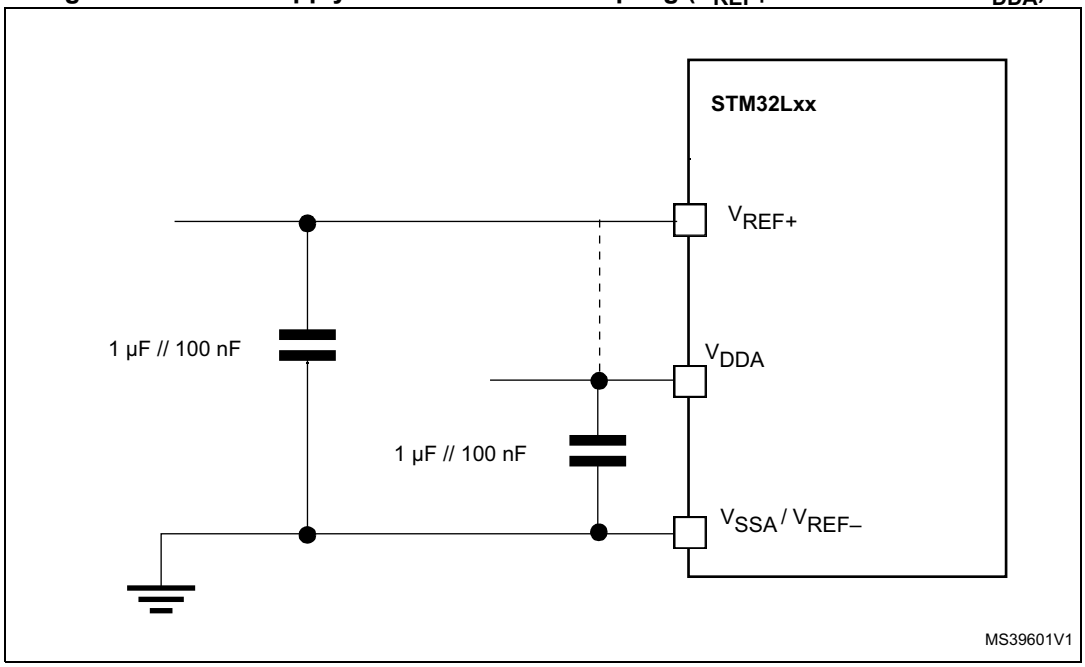


1. Refer to *Table 62: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

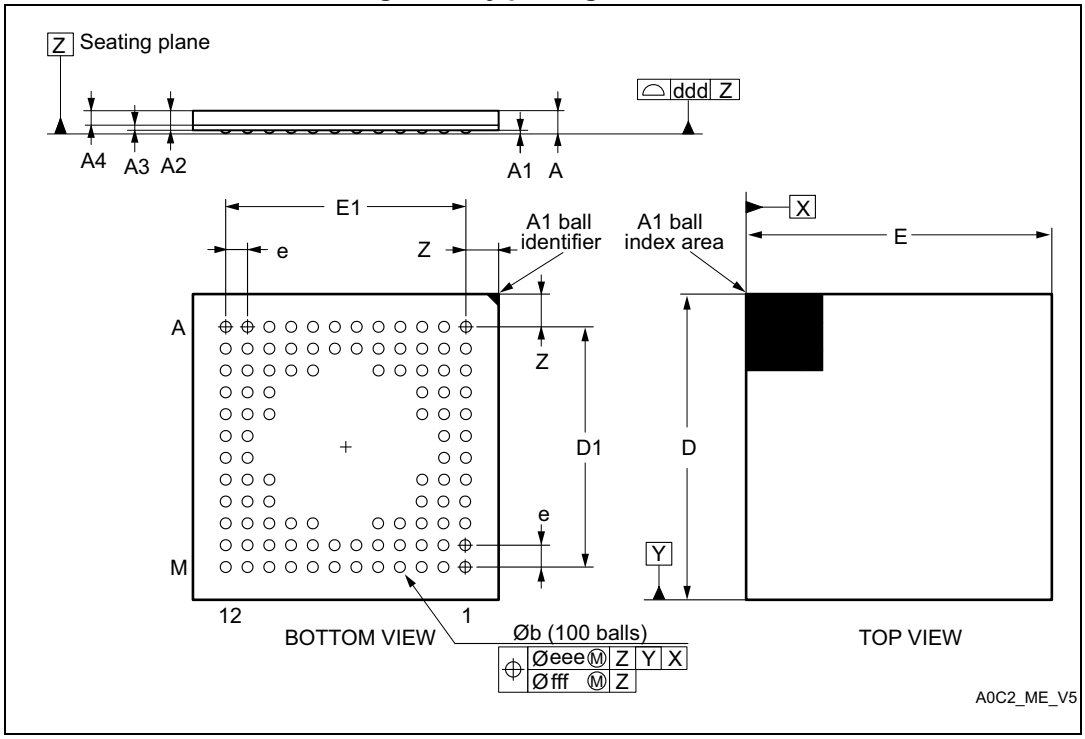
Power supply decoupling should be performed as shown in *Figure 32* or *Figure 33*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 32. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



7.2 UFBGA100 package information

Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



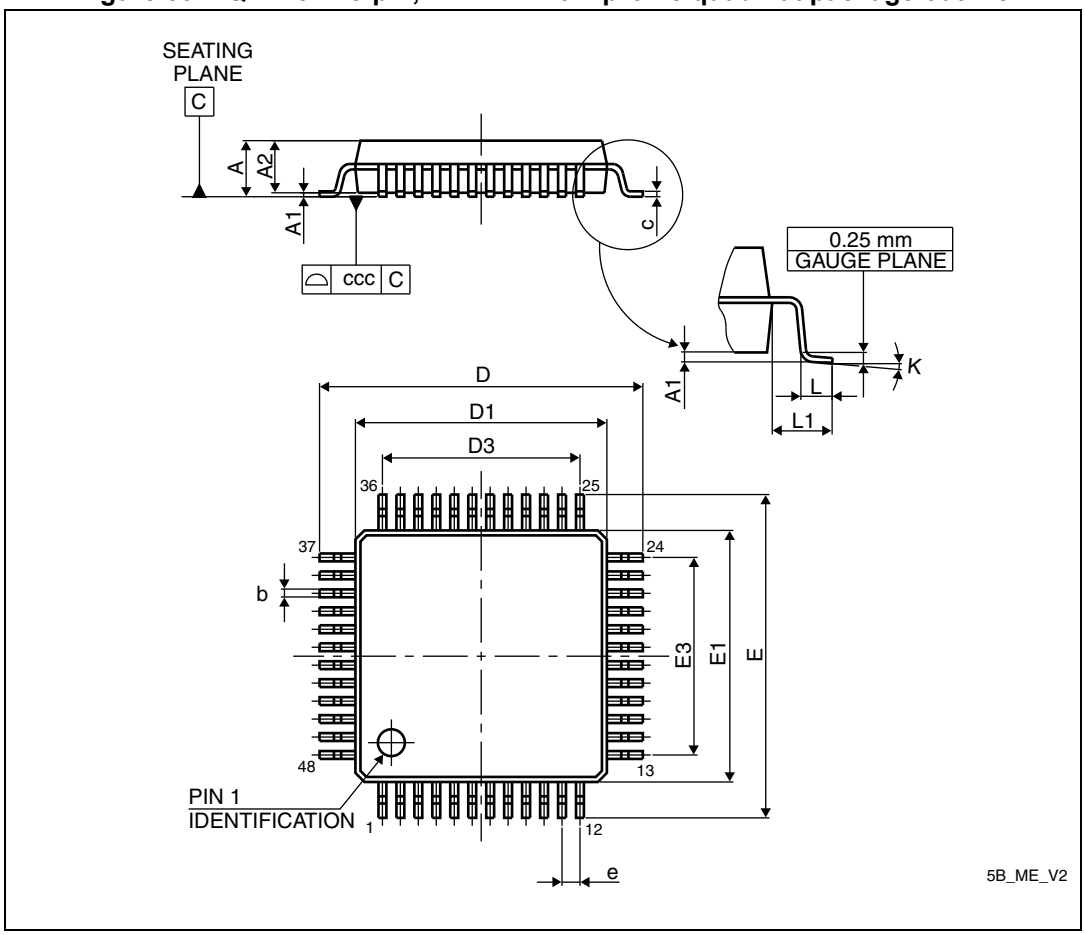
1. Drawing is not to scale.

Table 77. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

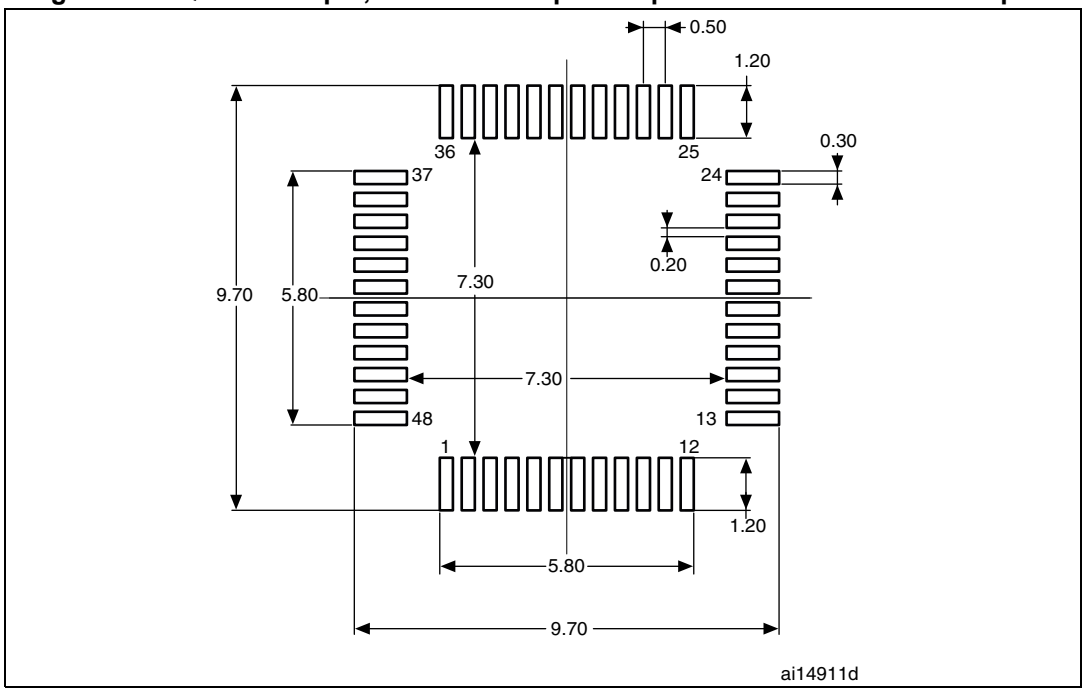
7.6 LQFP48 package information

Figure 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 54. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

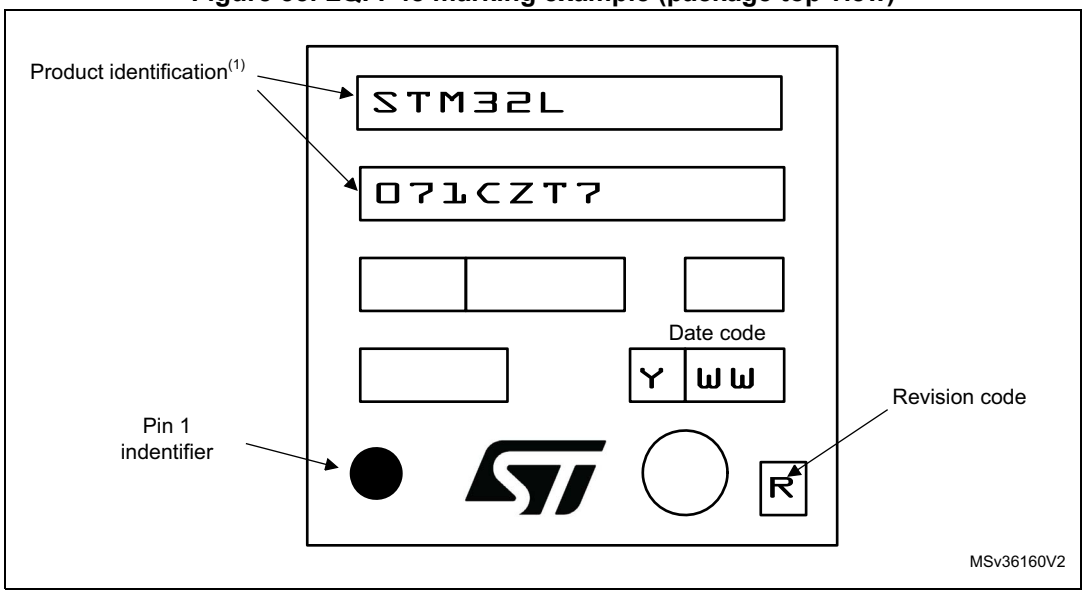


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 55. LQFP48 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.