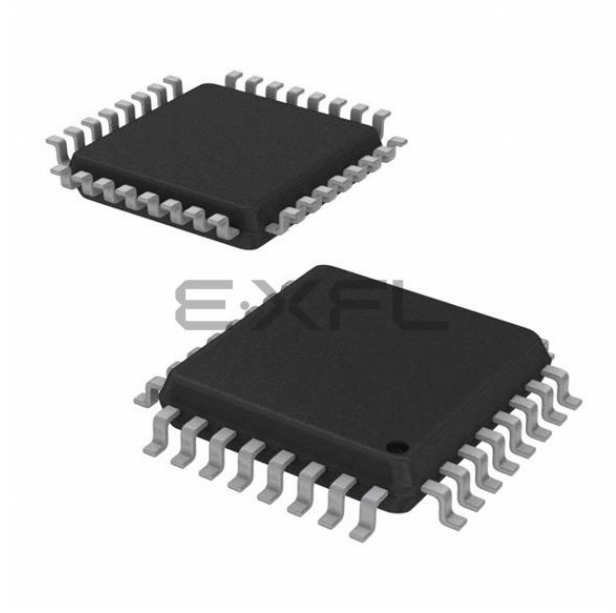

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 6K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071kbt6tr |

# List of figures

## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire $V_{CORE}$ domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.*

**Table 3. Functionalities depending on the operating power supply range**

| Operating power supply range | Functionalities depending on the operating power supply range | | |
|---|---|---|---|
| | ADC operation | Dynamic voltage scaling range | I/O operation |
| $V_{DD}$ = 1.65 to 1.71 V | ADC only, conversion time up to 570 ksps | Range 2 or range 3 | Degraded speed performance |
| $V_{DD}$ = 1.71 to 1.8 V(1) | ADC only, conversion time up to 1.14 Msps | Range 1, range 2 or range 3 | Degraded speed performance |
| $V_{DD}$ = 1.8 to 2.0 V(1) | Conversion time up to 1.14 Msps | Range1, range 2 or range 3 | Degraded speed performance |

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

### 3.15.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

One standard I2S interfaces (multiplexed with SPI2) is available. It can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When the I2S interfaces is configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The SPIs can be served by the DMA controller.

Refer to *Table 13* for the differences between SPI1 and SPI2.

**Table 13. SPI/I2S implementation**

| SPI features(1) | SPI1 | SPI2 |
|---|---|---|
| Hardware CRC calculation | X | X |
| I2S mode | - | X |
| TI mode | X | X |

1. X = supported.

## 3.16 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

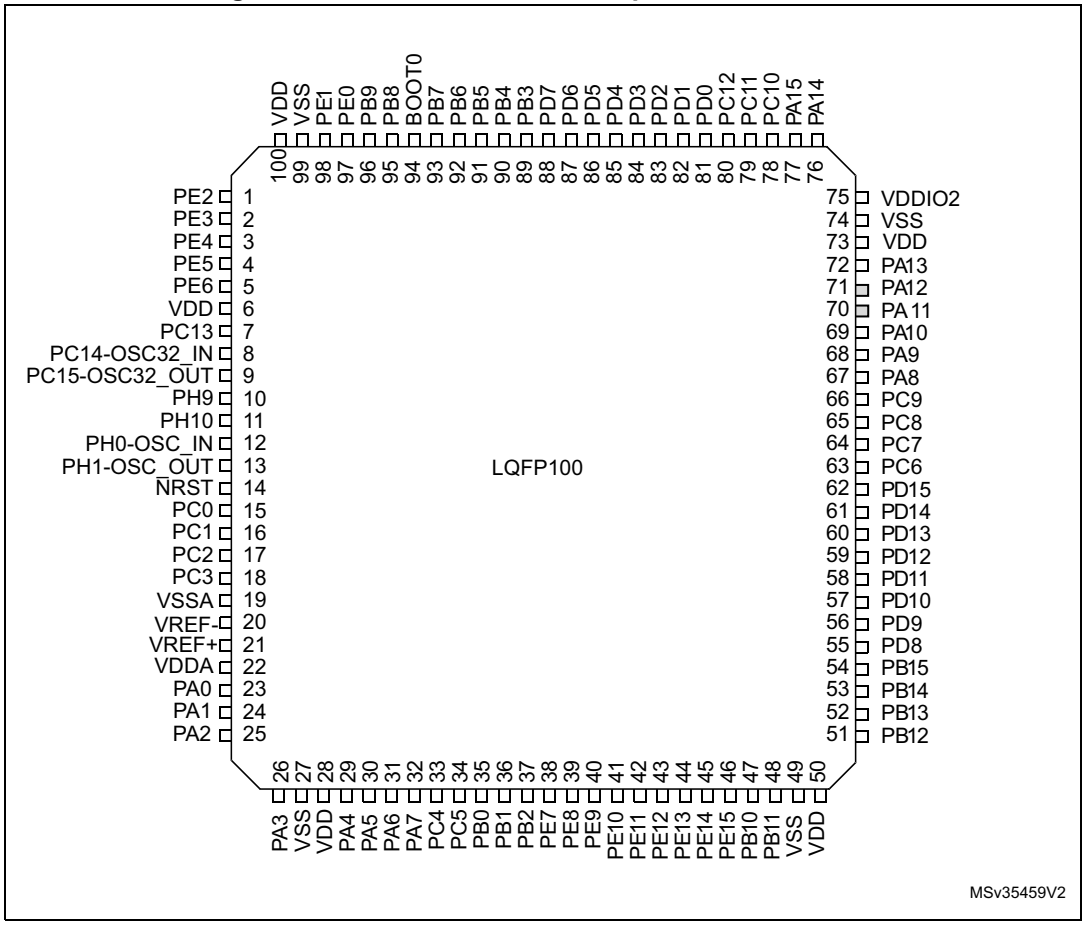
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.17 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

# 4 Pin descriptions

**Figure 3. STM32L071xx LQFP100 pinout - 14 x 14 mm**




1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

**Table 15. STM32L071xxx pin definition (continued)**

| Pin number | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP32 | UFQFPN32(1) | LQFP48 | LQFP64 | UFBGA64 | WLCSP49 | LQFP100 | UFBG100 | | | | | | |
| 30 | 29 | 43 | 59 | C3 | C3 | 93 | B4 | PB7 | I/O | FTf | - | USART1_RX, I2C1_SDA, LPTIM1_IN2, USART4_CTS | COMP2_INP, VREF_PVD_IN |
| 31 | 30 | 44 | 60 | B4 | A5 | 94 | A4 | BOOT0 | I | | - | - | - |
| - | - | 45 | 61 | B3 | B5 | 95 | A3 | PB8 | I/O | FTf | - | I2C1_SCL | - |
| - | - | 46 | 62 | A3 | A6 | 96 | B3 | PB9 | I/O | FTf | - | EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS | - |
| - | - | - | - | - | - | 97 | C3 | PE0 | I/O | FT | - | EVENTOUT | - |
| - | - | - | - | - | - | 98 | A2 | PE1 | I/O | FT | - | EVENTOUT | - |
| 32 | 31 | 47 | 63 | D4 | - | 99 | D3 | VSS | S | | - | - | - |
| - | 32 | 48 | 64 | E4 | A7 | 100 | C4 | VDD | S | | - | - | - |

1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.

**Table 18. Alternate functions port C**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2/I2C1/ TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/SYS_AF | I2C1/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT | I2C3/LPUART1/ COMP1/2/ TIM3 |
| Port C | PC0 | LPTIM1_IN1 | | EVENTOUT | | | | LPUART1_RX | I2C3_SCL |
| | PC1 | LPTIM1_OUT | | EVENTOUT | | | | LPUART1_TX | I2C3_SDA |
| | PC2 | LPTIM1_IN2 | | SPI2_MISO/ I2S2_MCK | | | | | |
| | PC3 | LPTIM1_ETR | | SPI2_MOSI/ I2S2_SD | | | | | |
| | PC4 | EVENTOUT | | LPUART1_TX | | | | | |
| | PC5 | | | LPUART1_RX | | | | | |
| | PC6 | TIM22_CH1 | | TIM3_CH1 | | | | | |
| | PC7 | TIM22_CH2 | | TIM3_CH2 | | | | | |
| | PC8 | TIM22_ETR | | TIM3_CH3 | | | | | |
| | PC9 | TIM21_ETR | | TIM3_CH4 | | | | | I2C3_SDA |
| | PC10 | LPUART1_TX | | | | | | USART4_TX | |
| | PC11 | LPUART1_RX | | | | | | USART4_RX | |
| | PC12 | | | USART5_TX | | | | USART4_CK | |
| | PC13 | | | | | | | | |
| | PC14 | | | | | | | | |
| | PC15 | | | | | | | | |

**Table 21. Alternate functions port H**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/ I2S2/USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2 /I2C1/TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3/ EVENTOUT/ SYS_AF | I2C1/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2/I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT | I2C3/ LPUART1/ COMP1/2/ TIM3 |
| Port H | PH0 | | - | - | - | - | - | - | - |
| | PH1 | - | - | - | - | - | - | - | - |
| | PH9 | - | - | - | - | - | - | - | - |
| | PH10 | - | - | - | - | - | - | - | - |

**Table 26. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD6}$ | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | V |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |
| $V_{hyst}$ | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| | | All BOR and PVD thresholds excepting BOR0 | - | 100 | - | |

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

### 6.3.3 Embedded internal reference voltage

The parameters given in *Table 28* are based on characterization results, unless otherwise specified.

**Table 27. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 25 °C $V_{DDA}$= 3 V | 0x1FF8 0078 - 0x1FF8 0079 |

**Table 28. Embedded internal reference voltage(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$(2) | Internal reference voltage | – 40 °C < $T_J$ < +125 °C | 1.202 | 1.224 | 1.242 | V |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ and $V_{REF+}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REFINT}$ value(3) | Including uncertainties due to ADC and $V_{DDA}$/$V_{REF+}$ values | - | - | ±5 | mV |
| $T_{Coeff}$(4) | Temperature coefficient | –40 °C < $T_J$ < +125 °C | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$(4) | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$(4) | Voltage coefficient | 3.0 V < $V_{DDA}$ < 3.6 V | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$(4)(5) | ADC sampling time when reading the internal reference voltage | - | 5 | 10 | - | µs |
| $T_{ADC\_BUF}$(4) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$(4) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$(4) | VREF_OUT output current(6) | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$(4) | VREF_OUT output load | - | - | - | 50 | pF |

**Figure 18. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS**

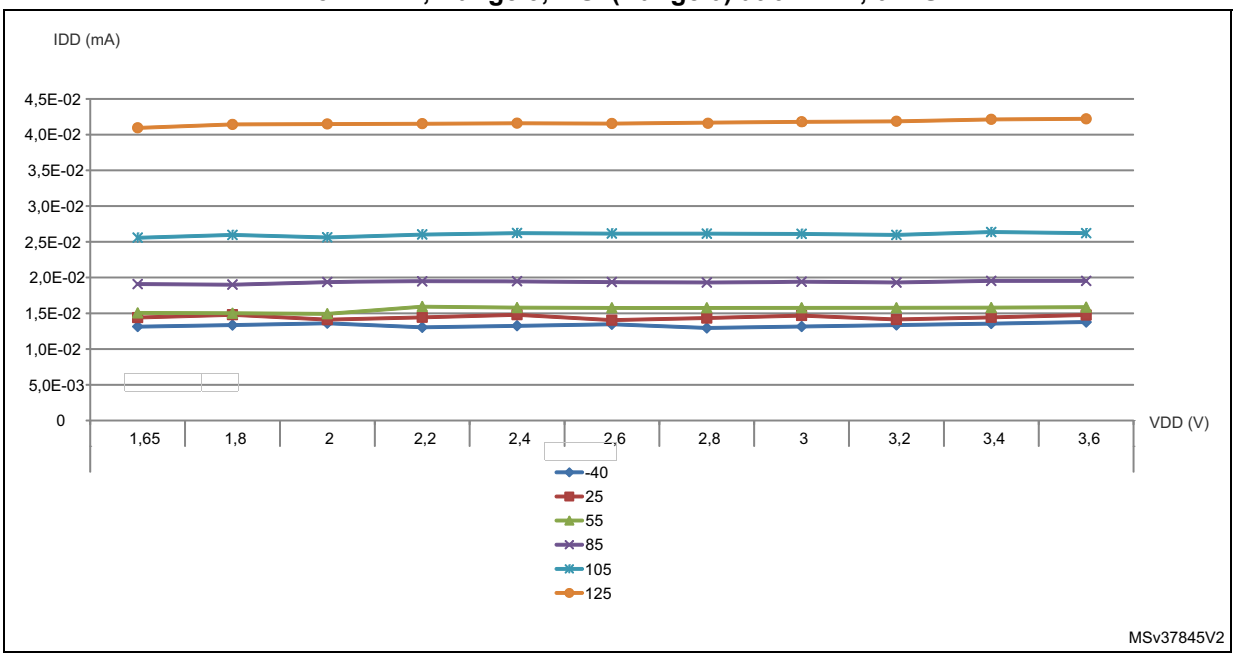



**Table 35. Current consumption in Low-power sleep mode**

| Symbol | Parameter | Condition | | | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Sleep) | Supply current in Low-power sleep mode | All peripherals OFF, code executed from Flash memory, $V_{DD}$ from 1.65 to 3.6 V | MSI clock = 65 kHz, $f_{HCLK}$= 32 kHz, Flash memory OFF | $T_A$ = −40 to 25°C | 4,7 | - | µA |
| | | | MSI clock = 65 kHz, $f_{HCLK}$= 32 kHz | $T_A$ = −40 to 25°C | 17 | 24 | |
| | | | | $T_A$ = 85°C | 19,5 | 30 | |
| | | | | $T_A$= 105°C | 23 | 47 | |
| | | | | $T_A$= 125°C | 32,5 | 70 | |
| | | | MSI clock = 65 kHz, $f_{HCLK}$= 65 kHz | $T_A$= − 40 to 25°C | 17 | 24 | |
| | | | | $T_A$= 85°C | 20 | 31 | |
| | | | | $T_A$ = 105°C | 23,5 | 47 | |
| | | | | $T_A$ = 125°C | 32,5 | 70 | |
| | | | MSI clock = 131kHz, $f_{HCLK}$= 131 kHz | $T_A$= − 40 to 25°C | 19,5 | 27 | |
| | | | | $T_A$ = 55°C | 20,5 | 28 | |
| | | | | $T_A$ = 85°C | 22,5 | 33 | |
| | | | | $T_A$ = 105°C | 26 | 50 | |
| | | | | $T_A$= 125°C | 35 | 73 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

**Table 36. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ (Stop) | Supply current in Stop mode | $T_A$ = − 40 to 25°C | 0,43 | 1,00 | µA |
| | | $T_A$ = 55°C | 0,735 | 2,50 | |
| | | $T_A$= 85°C | 2,25 | 4,90 | |
| | | $T_A$ = 105°C | 5,3 | 13,00 | |
| | | $T_A$ = 125°C | 12,5 | 28,00 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

**Figure 19. $I_{DD}$ vs $V_{DD}$, at $T_A$= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive**

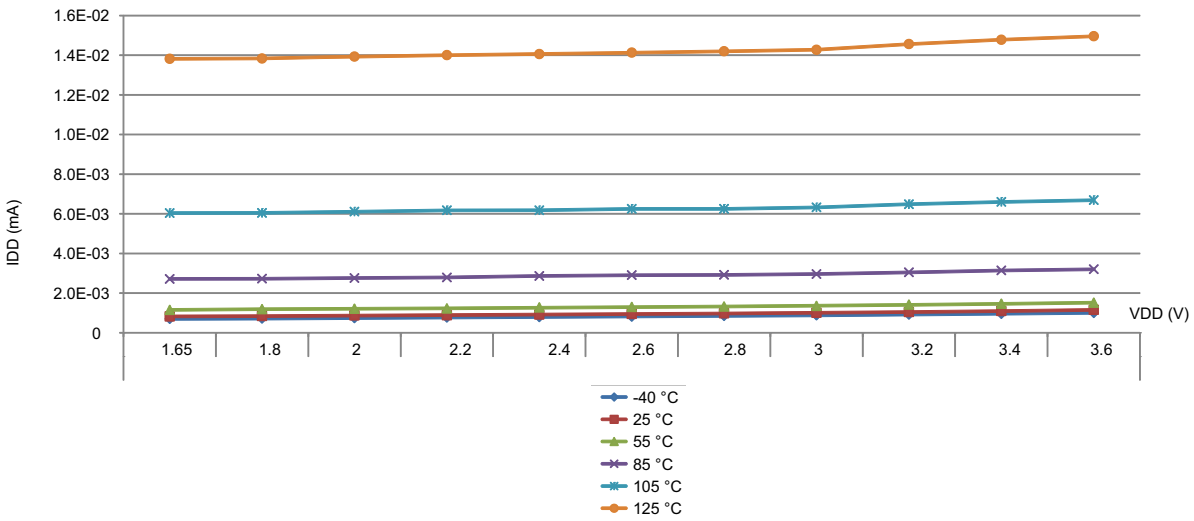


**Table 41. Low-power mode wakeup timings (continued)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUSTOP}$ | Wakeup from Stop mode, regulator in Run mode | $f_{HCLK} = f_{MSI}$ = 4.2 MHz | 5.0 | 8 | µs |
| | | $f_{HCLK} = f_{HSI}$ = 16 MHz | 4.9 | 7 | |
| | | $f_{HCLK} = f_{HSI}/4$ = 4 MHz | 8.0 | 11 | |
| | Wakeup from Stop mode, regulator in low-power mode | $f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1 | 5.0 | 8 | |
| | | $f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2 | 5.0 | 8 | |
| | | $f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3 | 5.0 | 8 | |
| | | $f_{HCLK} = f_{MSI}$ = 2.1 MHz | 7.3 | 13 | |
| | | $f_{HCLK} = f_{MSI}$ = 1.05 MHz | 13 | 23 | |
| | | $f_{HCLK} = f_{MSI}$ = 524 kHz | 28 | 38 | |
| | | $f_{HCLK} = f_{MSI}$ = 262 kHz | 51 | 65 | |
| | | $f_{HCLK} = f_{MSI}$ = 131 kHz | 100 | 120 | |
| | | $f_{HCLK}$ = MSI = 65 kHz | 190 | 260 | |
| | | $f_{HCLK} = f_{HSI}$ = 16 MHz | 4.9 | 7 | |
| | | $f_{HCLK} = f_{HSI}/4$ = 4 MHz | 8.0 | 11 | |
| | Wakeup from Stop mode, regulator in low-power mode, code running from RAM | $f_{HCLK} = f_{HSI}$ = 16 MHz | 4.9 | 7 | |
| | | $f_{HCLK} = f_{HSI}/4$ = 4 MHz | 7.9 | 10 | |
| | | $f_{HCLK} = f_{MSI}$ = 4.2 MHz | 4.7 | 8 | |
| $t_{WUSTDBY}$ | Wakeup from Standby mode FWU bit = 1 | $f_{HCLK}$ = MSI = 2.1 MHz | 65 | 130 | |
| | Wakeup from Standby mode FWU bit = 0 | $f_{HCLK}$ = MSI = 2.1 MHz | 2.2 | 3 | ms |

**Table 51. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Average current during the whole programming / erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 500 | 700 | µA |
| | Maximum current (peak) during the whole programming / erase operation | | - | 1.5 | 2.5 | mA |

1. Guaranteed by design.

**Table 52. Flash memory and data EEPROM endurance and retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{CYC}$(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 100 | |
| | Cycling (erase / write) Program memory | $T_A$ = -40°C to 125 °C | 0.2 | |
| | Cycling (erase / write) EEPROM data memory | | 2 | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | $T_{RET}$ = +85 °C | 30 | years |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 85 °C | | 30 | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | $T_{RET}$ = +105 °C | 10 | |
| | Data retention (EEPROM data memory) after 100 kcycles at $T_A$ = 105 °C | | | |
| | Data retention (program memory) after 200 cycles at $T_A$ = 125 °C | $T_{RET}$ = +125 °C | | |
| | Data retention (EEPROM data memory) after 2 kcycles at $T_A$ = 125 °C | | | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

### 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 54. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. frequency range at 32 MHz | Unit |
|---|---|---|---|---|---|
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | -7 | dBµV |
| | | | 30 to 130 MHz | 14 | |
| | | | 130 MHz to 1 GHz | 9 | |
| | | | EMI Level | 2 | - |

### 6.3.17 Comparators

**Table 67. Comparator 1 characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | | 3.6 | V |
| $R_{400K}$ | $R_{400K}$ value | - | - | 400 | - | kΩ |
| $R_{10K}$ | $R_{10K}$ value | - | - | 10 | - | |
| $V_{IN}$ | Comparator 1 input voltage range | - | 0.6 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | - | - | 7 | 10 | µs |
| td | Propagation delay(2) | - | - | 3 | 10 | |
| Voffset | Comparator offset | - | - | ±3 | ±10 | mV |
| $d_{Voffset}/dt$ | Comparator offset variation in worst voltage stress conditions | $V_{DDA}$ = 3.6 V, $V_{IN+}$ = 0 V, $V_{IN-}$ = $V_{REFINT}$, $T_A$ = 25 °C | 0 | 1.5 | 10 | mV/1000 h |
| $I_{COMP1}$ | Current consumption(3) | - | - | 160 | 260 | nA |

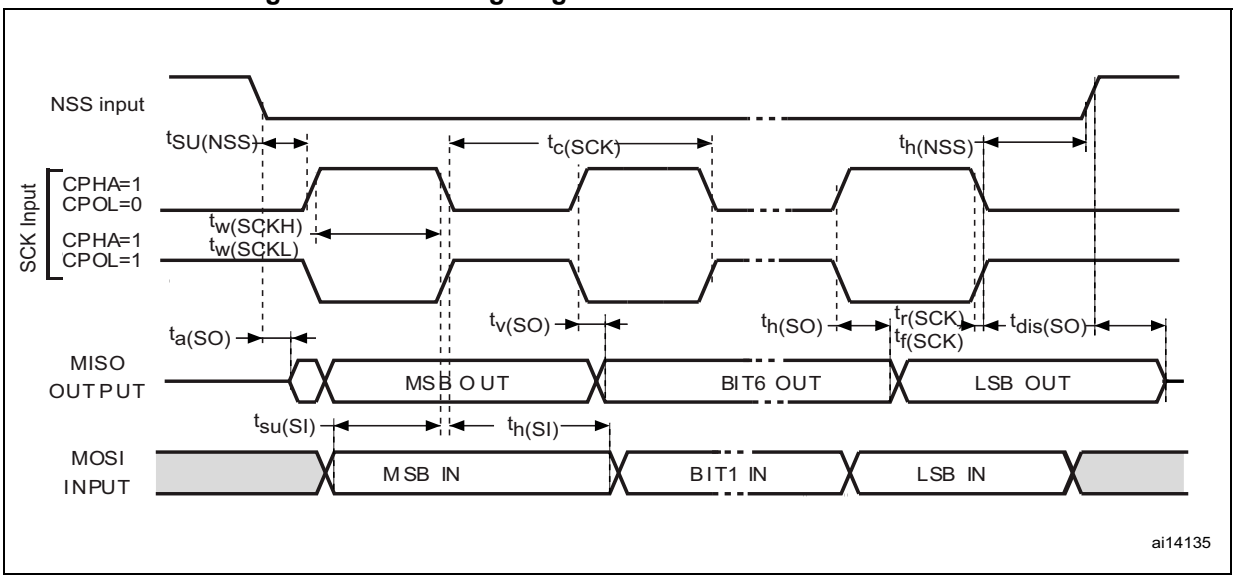
1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

**Table 68. Comparator 2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | - | 3.6 | V |
| $V_{IN}$ | Comparator 2 input voltage range | - | 0 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | Fast mode | - | 15 | 20 | µs |
| | | Slow mode | - | 20 | 25 | |
| $t_{d\ slow}$ | Propagation delay(2) in slow mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 1.8 | 3.5 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 2.5 | 6 | |
| $t_{d\ fast}$ | Propagation delay(2) in fast mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 0.8 | 2 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 1.2 | 4 | |
| $V_{offset}$ | Comparator offset error | | - | ±4 | ±20 | mV |
| dThreshold/ dt | Threshold voltage temperature coefficient | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C, V- = $V_{REFINT}$, 3/4 $V_{REFINT}$, 1/2 $V_{REFINT}$, 1/4 $V_{REFINT}$. | - | 15 | 30 | ppm /°C |
| $I_{COMP2}$ | Current consumption(3) | Fast mode | - | 3.5 | 5 | µA |
| | | Slow mode | - | 0.5 | 2 | |

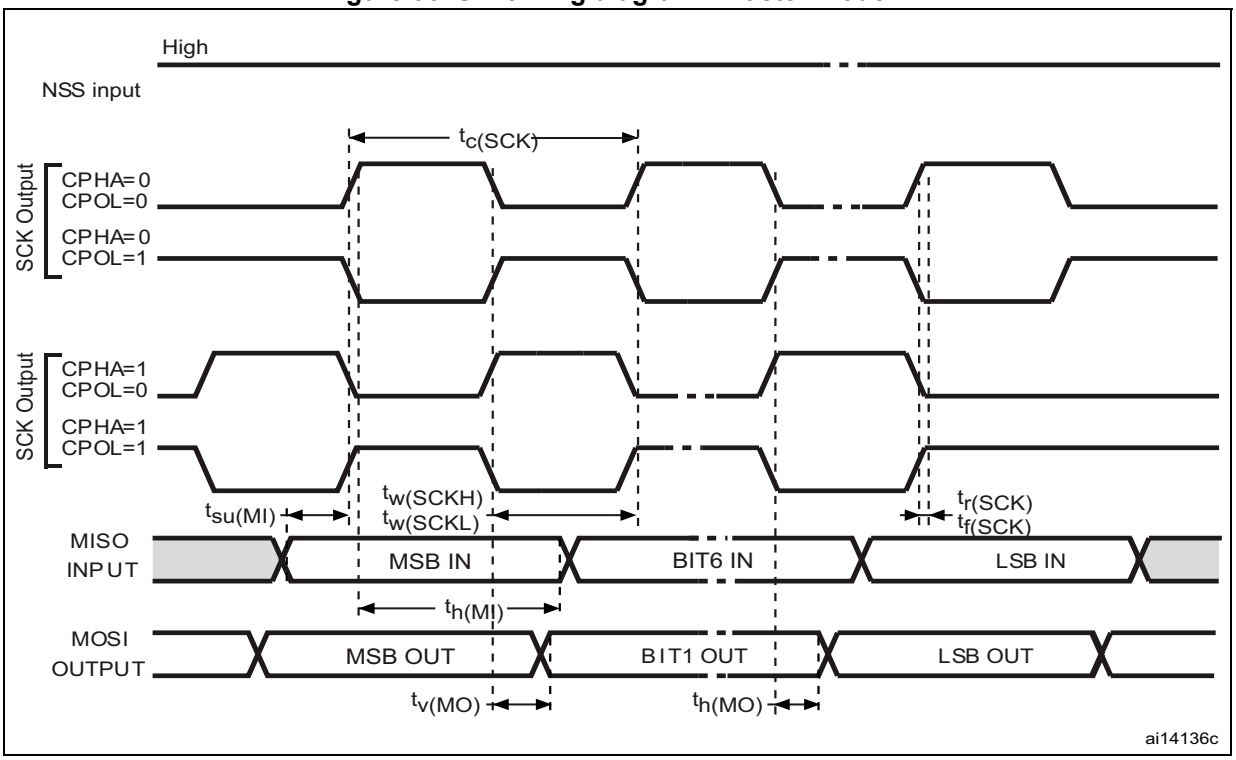
1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

**Figure 35. SPI timing diagram - slave mode and CPHA = 1(1)**



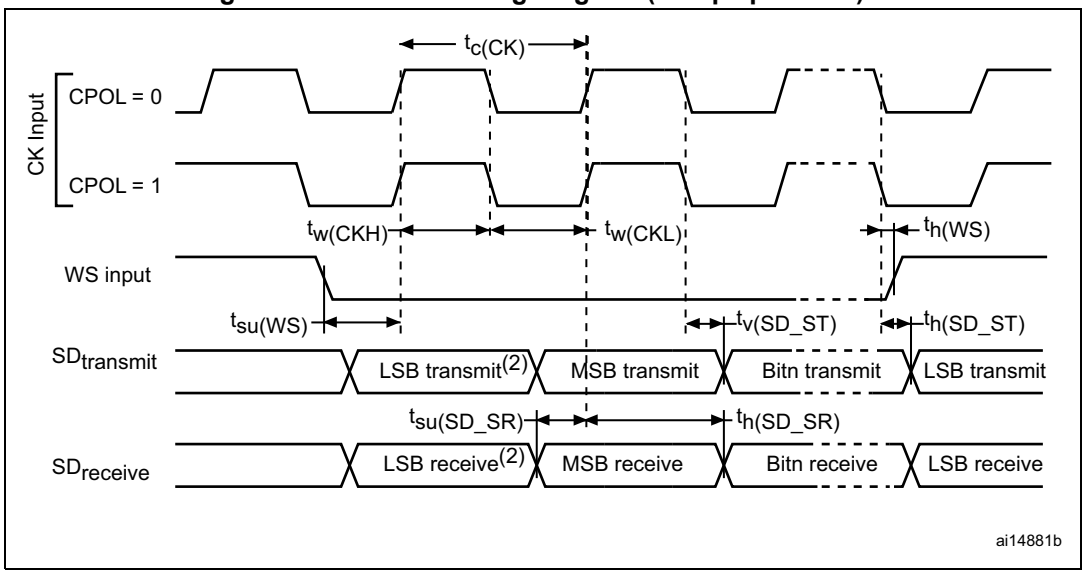

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 36. SPI timing diagram - master mode(1)**



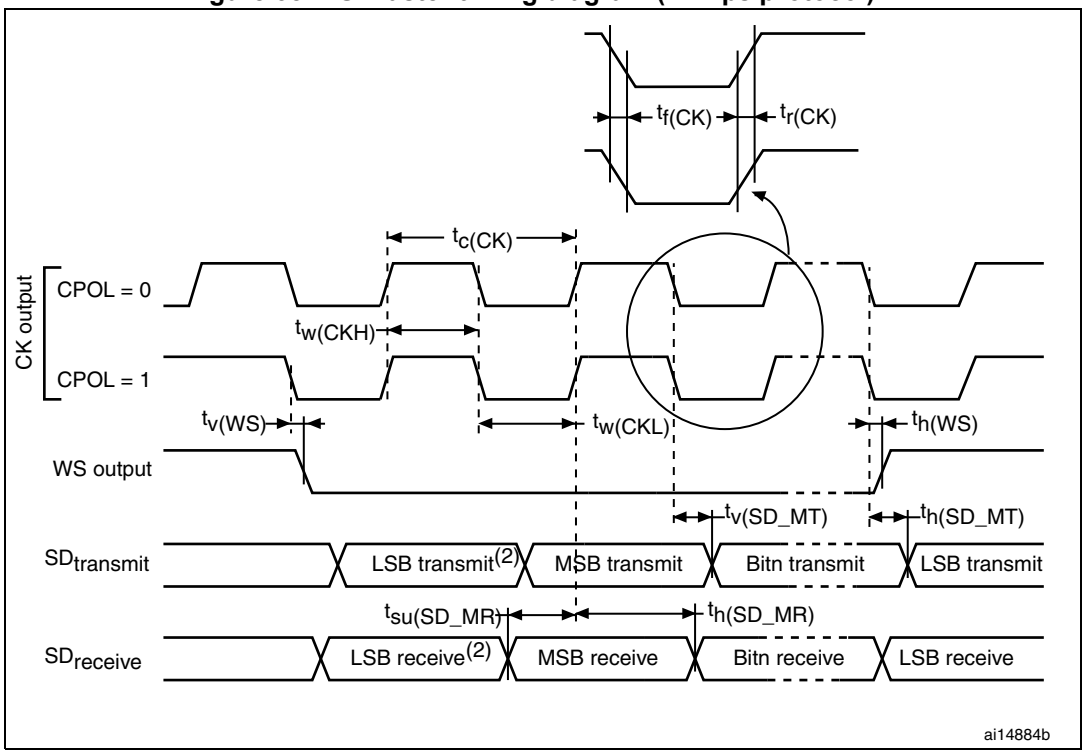

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 37. I²S slave timing diagram (Philips protocol)(1)**




1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

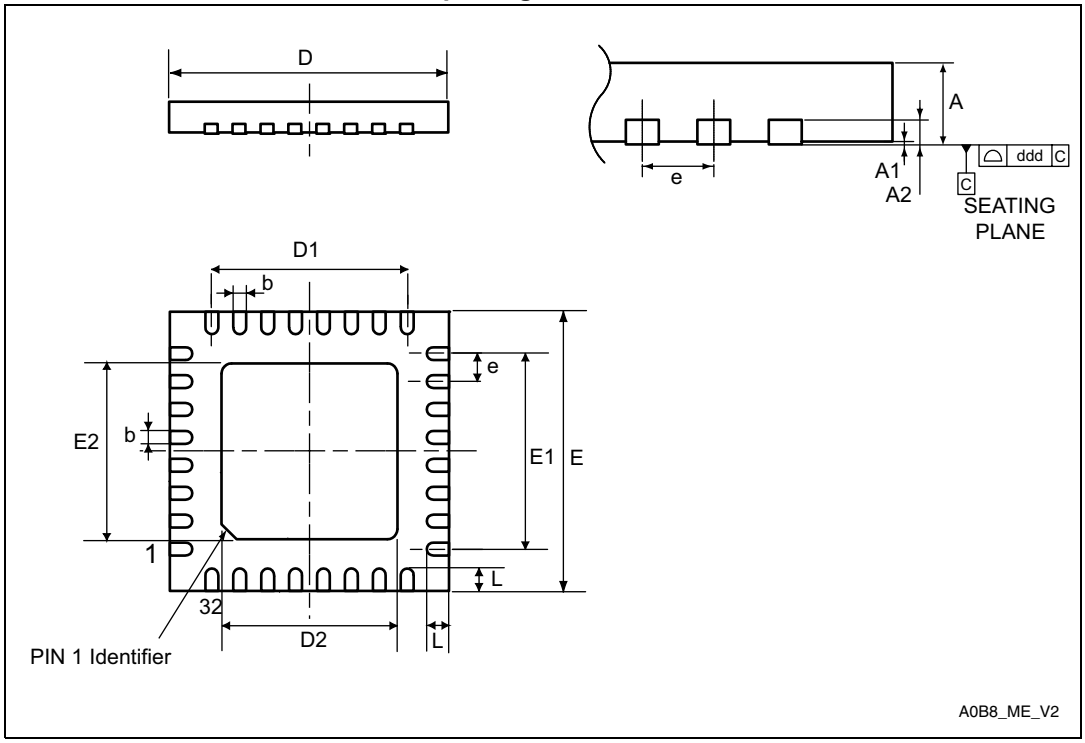
**Figure 38. I²S master timing diagram (Philips protocol)(1)**




1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

## 7.8 UFQFPN32 package information

**Figure 59. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline**



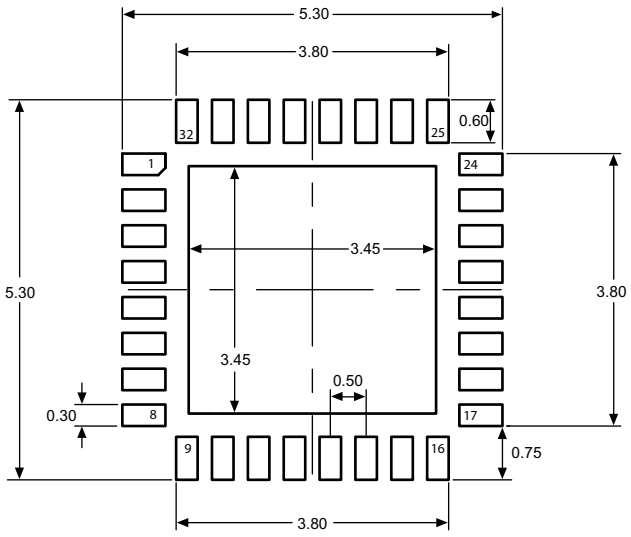

1. Drawing is not to scale.

**Table 86. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.0060 | - |
| b | 0.180 | 0.230 | 0.280 | 0.0071 | 0.0091 | 0.0110 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| D1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| D2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| E1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 60. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint**




1. Dimensions are expressed in millimeters.