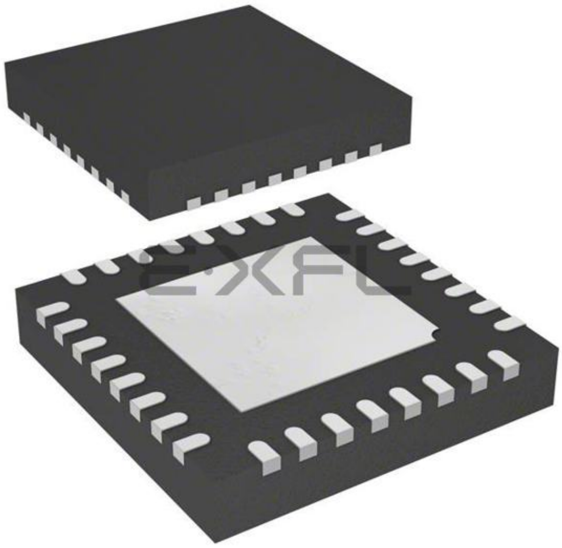

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071kbu3

2.1 Device overview

Table 2. Ultra-low-power STM32L071xx device features and peripheral counts

Peripheral		STM32L 071K8	STM32L 071C8	STM32L 071V8	STM32L 071KB	STM32L 071CB	STM32L 071VB	STM32L 071RB	STM32L 071KZ	STM32L 071CZ	STM32L 071VZ	STM32L 071RZ
Flash (Kbytes)		64 Kbytes			128 Kbytes				192 Kbytes			
Data EEPROM (Kbytes)		3 Kbytes			6 Kbytes							
RAM (Kbytes)		20 Kbytes										
Timers	General-purpose	4										
	Basic	2										
	LPTIMER	1										
RTC/SYSTICK/IWDG /WWDG		1/1/1/1										
Com. interfaces	SPI/I2S	4(3)[1]/0	6(4)[2]/1		4(3)[1]/0	6(4)[2]/1			4(3)[1]/0	6(4)[2]/1		
	I^2C	2	3		2	3			2	3		
	USART	3	4		3	4			3	4		
	LPUART	1										
GPIOs		23	37	84	25[3]	40[4]	84	51[5]	25[3]	40[4]	84	51[5]
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1										
12-bit synchronized ADC Number of channels		1 10	1 13	1 16	1 10	1 13[4]	1 16	1 16[5]	1 10	1 13[4]	1 16	1 16[5]
Comparators		2										
Max. CPU frequency		32 MHz										
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option										
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C										
Packages		UFQFPN 32	LQFP48	LQFP/ UFBGA 100	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64

1. 3 SPI interfaces are USARTs operating in SPI master mode.
2. 4 SPI interfaces are USARTs operating in SPI master mode.
3. UFQFPN32 has 2 GPIOs less than LQFP32.
4. LQFP48 has three GPIOs less than WLCSP49.
5. TFBGA64 has one GPIO, one ADC input less than LQFP64.

internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**

  To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**

  Clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management**

  To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**

  Three different clock sources can be used to drive the master clock SYSCLK:
  - 1-25 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLLMultispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**

  Two ultra-low-power clock sources that can be used to drive the real-time clock:

3.15 Communication interfaces

3.15.1 I²C bus

Up to three I²C interfaces (I2C1 and I2C3) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 10. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 and I2C3 provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1/I2C3 also have a clock domain independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

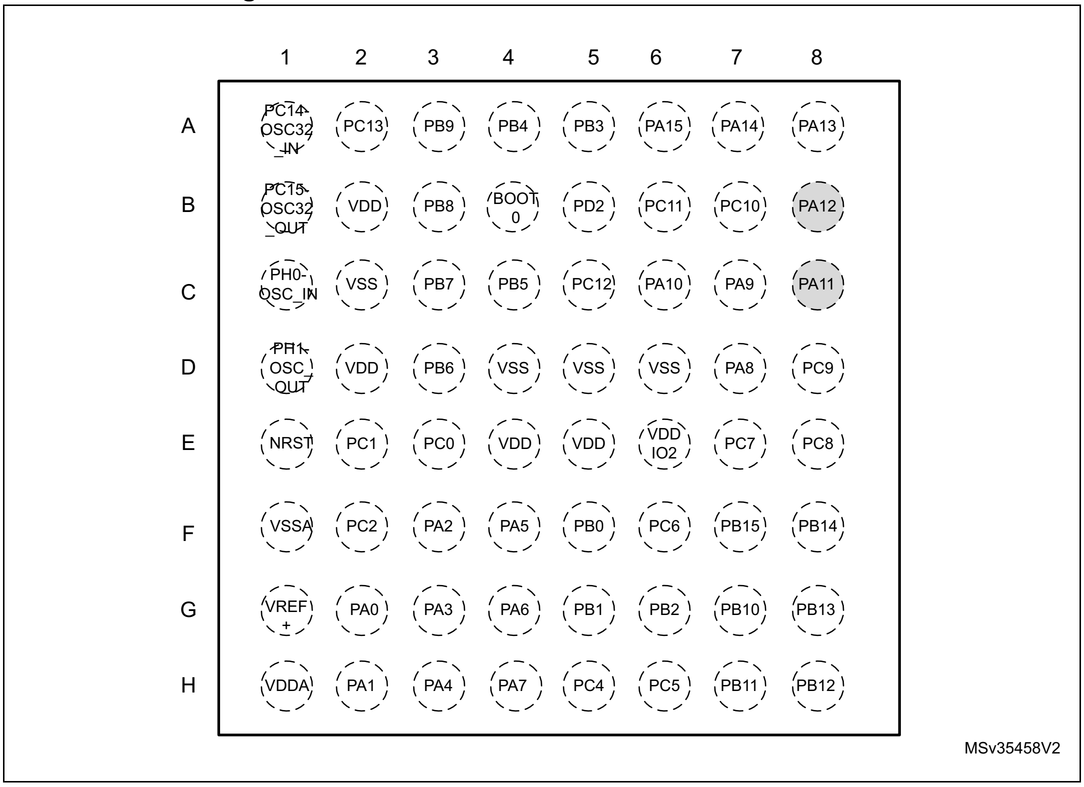
Refer to *Table 11* for an overview of I2C interface features.

Table 11. STM32L071xx I²C implementation

I2C features[1]	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X[2]	X
Independent clock	X	-	X
SMBus	X	-	X
Wakeup from STOP	X	-	X

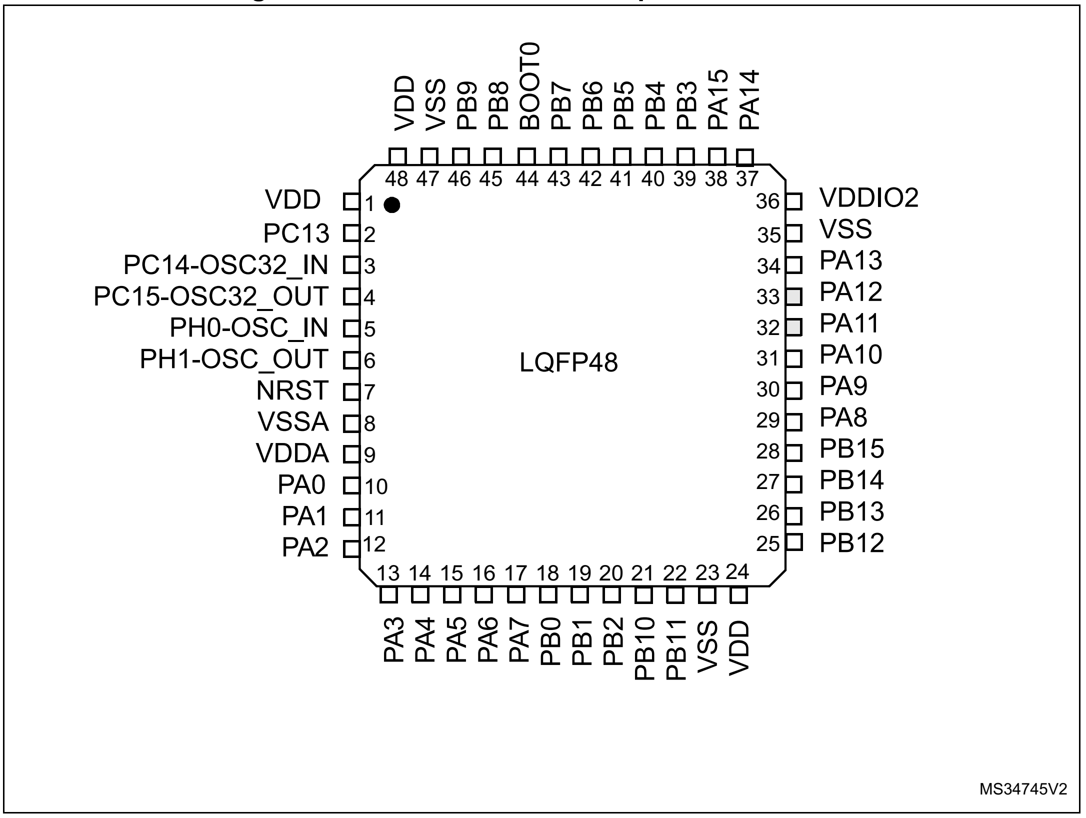
1. X = supported.
2. See *Table 15: STM32L071xxx pin definition on page 39* for the list of I/Os that feature Fast Mode Plus capability

Figure 6. STM32L071xx TFBGA64 ballout - 5x 5 mm



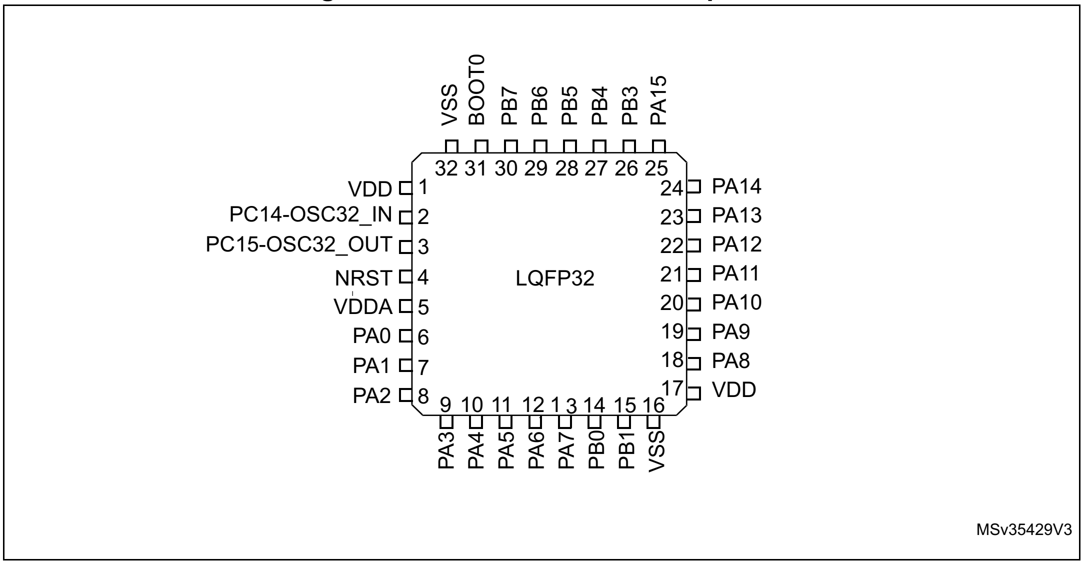
1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Figure 8. STM32L071xx LQFP48 pinout - 7 x 7 mm



1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Figure 9. STM32L071xx LQFP32 pinout



1. The above figure shows the package top view.

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[(1)]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
12	12	16	22	G4	G5	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM3_CH1, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
13	13	17	23	H4	F4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM3_CH2, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	-	-	24	H5	-	33	K5	PC4	I/O	FT	-	EVENTOUT, LPUART1_TX	ADC_IN14
-	-	-	25	H6	-	34	L5	PC5	I/O	FT	-	LPUART1_RX	ADC_IN15
14	14	18	26	F5	G4	35	M5	PB0	I/O	FT	-	EVENTOUT, TIM3_CH3	ADC_IN8, VREF_OUT
15	15	19	27	G5	D3	36	M6	PB1	I/O	FT	-	TIM3_CH4, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
-	-	20	28	G6	E3	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, I2C3_SMBA	-
-	-	-	-	-	-	38	M7	PE7	I/O	FT	-	USART5_CK/USART5_RTS_DE	-
-	-	-	-	-	-	39	L7	PE8	I/O	FT	-	USART4_TX	-
-	-	-	-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, TIM2_ETR, USART4_RX	-
-	-	-	-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, USART5_TX	-
-	-	-	-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	-
-	-	-	-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	-
-	-	-	-	-	-	44	M10	PE13	I/O	FT	-	SPI1_SCK	-
-	-	-	-	-	-	45	M11	PE14	I/O	FT	-	SPI1_MISO	-
-	-	-	-	-	-	46	M12	PE15	I/O	FT	-	SPI1_MOSI	-

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[(1)]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
30	29	43	59	C3	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	60	B4	A5	94	A4	BOOT0	I		-	-	-
-	-	45	61	B3	B5	95	A3	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	46	62	A3	A6	96	B3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	31	47	63	D4	-	99	D3	VSS	S		-	-	-
-	32	48	64	E4	A7	100	C4	VDD	S		-	-	-

1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.

Table 18. Alternate functions port C

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	I2C3/LPUART1/ COMP1/2/ TIM3
Port C	PC0	LPTIM1_IN1		EVENTOUT				LPUART1_RX	I2C3_SCL
	PC1	LPTIM1_OUT		EVENTOUT				LPUART1_TX	I2C3_SDA
	PC2	LPTIM1_IN2		SPI2_MISO/ I2S2_MCK					
	PC3	LPTIM1_ETR		SPI2_MOSI/ I2S2_SD					
	PC4	EVENTOUT		LPUART1_TX					
	PC5			LPUART1_RX					
	PC6	TIM22_CH1		TIM3_CH1					
	PC7	TIM22_CH2		TIM3_CH2					
	PC8	TIM22_ETR		TIM3_CH3					
	PC9	TIM21_ETR		TIM3_CH4					I2C3_SDA
	PC10	LPUART1_TX						USART4_TX	
	PC11	LPUART1_RX						USART4_RX	
	PC12			USART5_TX				USART4_CK	
	PC13								
	PC14								
	PC15								

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics*, and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 22. Voltage characteristics

Symbol	Definition	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DDIO2} V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	V_{DD}+4.0	
	Input voltage on TC pins	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0	V_{SS}	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$\|\Delta V_{DD}\|$	Variations between different V_{DDx} power pins	-	50	mV
$\|V_{DDA}$-$V_{DDx}\|$	Variations between any V_{DDx} and V_{DDA} power pins(3)	-	300	
$\|\Delta V_{SS}\|$	Variations between all different ground pins including V_{REF-} pin	-	50	
V_{REF+} –V_{DDA}	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		

1. All main power (V_{DD},, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 23* for maximum allowed injected current values.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation. V_{DDIO2} is independent from V_{DD} and V_{DDA}: its value does not need to respect this rule.

Figure 16. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS

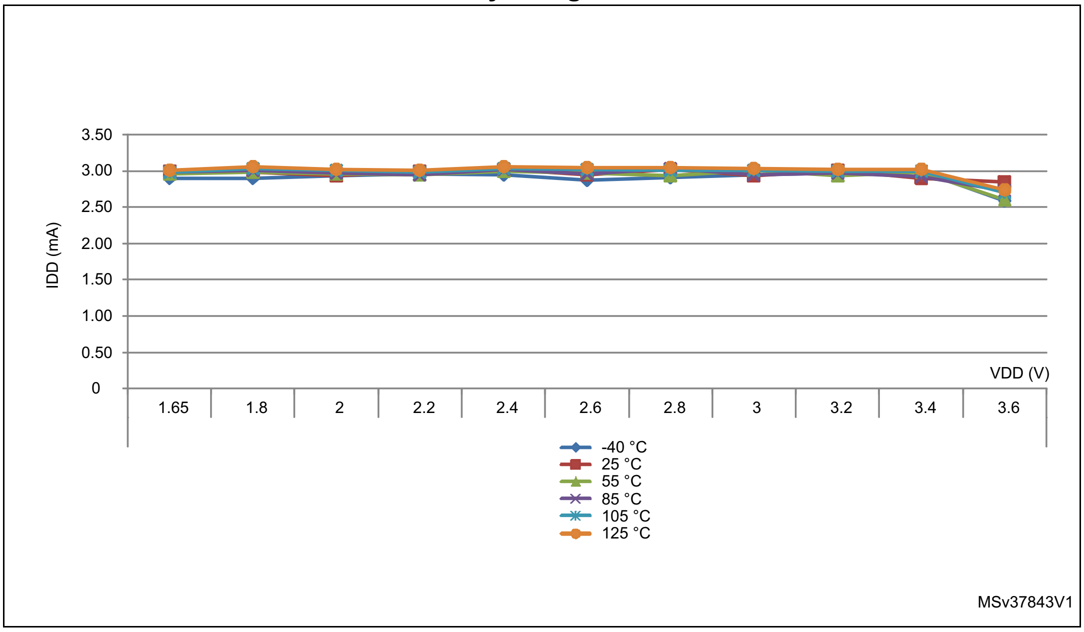


Figure 17. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS

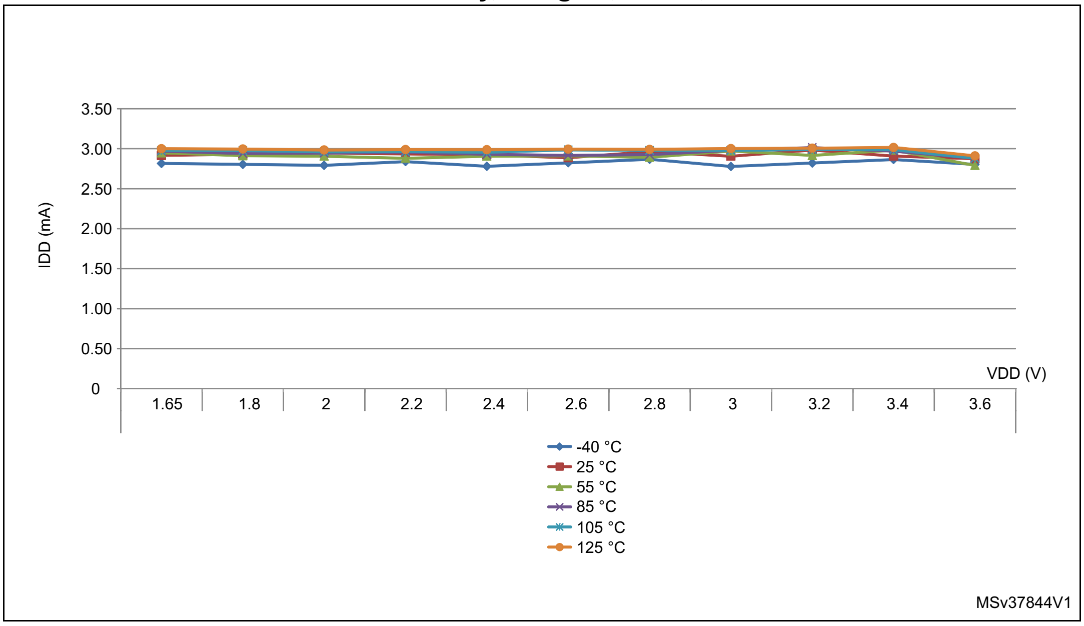


Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 53*. They are based on the EMS levels and classes defined in application note AN1709.

Table 53. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

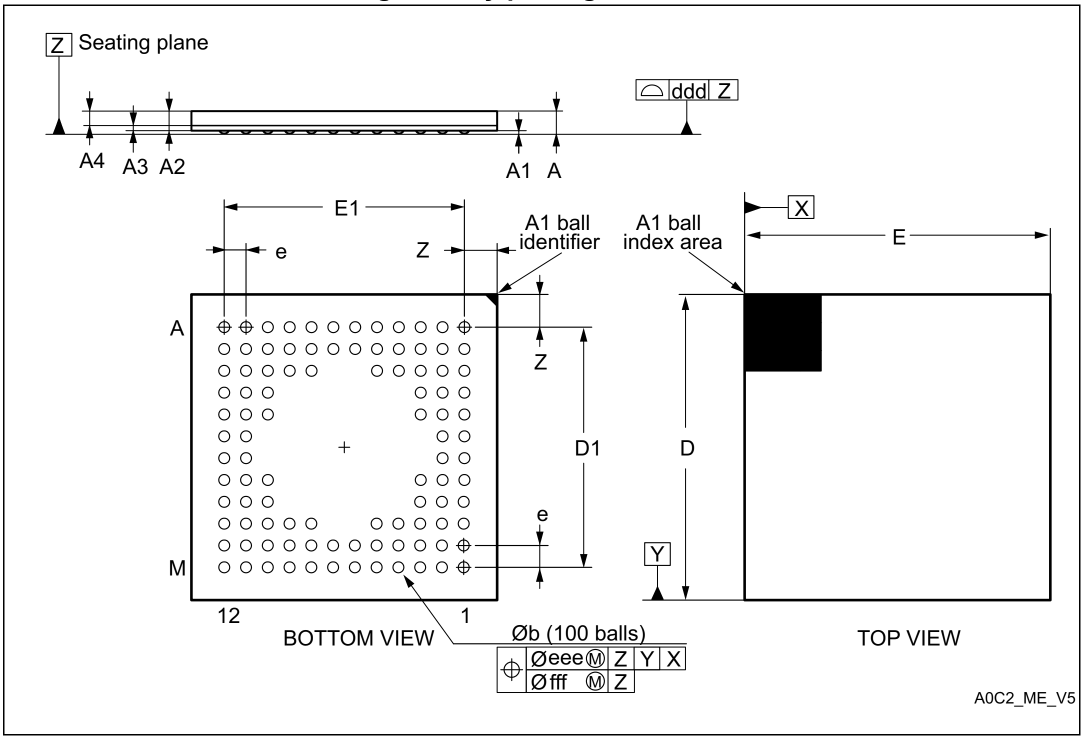
The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range at 32 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-7	dBµV
			30 to 130 MHz	14	
			130 MHz to 1 GHz	9	
			EMI Level	2	-

7.2 UFBGA100 package information

Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 77. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

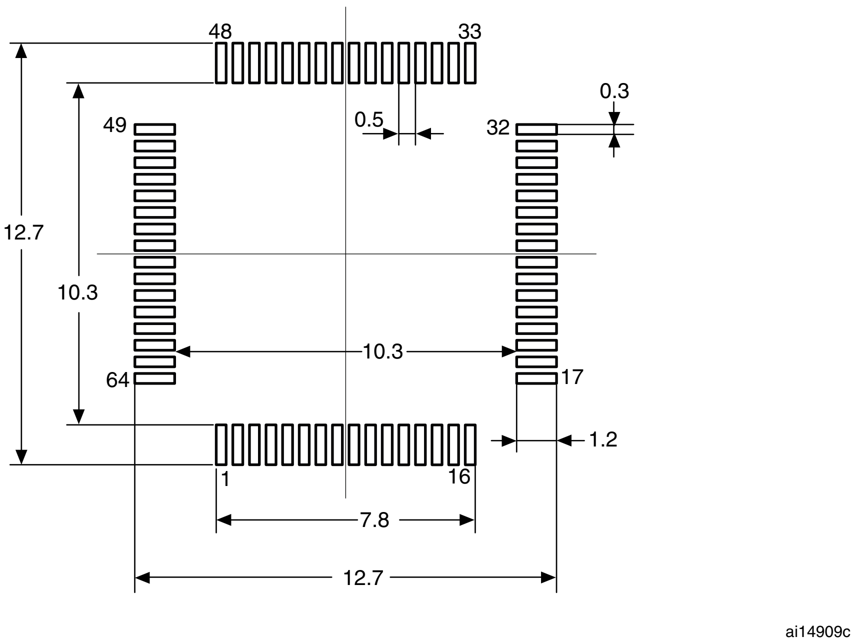
Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

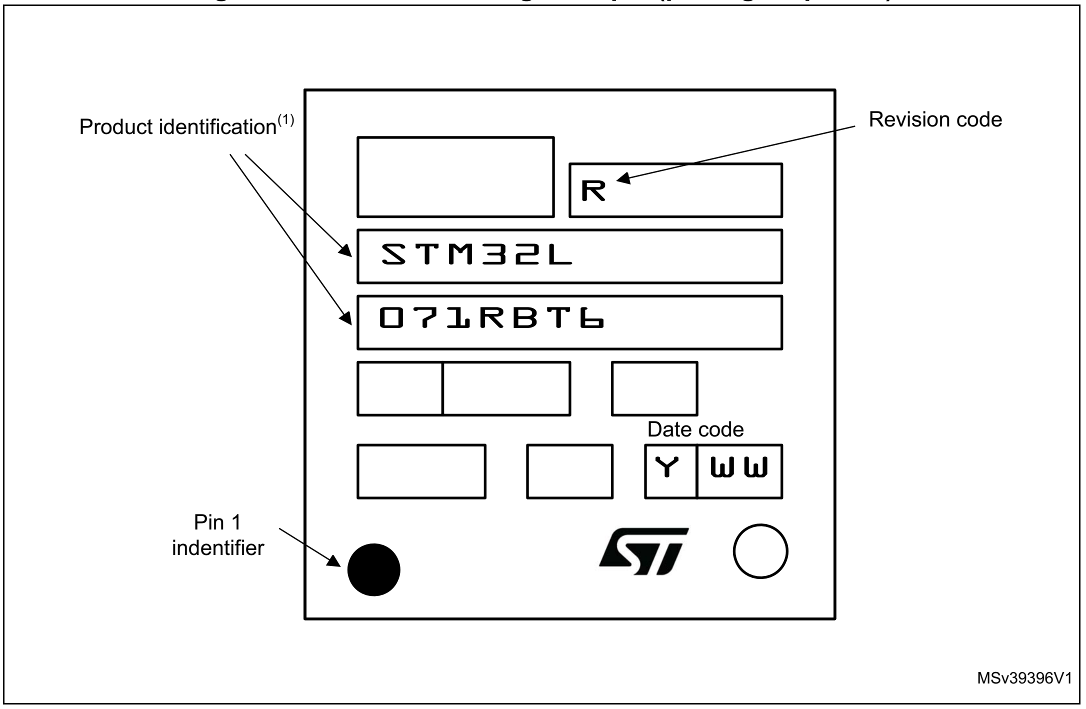


1. Dimensions are expressed in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 46. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 80. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball ,grid array recommended footprint

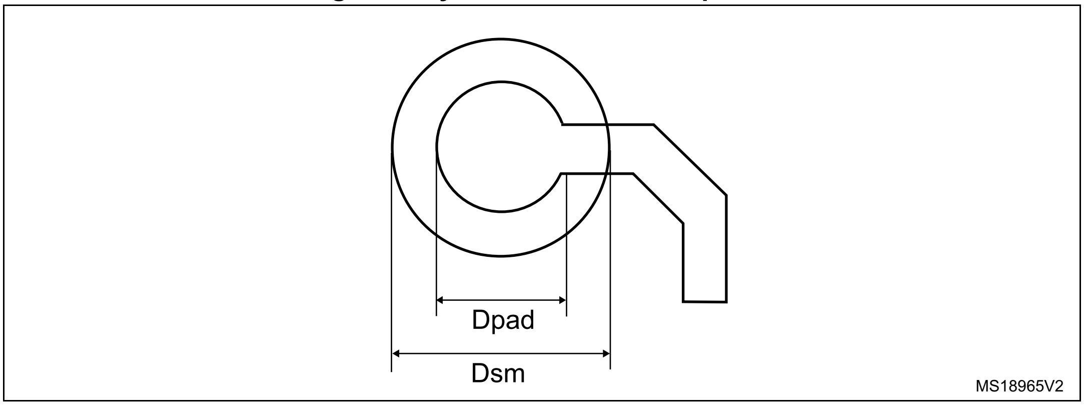


Table 81. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

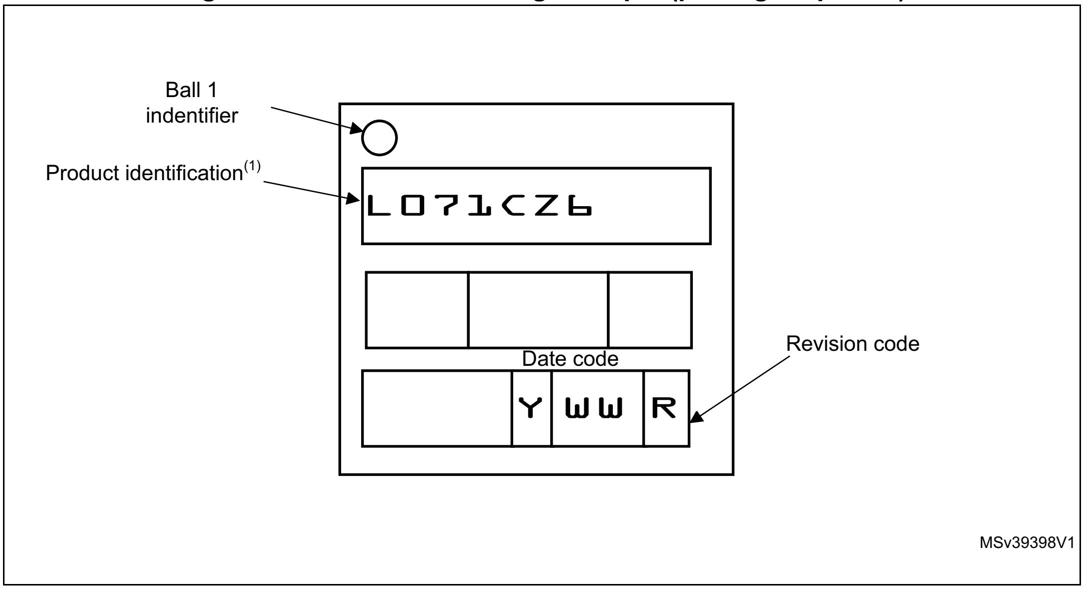
Table 83. WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Device marking for WLCSP49

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 52. WLCSP49 marking example (package top view)



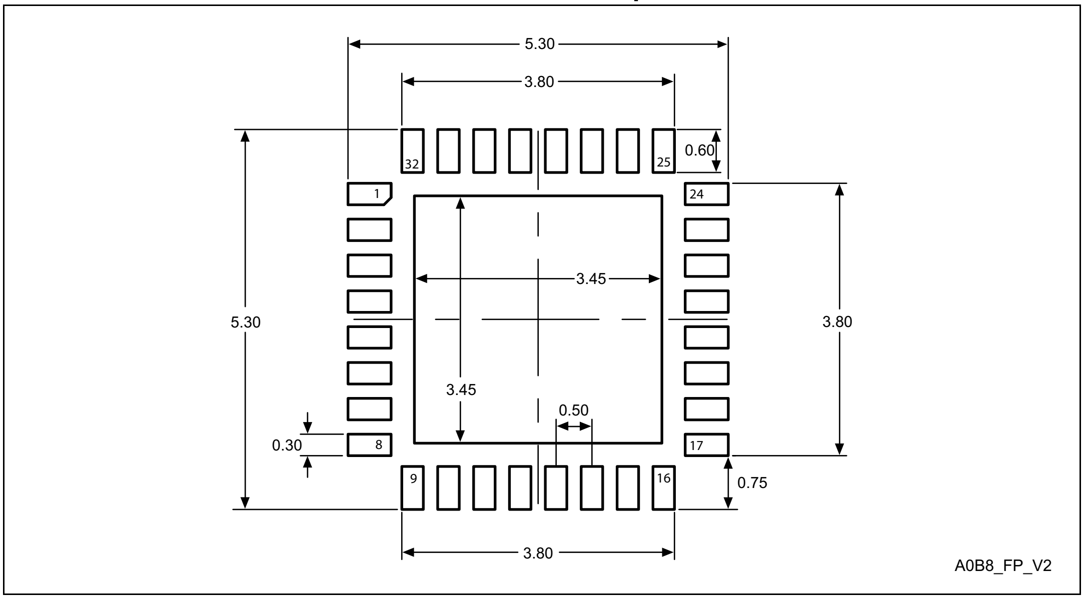
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 86. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

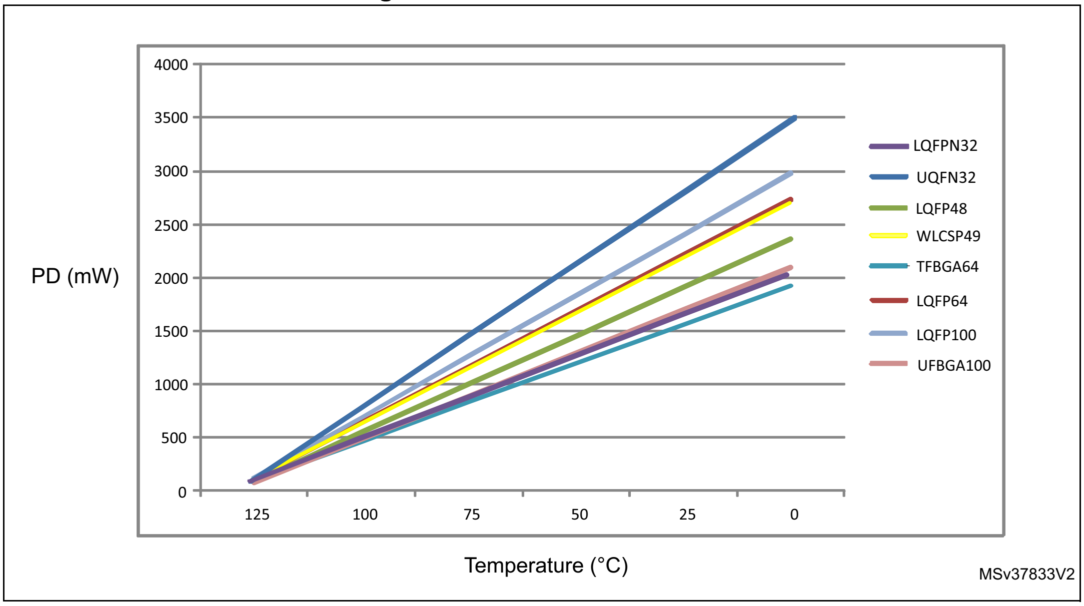
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 60. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Figure 62. Thermal resistance



7.9.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.