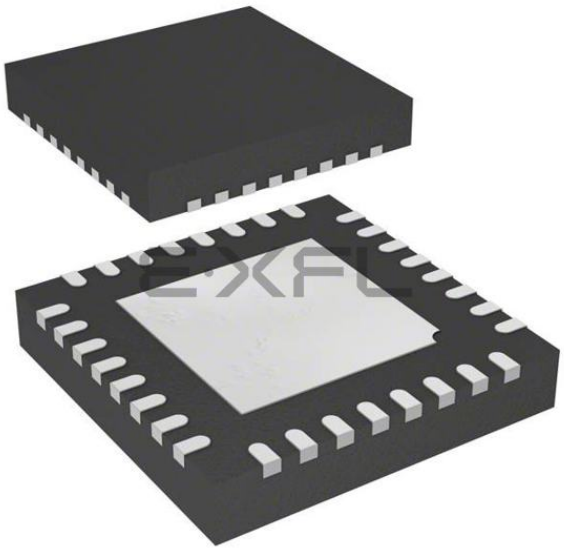

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071kbu3tr

Contents

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3.14 Timers and watchdogs

The ultra-low-power STM32L071xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

Table 9 compares the features of the general-purpose and basic timers.

Table 9. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.14.1 General-purpose timers (TIM2, TIM3, TIM21 and TIM22)

There are four synchronizable general-purpose timers embedded in the STM32L071xx device (see *Table 9* for differences).

TIM2, TIM3

TIM2 and TIM3 are based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2/TIM3 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2/TIM3 have independent DMA request generation.

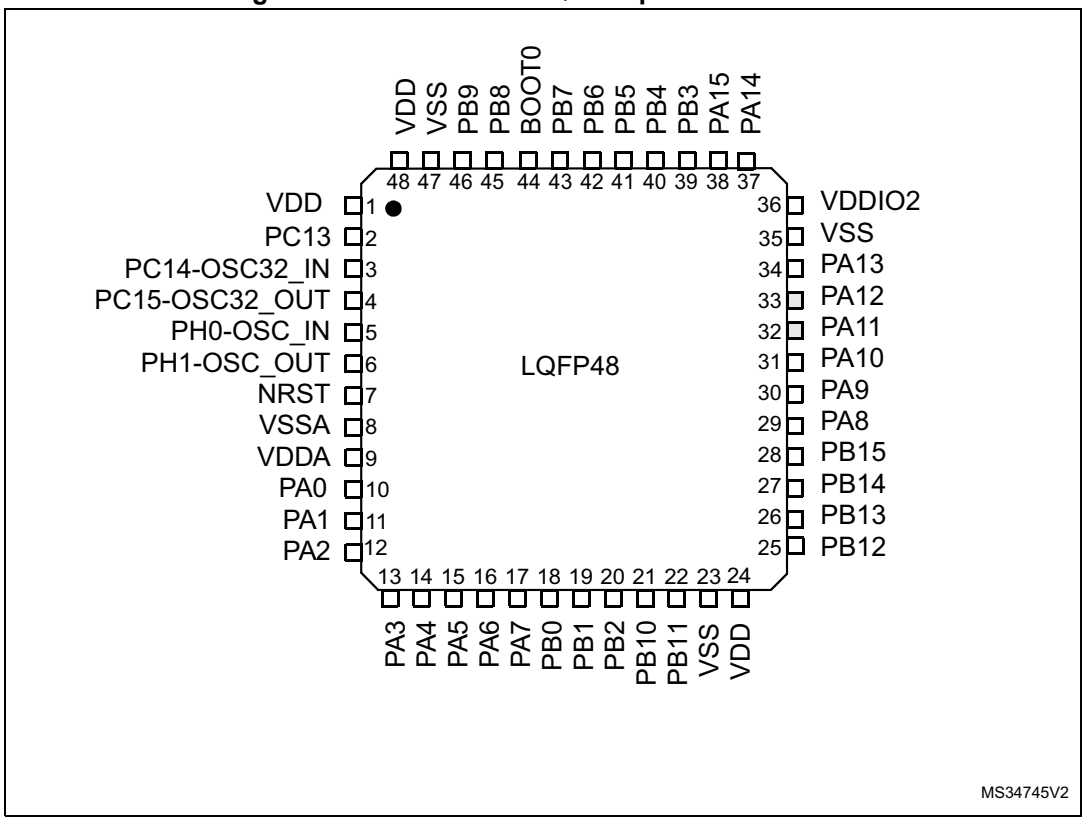
These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2/TIM3, full-featured general-purpose timers.

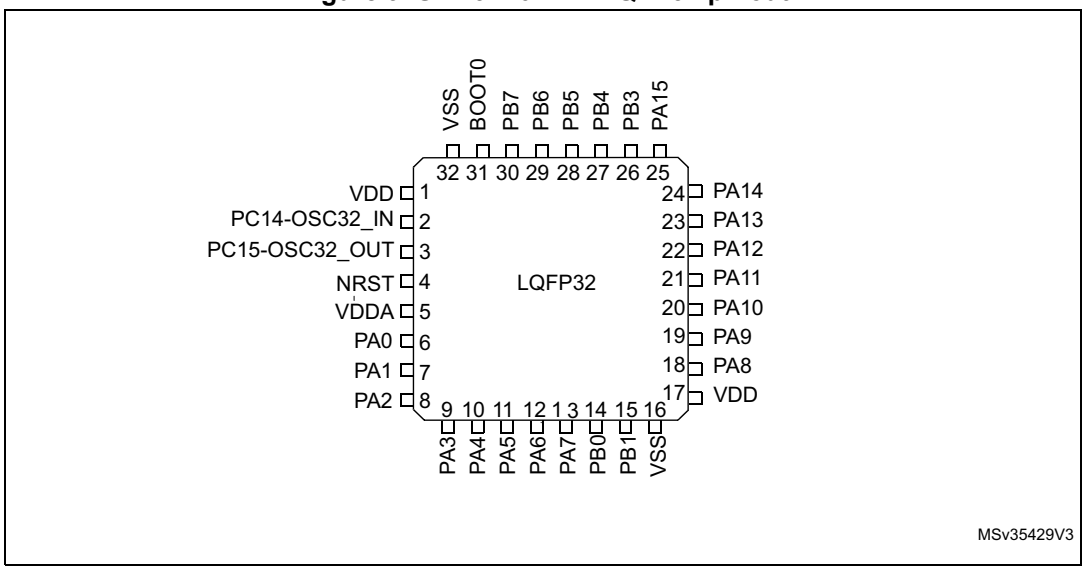
They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

Figure 8. STM32L071xx LQFP48 pinout - 7 x 7 mm



1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Figure 9. STM32L071xx LQFP32 pinout



1. The above figure shows the package top view.

Table 15. STM32L071xxx pin definition

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	1	B2	PE2	I/O	FT	-	TIM3_ETR	-
-	-	-	-	-	-	2	A1	PE3	I/O	FT	-	TIM22_CH1, TIM3_CH1	-
-	-	-	-	-	-	3	B1	PE4	I/O	FT	-	TIM22_CH2, TIM3_CH2	-
-	-	-	-	-	-	4	C2	PE5	I/O	FT	-	TIM21_CH1, TIM3_CH3	-
-	-	-	-	-	-	5	D2	PE6	I/O	FT	-	TIM21_CH2, TIM3_CH4	RTC_TAMP3/WKUP3
1	-	1	1	B2	B6	6	E2	VDD	S		-	-	-
-	-	2	2	A2	B7	7	C1	PC13	I/O	FT	-	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/WKUP2
2	1	3	3	A1	C6	8	D1	PC14-OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
3	2	4	4	B1	C7	9	E1	PC15-OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
-	-	-	-	-	-	10	F2	PH9	I/O	FT	-	-	-
-	-	-	-	-	-	11	G2	PH10	I/O	FT	-	-	-
-	-	5	5	C1	D6	12	F1	PH0-OSC_IN (PH0)	I/O	TC	-	-	OSC_IN
-	-	6	6	D1	D7	13	G1	PH1-OSC_OUT (PH1)	I/O	TC	-	-	OSC_OUT
4	3	7	7	E1	D5	14	H2	NRST	I/O	-	-	-	-
-	-	-	8	E3	C5	15	H1	PC0	I/O	FTf	-	LPTIM1_IN1, EVENTOUT, LPUART1_RX, I2C3_SCL	ADC_IN10
-	-	-	9	E2	C4	16	J2	PC1	I/O	FTf	-	LPTIM1_OUT, EVENTOUT, LPUART1_TX, I2C3_SDA	ADC_IN11
-	-	-	10	F2	E7	17	J3	PC2	I/O	FTf	-	LPTIM1_IN2, SPI2_MISO/I2S2_MCK	ADC_IN12

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
12	12	16	22	G4	G5	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM3_CH1, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
13	13	17	23	H4	F4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM3_CH2, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	-	-	24	H5	-	33	K5	PC4	I/O	FT	-	EVENTOUT, LPUART1_TX	ADC_IN14
-	-	-	25	H6	-	34	L5	PC5	I/O	FT	-	LPUART1_RX	ADC_IN15
14	14	18	26	F5	G4	35	M5	PB0	I/O	FT	-	EVENTOUT, TIM3_CH3	ADC_IN8, VREF_OUT
15	15	19	27	G5	D3	36	M6	PB1	I/O	FT	-	TIM3_CH4, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
-	-	20	28	G6	E3	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, I2C3_SMBA	-
-	-	-	-	-	-	38	M7	PE7	I/O	FT	-	USART5_CK/USART5_RTS_DE	-
-	-	-	-	-	-	39	L7	PE8	I/O	FT	-	USART4_TX	-
-	-	-	-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, TIM2_ETR, USART4_RX	-
-	-	-	-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, USART5_TX	-
-	-	-	-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	-
-	-	-	-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	-
-	-	-	-	-	-	44	M10	PE13	I/O	FT	-	SPI1_SCK	-
-	-	-	-	-	-	45	M11	PE14	I/O	FT	-	SPI1_MISO	-
-	-	-	-	-	-	46	M12	PE15	I/O	FT	-	SPI1_MOSI	-

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	39	E8	-	65	E10	PC8	I/O	FT	-	TIM22_ETR, TIM3_CH3	-
-	-	-	40	D8	-	66	D12	PC9	I/O	FTf	-	TIM21_ETR, TIM3_CH4, I2C3_SDA	-
18	18	29	41	D7	D1	67	D11	PA8	I/O	FTf	-	MCO, EVENTOUT, USART1_CK, I2C3_SCL	-
19	19	30	42	C7	E2	68	D10	PA9	I/O	FTf	-	MCO, USART1_TX, I2C1_SCL, I2C3_SMBA	-
20	20	31	43	C6	C1	69	C12	PA10	I/O	FTf	-	USART1_RX, I2C1_SDA	-
21	21	32	44	C8	D2	70	B12	PA11	I/O	FT	-	SPI1_MISO, EVENTOUT, USART1_CTS, COMP1_OUT	-
22	22	33	45	B8	B1	71	A12	PA12	I/O	FT	-	SPI1_MOSI, EVENTOUT, USART1_RTS_DE, COMP2_OUT	-
23	23	34	46	A8	C2	72	A11	PA13	I/O	FT	-	SWDIO, LPUART1_RX	-
-	-	-	-	-	-	73	C11	VDD	S		-	-	-
-	-	35	47	D5	-	74	F11	VSS	S		-	-	-
-	24	36	48	E5	A1	75	G11	VDDIO2	S		-	-	-
24	25	37	49	A7	B2	76	A10	PA14	I/O	FT	-	SWCLK, USART2_TX, LPUART1_TX	-
25	-	38	50	A6	A2	77	A9	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE	-
-	-	-	51	B7	-	78	B11	PC10	I/O	FT	-	LPUART1_TX, USART4_TX	-
-	-	-	52	B6	-	79	C10	PC11	I/O	FT	-	LPUART1_RX, USART4_RX	-
-	-	-	53	C5	-	80	B10	PC12	I/O	FT	-	USART5_TX, USART4_CK	-

Table 16. Alternate functions port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/USART1/2/LPUART1/LPTIM1/TIM2/21/22/EVENTOUT/SYS_AF	SPI1/SPI2/I2S2/I2C1/TIM2/21	SPI1/SPI2/I2S2/LPUART1/USART5/LPTIM1/TIM2/3/EVENTOUT/SYS_AF	I2C1/EVENTOUT	I2C1/USART1/2/LPUART1/TIM3/22/EVENTOUT	SPI2/I2S2/I2C2/USART1/TIM2/21/22	I2C1/2/LPUART1/USART4/UASRT5/TIM21/EVENTOUT	I2C3/LPUART1/COMP1/2/TIM3
Port A	PA0	-	-	TIM2_CH1		USART2_CTS	TIM2_ETR	USART4_TX	COMP1_OUT
	PA1	EVENTOUT		TIM2_CH2		USART2_RTS_DE	TIM21_ETR	USART4_RX	-
	PA2	TIM21_CH1		TIM2_CH3		USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2		TIM2_CH4		USART2_RX	-	LPUART1_RX	-
	PA4	SPI1_NSS	-	-		USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR			TIM2_CH1	-	-
	PA6	SPI1_MISO		TIM3_CH1		LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI		TIM3_CH2		-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO			EVENTOUT	USART1_CK	-	-	I2C3_SCL
	PA9	MCO		-		USART1_TX	-	I2C1_SCL	I2C3_SMBA
	PA10	-		-		USART1_RX	-	I2C1_SDA	-
	PA11	SPI1_MISO	-	EVENTOUT		USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT		USART1_RTS_DE	-	-	COMP2_OUT
	PA13	SWDIO	-		-	-	-	LPUART1_RX	-
	PA14	SWCLK	-	-	-	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS		TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	USART4_RTS_DE	-

Table 26. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 28* are based on characterization results, unless otherwise specified.

Table 27. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 28. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF

Table 38. Average current consumption during Wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I_{DD} (Wakeup from Stop)	Supply current during Wakeup from Stop mode	HSI	1	mA
		HSI/4	0,7	
		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I_{DD} (Reset)	Reset pin pulled down	-	0,21	
I_{DD} (Power-up)	BOR on	-	0,23	
I_{DD} (Wakeup from StandBy)	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Low-speed internal (LSI) RC oscillator

Table 47. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift 0°C ≤ T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 48. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤ T_A ≤ 85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤ T_A ≤ 110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤ V_{DD} ≤ 3.6 V, T_A = 25 °C	-	-	2.5	%/V

Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.18 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 69* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 69. TIMx characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

6.3.19 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

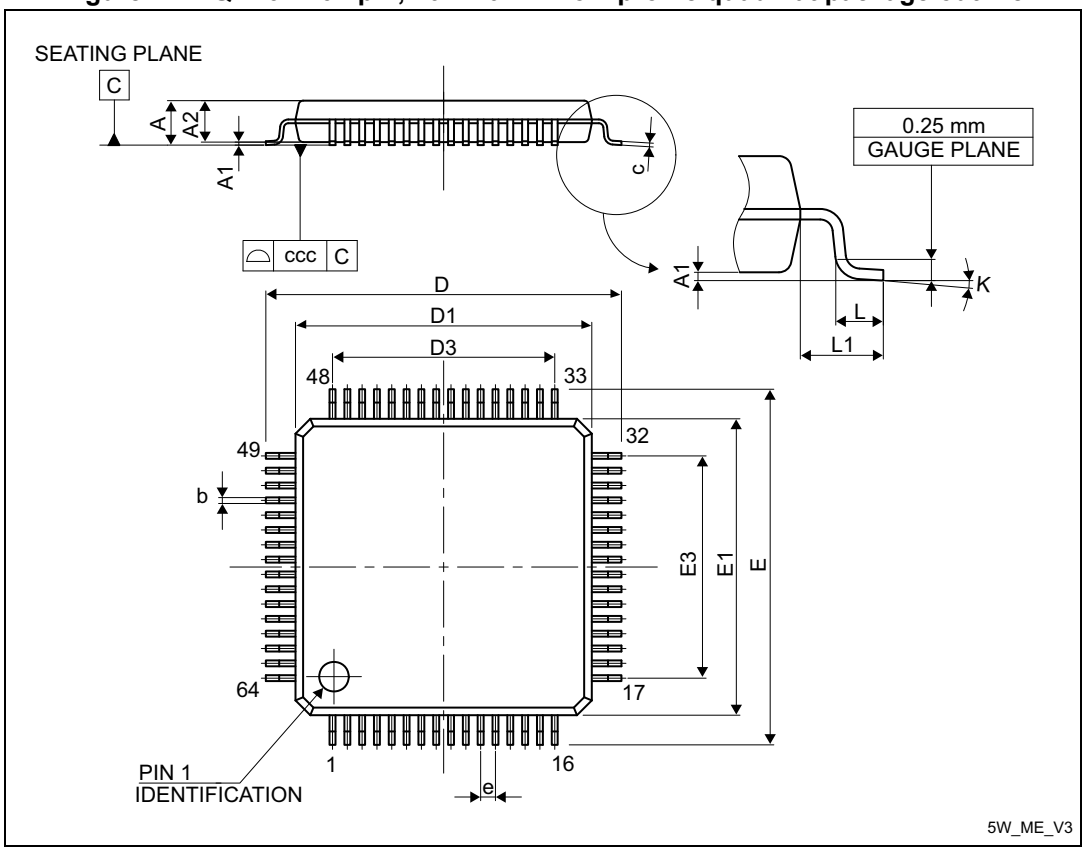
- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I^2C timing requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I^2C SDA and SCL I/Os embed an analog filter (see *Table 70* for the analog filter characteristics).

7.3 LQFP64 package information

Figure 44. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

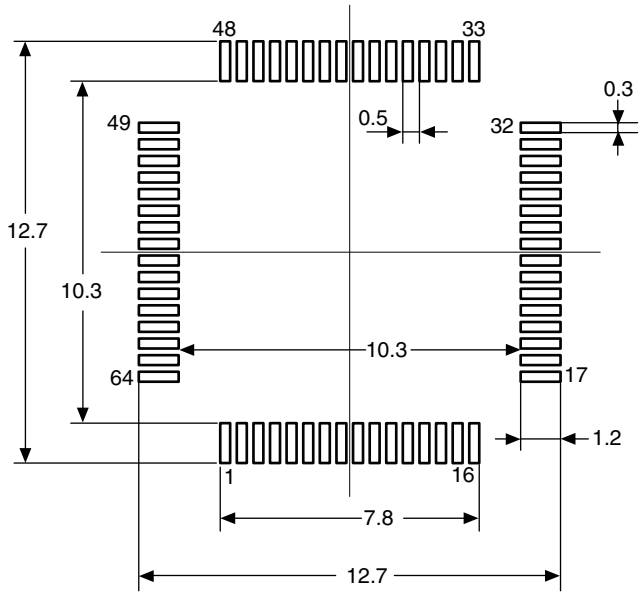
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

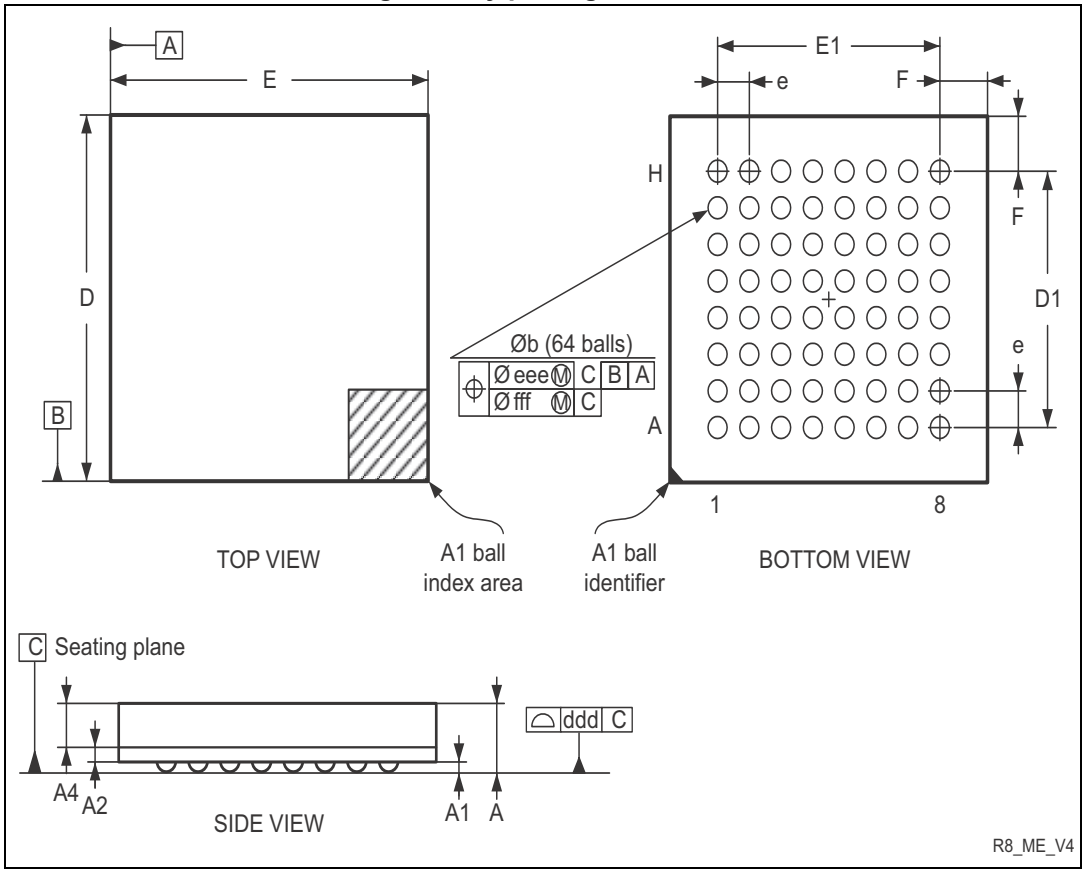
Figure 45. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

7.4 TFBGA64 package information

Figure 47. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline



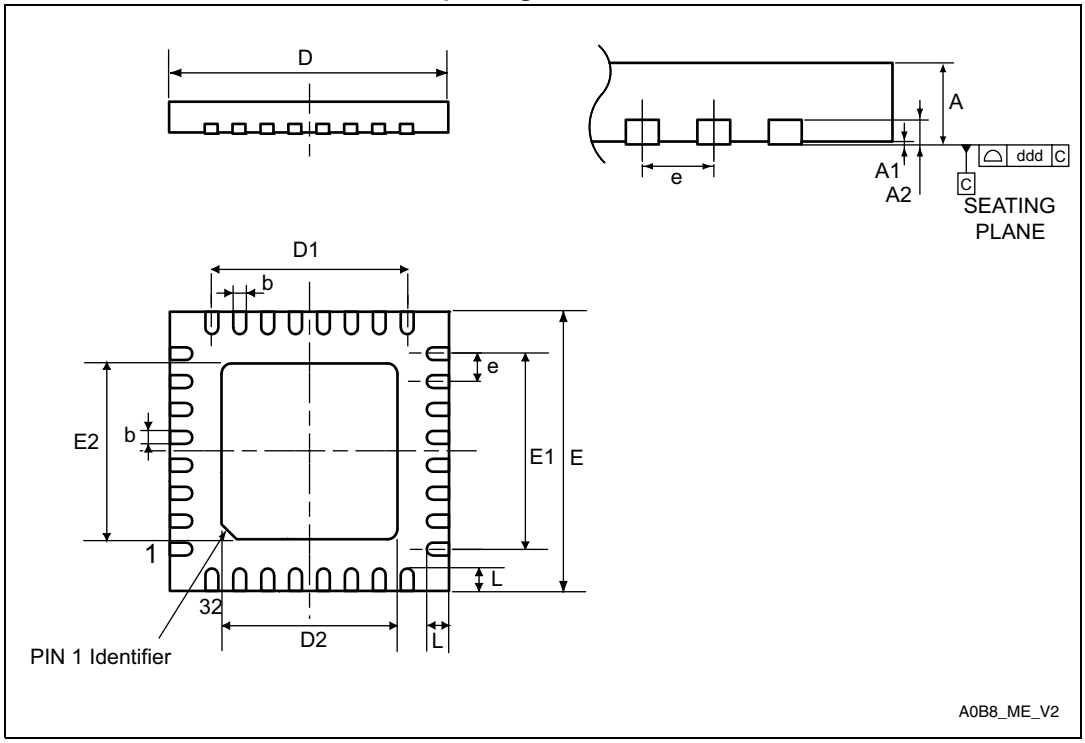
1. Drawing is not to scale.

Table 80. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-

7.8 UFQFPN32 package information

Figure 59. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

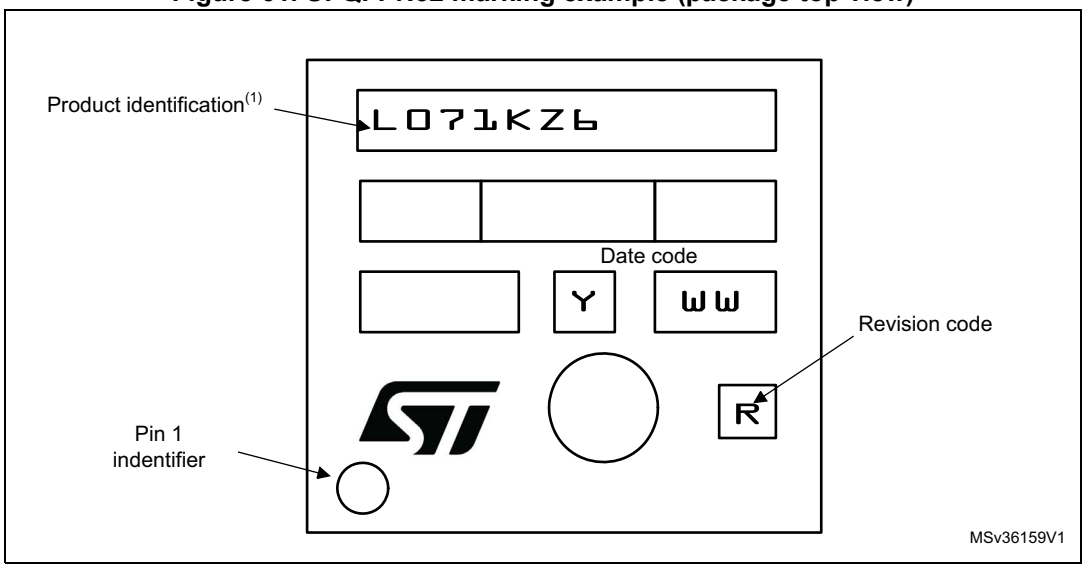


1. Drawing is not to scale.

Device marking for UFQFPN32

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 61. UFQFPN32 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

9 Revision history

Table 89. Document revision history

Date	Revision	Changes
02-Sep-2015	1	Initial release
26-Oct-2015	2	Changed confidentiality level to public. Updated datasheet status to “production data”. Modified ultra-low-power platform features on cover page. In *Table 15: STM32L071xxx pin definition*: – changed pin name to VDDIO2 for the following pins: UFQFPN32 pin 24, LQFP48 pin 36, LQFP64 pin 48, UFBGA64 pin E5, WLCSP49 pin A1, LQFP100 pin 75 and UFBGA100 pin G11. – Added note related to UFQFPN32. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated $\lvert\Delta V_{SS}\rvert$ definition to include V_{REF-} in *Table 22: Voltage characteristics*. Updated f_{TRIG} and V_{AIN} maximum value, added V_{REF+} and V_{REF-} in *Table 62: ADC characteristics*. Added *Section : Device marking for LQFP100*. Updated *Figure 42: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 76: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*. Added *Section : Device marking for LQFP100*, *Section : Device marking for LQFP64*, *Section : Device marking for TFBGA64* and *Section : Device marking for WLCSP49*. Updated *Figure 55: LQFP48 marking example (package top view)*.