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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071kbu6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 1. STM32L071xx block diagram

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L071xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

• Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

Low-power run mode

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the lowspeed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Lowpower run mode, the clock frequency and the number of enabled peripherals are both limited.

Low-power sleep mode

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

Stop mode with RTC

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in $3.5 \,\mu$ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.



			Low-	Low-	Stop		5	Standby
IPs	Run/Active	Sleep	power run	power sleep		Wakeup capability		Wakeup capability
High Speed External (HSE)	0	О	0	0				
Low Speed Internal (LSI)	0	О	0	0	0		0	
Low Speed External (LSE)	0	О	0	0	0		0	
Multi-Speed Internal (MSI)	0	О	Y	Y				
Inter-Connect Controller	Y	Y	Y	Y	Y			
RTC	0	0	0	0	0	0	0	
RTC Tamper	0	0	0	0	0	0	0	0
Auto WakeUp (AWU)	0	0	0	0	0	0	0	0
USART	0	0	0	0	O ⁽⁴⁾	0		
LPUART	0	0	0	0	O ⁽⁴⁾	0		
SPI	0	0	0	0				
I2C	0	0	0	0	O ⁽⁵⁾	0		
ADC	0	0						
Temperature sensor	Ο	О	О	Ο	0			
Comparators	0	0	0	0	0	0		
16-bit timers	0	0	0	0				
LPTIMER	0	0	0	0	0	0		
IWDG	0	0	0	0	0	0	0	0
WWDG	0	0	0	0				
SysTick Timer	0	0	0	0				
GPIOs	0	0	0	0	0	0		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs		3.5 µs		50 µs

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)⁽¹⁾⁽²⁾



internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, V_{POR/PDR} or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the startup time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.5 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

Clock prescaler

To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

Safe clock switching

Clock sources can be changed safely on the fly in Run mode through a configuration register.

• Clock management

To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

• System clock source

Three different clock sources can be used to drive the master clock SYSCLK:

- 1-25 MHz high-speed external crystal (HSE), that can supply a PLL
- 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLLMultispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

Auxiliary clock source

Two ultra-low-power clock sources that can be used to drive the real-time clock:



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 84 GPIOs can be connected to the 16 configurable interrupt/event lines. The 13 other lines are connected to PVD, RTC, USARTs, I2C, LPUART, LPTIMER or comparator events.



3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, LPUART, general-purpose timers, and ADC.

3.11 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L071xx device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 μ A at 10 kSPS, ~240 μ A at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.12 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.



3.14 Timers and watchdogs

The ultra-low-power STM32L071xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

Table 9 compares the features of the general-purpose and basic timers.

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table	9.	Timer	feature	comparison
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3.14.1 General-purpose timers (TIM2, TIM3, TIM21 and TIM22)

There are four synchronizable general-purpose timers embedded in the STM32L071xx device (see *Table 9* for differences).

TIM2, TIM3

TIM2 and TIM3 are based on 16-bit auto-reload up/down counter. It includes a 16-bit prescaler. It features four independent channels each for input capture/output compare, PWM or one-pulse mode output.

The TIM2/TIM3 general-purpose timers can work together or with the TIM21 and TIM22 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2/TIM3 have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2/TIM3, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.



		I	Pin n	umb	er								
LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
30	29	43	59	C3	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	60	B4	A5	94	A4	BOOT0	I		-	-	-
-	-	45	61	B3	B5	95	A3	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	46	62	A3	A6	96	В3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	31	47	63	D4	-	99	D3	VSS	S		-	-	-
-	32	48	64	E4	A7	100	C4	VDD	S		-	-	-

Table 15. STM32L071xxx	pin definition	(continued)
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1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.





Figure 20. I_{DD} vs V_{DD} , at T_A = 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off

Table 37. T	vpical and	maximum	current	consum	ntions i	n Standb	v mode
	ypical allu	maximum	current	consum	puonsi	II Stanub	y moue

Symbol	Parameter	Conditi	ons	Тур	Max ⁽¹⁾	Unit
I _{DD}			$T_A = -40 \text{ to } 25^{\circ}\text{C}$	0,855	1,70	
			T _A = 55 °C	-	2,90	
		Independent watchdog and LSI enabled	T _A = 85 °C	-	3,30	- - μΑ -
	Supply current in Standby mode		T _A = 105 °C	-	4,10	
			T _A = 125 °C	-	8,50	
(Standby)			T _A = − 40 to 25°C	0,29	0,60	
			T _A = 55 °C	0,32	1,20	
		Independent watchdog and LSI off	T _A = 85 °C	0,5	2,30	
			T _A = 105 °C	0,94	3,00	
			T _A = 125 °C	2,6	7,00	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified



		Typical consumption, V _{DD} = 3.0 V, T _A = 25 °C						
Per	ipheral	Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	Low-power sleep and run	Unit		
	GPIOA	3.5	3	2.5	2.5			
Cortex- M0+ core I/O port	GPIOB	3.5	2.5	2	2.5			
	GPIOC	8.5	6.5	5.5	7	µA/MHz		
	GPIOD	1	0.5	0.5	0.5	(f _{HCLK})		
	GPIOE	8	6	5	6			
	GPIOH	1.5	1	1	0.5			
	CRC	1.5	1	1	1			
AHB	FLASH	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	µA/MHz		
	DMA1	10	8	6.5	8.5	VIICLK/		
All e	enabled	204	162	130	202	µА/МНz (f _{HCLK})		
F	PWR	2.5	2	2	1	µA/MHz (f _{HCLK})		

Table 39. Peripheral current consumption in Run or Sleep mode(1) (continu

 Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.

2. HSI oscillator is off for this measure.

3. Current consumption is negligible and close to 0 $\mu A.$



6.3.7 Internal clock source characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

High-speed internal 16 MHz (HSI16) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI16}	Frequency	V _{DD} = 3.0 V	-	16	-	MHz
(1)(2)	HSI16 user-	Trimming code is not a multiple of 16	-	±0.4	0.7	%
TRIM	trimmed resolution	Trimming code is a multiple of 16	-	-	± 1.5	%
		V _{DDA} = 3.0 V, T _A = 25 °C	-1 ⁽³⁾	-	1 ⁽³⁾	%
		V_{DDA} = 3.0 V, T_{A} = 0 to 55 °C	-1.5	-	1.5	%
ACC	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
(2)		V _{DDA} = 3.0 V, T _A = -10 to 85 °C	-2.5	-	2	%
		V _{DDA} = 3.0 V, T _A = -10 to 105 °C	-4	-	2	%
		$V_{DDA} = 1.65 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ to } 125 \text{ °C}$	-5.45	-	3.25	%
t _{SU(HSI16)} ⁽²⁾	HSI16 oscillator startup time	-	-	3.7	6	μs
I _{DD(HSI16)} ⁽²⁾	HSI16 oscillator power consumption	-	-	100	140	μA

Table 46. 16 MHz HSI16 oscillator characteristics

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Guaranteed by test in production.



Figure 25. HSI16 minimum and maximum value versus temperature



Symbol	Parameter	Conditions	Min	Тур	Max ⁽¹⁾	Unit
	Average current during the whole programming / erase operation		-	500	700	μA
I _{DD}	Maximum current (peak) during the whole programming / erase operation	T _A = 25 °C, V _{DD} = 3.6 V	-	1.5	2.5	mA

 Table 51. Flash memory and data EEPROM characteristics

1. Guaranteed by design.

Cumhal	Devenedar	Conditions	Value	11	
Symbol	Parameter	Conditions	Min ⁽¹⁾	Unit	
	Cycling (erase / write) Program memory		10		
Novo ⁽²⁾	Cycling (erase / write) EEPROM data memory		100	kovoles	
N _{CYC} (-/	Cycling (erase / write) Program memory	T. – -40°C to 125 °C	0.2	kcycles	
	Cycling (erase / write) EEPROM data memory		2		
	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T = +85 °C	30		
	Data retention (EEPROM data memory) after 100 kcycles at $T_A = 85 \text{ °C}$	TRET - 100 C	30		
t(2)	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T = +105 °C		veare	
^I RET ⁽⁻⁾	Data retention (EEPROM data memory) after 100 kcycles at T _A = 105 °C	1 RET = 1100 0	- 10	years	
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T = +125 °C			
	Data retention (EEPROM data memory) after 2 kcycles at T_A = 125 °C	1 RET - 123 C			

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.



Output voltage levels

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OL} ⁽¹⁾	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ ,	-	0.4	
V _{OH} ⁽³⁾	Output high level voltage for an I/O pin	$1_{\text{IO}} = +6 \text{ IIA}$ 2.7 V \leq V _{DD} \leq 3.6 V	V _{DD} -0.4	-	
V _{OL} ⁽¹⁾	Output low level voltage for an I/O pin	$\begin{array}{c} {\sf TTL \ port}^{(2)}, \\ {\sf I}_{IO} = + \ 8 \ mA \\ {\sf 2.7 \ V} \leq {\sf V}_{DD} \leq \ 3.6 \ {\sf V} \end{array}$	-	0.4	
V _{OH} ⁽³⁾⁽⁴⁾	Output high level voltage for an I/O pin	$\begin{array}{l} \text{TTL port}^{(2)},\\ \text{I}_{\text{IO}} \texttt{=} -6 \text{ mA}\\ 2.7 \text{ V} \leq \text{V}_{DD} \leq \ 3.6 \text{ V} \end{array}$	2.4	-	
V _{OL} ⁽¹⁾⁽⁴⁾	Output low level voltage for an I/O pin	I_{IO} = +15 mA 2.7 V \leq V _{DD} \leq 3.6 V	-	1.3	V
V _{OH} ⁽³⁾⁽⁴⁾	Output high level voltage for an I/O pin	$\begin{array}{l} \text{I}_{\text{IO}} \text{ = -15 mA} \\ \text{2.7 V} \leq \text{V}_{DD} \leq \ \text{3.6 V} \end{array}$	V _{DD} -1.3	-	
V _{OL} ⁽¹⁾⁽⁴⁾	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V \leq V _{DD} < 3.6 V	-	0.45	
V _{OH} ⁽³⁾⁽⁴⁾	Output high level voltage for an I/O pin	I_{IO} = -4 mA 1.65 V \leq V _{DD} \leq 3.6 V	V _{DD} -0.45	-	
V _{OLFM+} ⁽¹⁾⁽⁴⁾	Output low level voltage for an FTf	$I_{IO} = 20 \text{ mA}$ 2.7 V \leq V _{DD} \leq 3.6 V	-	0.4	
	I/O pin in Fm+ mode	$\begin{array}{c} {\sf I}_{IO} = 10 \mbox{ mA} \\ 1.65 \mbox{ V} \leq {\sf V}_{DD} \leq \ 3.6 \mbox{ V} \end{array}$	-	0.4	

Table 59. Output voltage characteristics

 The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 23*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed ΣI_{IO(PIN)}.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in Table 23. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.

4. Guaranteed by characterization results.

Equation 1: RAIN max formula

$$R_{AIN} < \frac{T_{S}}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

		R _{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (k Ω)						
T _s (cycles)	t _S (µs)		V _{DD} > 2.7 V	V _{DD} > 2.4 V	V _{DD} > 2.0 V	V _{DD} > 1.8 V	V _{DD} > 1.75 V	V _{DD} > 1.65 V and T _A > –10 °C	V _{DD} > 1.65 V and T _A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

Table 63. R_{AIN} max for f_{ADC} = 16 MHz⁽¹⁾

1. Guaranteed by design.

Table 64. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
ET	Total unadjusted error		-	2	4	
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	LSB
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error	fferential linearity error		1	1.5	
	Effective number of bits	1.65 V < V _{DDA} = V _{REF+} < 3.6 V, range 1/2/3	10.2	11		bits
ENOB	Effective number of bits (16-bit mode oversampling with ratio =256) ⁽⁴⁾		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	
	Signal-to-noise ratio		63	69	-	
SNR	Signal-to-noise ratio (16-bit mode oversampling with ratio =256) ⁽⁴⁾		70	76	-	dB
THD	Total harmonic distortion		-	-85	-73	





Figure 33. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

6.3.16 Temperature sensor characteristics

Table 65. Temperature sensor calibration values

Calibration value name	Description	Memory address	
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V _{DDA} = 3 V	0x1FF8 007A - 0x1FF8 007B	
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA} = 3 V	0x1FF8 007E - 0x1FF8 007F	

Symbol	Parameter	Min	Тур	Max	Unit
T _L ⁽¹⁾	V _{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope ⁽¹⁾	Average slope	1.48	1.61	1.75	mV/°C
V ₁₃₀	Voltage at 130°C ±5°C ⁽²⁾	640	670	700	mV
I _{DDA(TEMP)} ⁽³⁾	Current consumption	-	3.4	6	μA
t _{START} ⁽³⁾	Startup time	-	-	10	116
$T_{S_{temp}}^{(4)(3)}$	ADC sampling time when reading the temperature	10	-	-	μο

Table 66. Temperature sensor characteristics

1. Guaranteed by characterization results.

2. Measured at V_{DD} = 3 V \pm 10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.

3. Guaranteed by design.

4. Shortest sampling time can be determined in the application by multiple iterations.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		Master mode			8	
f _{SCK}	SPI clock frequency	Slave mode Transmitter 1.65 <v<sub>DD<3.6V</v<sub>	_	-	8	MHz
		Slave mode Transmitter 2.7 <v<sub>DD<3.6V</v<sub>			8 ⁽²⁾	
Duty _(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
t _{su(NSS)}	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	
t _{h(NSS)}	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
t _{su(MI)}	Deta input actua tima	Master mode	0	-	-	
t _{su(SI)}	Data input setup time	Slave mode	3	-	-	
t _{h(MI)}	Data input hold time	Master mode	11	-	-	
t _{h(SI)}	Data input hold time	Slave mode	4.5	-	-	ns
t _{a(SO}	Data output access time	Slave mode	18	-	52	
t _{dis(SO)}	Data output disable time	Slave mode	12	-	42	
t _{v(SO)}	Data output valid time	Slave mode	-	20	56.5	
t _{v(MO)}		Master mode	-	5	9	
t _{h(SO)}	Data output hold time	Slave mode	13	-	-	
t _{h(MO)}		Master mode	3	-	-	

Table 73. SPI	characteristics in	voltage	Range	2 ⁽¹⁾

1. Guaranteed by characterization results.

2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty_(SCK) = 50%.



Symbol		millimeters			inches			
Cymbol	Min	Тур	Max	Min	Тур	Max		
A	0.525	0.555	0.585	0.0207	0.0219	0.0230		
A1	-	0.175	-	-	0.0069	-		
A2	-	0.380	-	-	0.0150	-		
A3 ⁽²⁾	-	0.025	-	-	0.0010	-		
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110		
D	3.259	3.294	3.329	0.1283	0.1297	0.1311		
E	3.223	3.258	3.293	0.1269	0.1283	0.1296		
е	-	0.400	-	-	0.0157	-		
e1	-	2.400	-	-	0.0945	-		
e2	-	2.400	-	-	0.0945	-		
F	-	0.447	-	-	0.0176	-		
G	-	0.429	-	-	0.0169	-		
aaa	-	-	0.100	-	-	0.0039		
bbb	-	-	0.100	-	-	0.0039		
CCC	-	-	0.100	-	-	0.0039		
ddd	-	-	0.050	-	-	0.0020		
eee	-	-	0.050	-	-	0.0020		

Table 82. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scalepackage mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 51. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale recommended footprint







Figure 54. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking versus pin 1 position identifier location.



Figure 55. LQFP48 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



Gumbal	millimeters			inches ⁽¹⁾			
Зутвої	Min	Тур	Мах	Min	Тур	Мах	
А	-	-	1.600	-	-	0.0630	
A1	0.050	-	0.150	0.0020	-	0.0059	
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571	
b	0.300	0.370	0.450	0.0118	0.0146	0.0177	
с	0.090	-	0.200	0.0035	-	0.0079	
D	8.800	9.000	9.200	0.3465	0.3543	0.3622	
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835	
D3	-	5.600	-	-	0.2205	-	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622	
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835	
E3	-	5.600	-	-	0.2205	-	
е	-	0.800	-	-	0.0315	-	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295	
L1	-	1.000	-	-	0.0394	-	
k	0°	3.5°	7°	0°	3.5°	7°	
ccc	-	-	0.100	-	-	0.0039	

Table 85. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.





1. Dimensions are expressed in millimeters.



7.9 Thermal characteristics

The maximum chip-junction temperature, $T_{\rm J}$ max, in degrees Celsius, may be calculated using the following equation:

 $T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and P_{I/O} max (P_D max = P_{INT} max + P_{I/O}max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

P_{I/O} max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I}/\mathsf{O}} \max = \Sigma (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma ((\mathsf{V}_{\mathsf{DD}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	36	
Θ _{JA}	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	54	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	48	°C/W
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	64	0,11
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm / 0.5 mm pitch	57	

Table of . Thermal characteristic	Table 8	37. Thei	rmal chai	racteristic
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