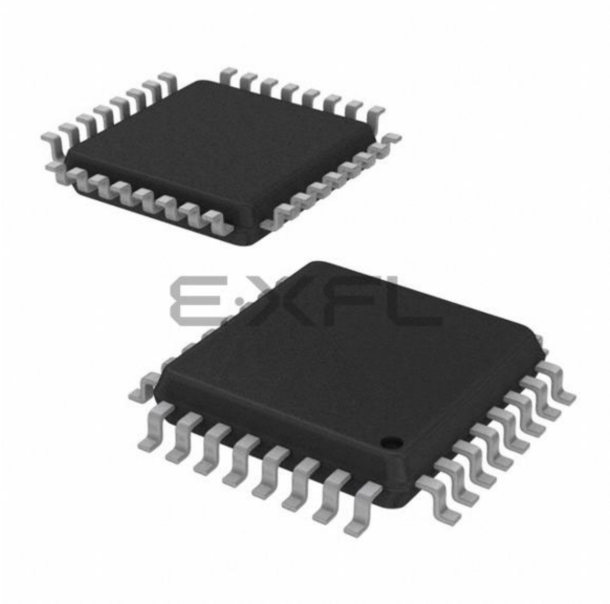

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 6K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071kzt6 |

# List of tables

# 1 Introduction

The ultra-low-power STM32L071xx are offered in 9 different package types from 32 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L071xx microcontrollers suitable for a wide range of applications:

- Gas/water meters and industrial sensors
- Healthcare and fitness equipment
- Remote control and user interface
- PC peripherals, gaming, GPS equipment
- Alarm system, wired and wireless sensors, video intercom

This STM32L071xx datasheet should be read in conjunction with the STM32L0x1xx reference manual (RM0377).

For information on the ARM® Cortex®-M0+ core please refer to the Cortex®-M0+ Technical Reference Manual, available from the www.arm.com website.

*Figure 1* shows the general block diagram of the device family.

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)(2)

| IPs | Run/Active | Sleep | Low-power run | Low-power sleep | Stop | Stop Wakeup capability | Standby | Standby Wakeup capability |
|---|---|---|---|---|---|---|---|---|
| Consumption $V_{DD}$=1.8 to 3.6 V (Typ) | Down to 140 µA/MHz (from Flash memory) | Down to 37 µA/MHz (from Flash memory) | Down to 8 µA | Down to 4.5 µA | 0.4 µA (No RTC) $V_{DD}$=1.8 V | | 0.28 µA (No RTC) $V_{DD}$=1.8 V | |
| | | | | | 0.8 µA (with RTC) $V_{DD}$=1.8 V | | 0.65 µA (with RTC) $V_{DD}$=1.8 V | |
| | | | | | 0.4 µA (No RTC) $V_{DD}$=3.0 V | | 0.29 µA (No RTC) $V_{DD}$=3.0 V | |
| | | | | | 1 µA (with RTC) $V_{DD}$=3.0 V | | 0.85 µA (with RTC) $V_{DD}$=3.0 V | |

1. Legend:
"Y" = Yes (enable).
"O" = Optional can be enabled/disabled by software)
"-" = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

## 3.2 Interconnect matrix

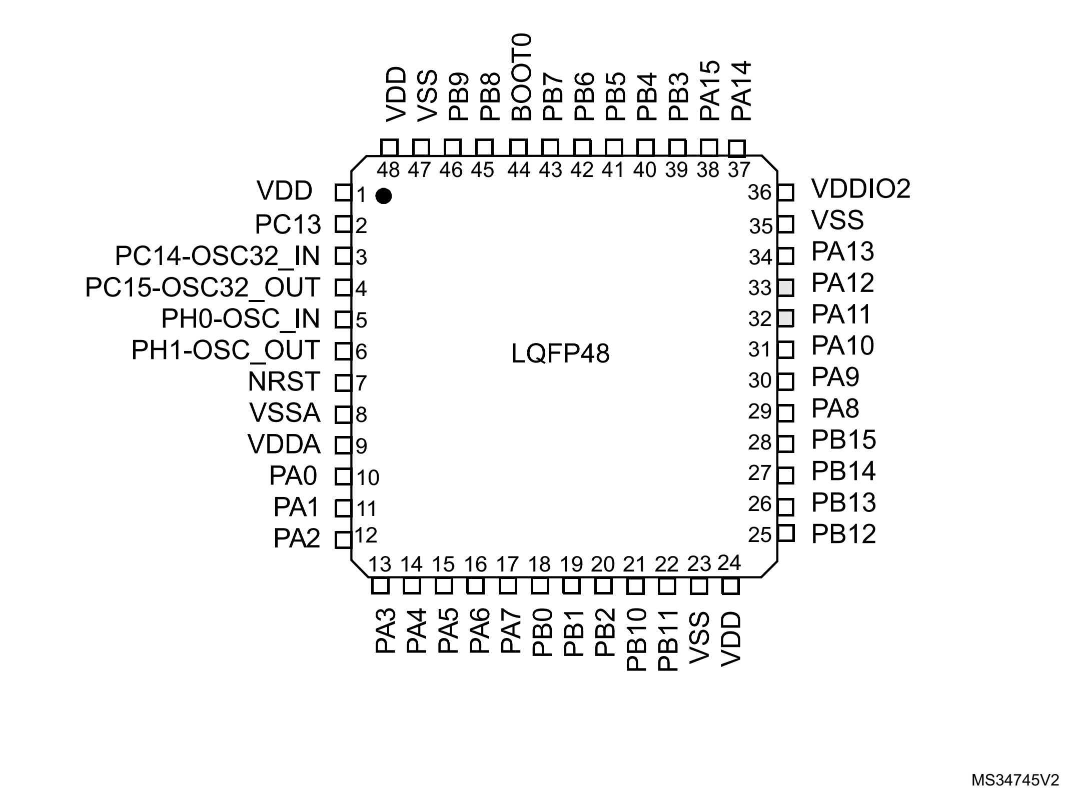
Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

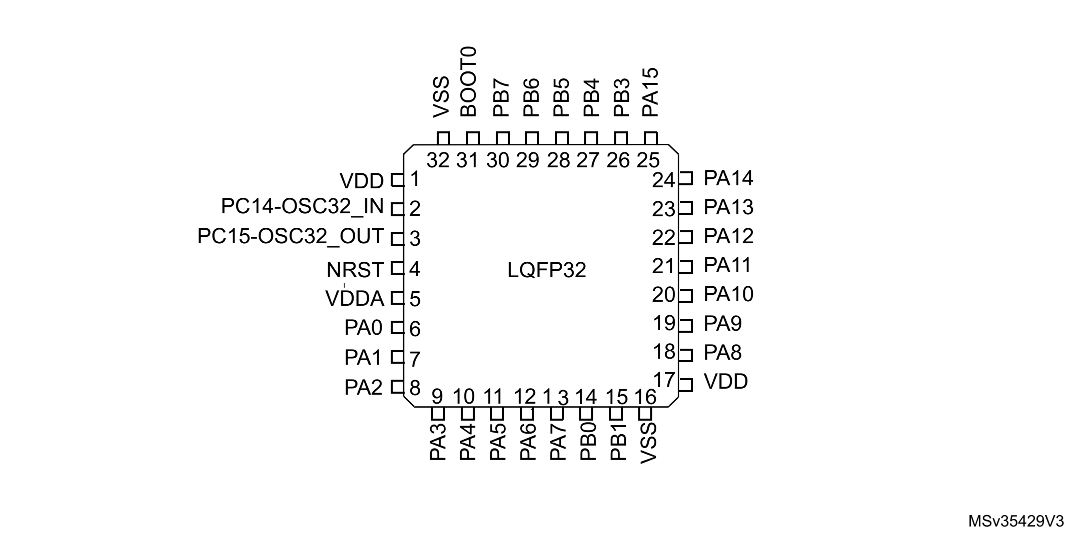
| Interconnect source | Interconnect destination | Interconnect action | Run | Sleep | Low-power run | Low-power sleep | Stop |
|---|---|---|---|---|---|---|---|
| COMPx | TIM2,TIM21, TIM22 | Timer input channel, trigger from analog signals comparison | Y | Y | Y | Y | - |
| | LPTIM | Timer input channel, trigger from analog signals comparison | Y | Y | Y | Y | Y |
| TIMx | TIMx | Timer triggered by other timer | Y | Y | Y | Y | - |

**Figure 8. STM32L071xx LQFP48 pinout - 7 x 7 mm**




1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

**Figure 9. STM32L071xx LQFP32 pinout**




1. The above figure shows the package top view.

**Table 19. Alternate functions port D**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2/I2C1/ TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF | I2C1/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT | I2C3/LPUART1/ COMP1/2/TIM3 |
| Port D | PD0 | TIM21_CH1 | SPI2_NSS/I2S2_WS | - | - | - | - | - | - |
| | PD1 | - | SPI2_SCK/I2S2_CK | - | - | - | - | - | - |
| | PD2 | LPUART1_RTS_ DE | | TIM3_ETR | - | - | - | USART5_RX | - |
| | PD3 | USART2_CTS | | SPI2_MISO/ I2S2_MCK | - | - | - | - | - |
| | PD4 | USART2_RTS_D E | SPI2_MOSI/I2S2_SD | - | - | - | - | - | - |
| | PD5 | USART2_TX | - | - | - | - | - | - | - |
| | PD6 | USART2_RX | - | - | - | - | - | - | - |
| | PD7 | USART2_CK | TIM21_CH2 | - | - | - | - | - | - |
| | PD8 | LPUART1_TX | | - | - | - | - | - | - |
| | PD9 | LPUART1_RX | | - | - | - | - | - | - |
| | PD10 | - | | - | - | - | - | - | - |
| | PD11 | LPUART1_CTS | | - | - | - | - | - | - |
| | PD12 | LPUART1_RTS_ DE | | - | - | - | - | - | - |
| | PD13 | - | | - | - | - | - | - | - |
| | PD14 | - | | - | - | - | - | - | - |
| | PD15 | | | - | - | - | - | - | - |

**Table 20. Alternate functions port E**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/I2S2/ USART1/2/ LPUART1/LPTI M1/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2/I2C1 /TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF | I2C1/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT | I2C3/LPUART1/ COMP1/2/TIM3 |
| Port E | PE0 | - | | EVENTOUT | - | - | - | - | - |
| | PE1 | - | | EVENTOUT | - | - | - | - | - |
| | PE2 | - | | TIM3_ETR | - | - | - | - | - |
| | PE3 | TIM22_CH1 | | TIM3_CH1 | - | - | - | - | - |
| | PE4 | TIM22_CH2 | - | TIM3_CH2 | - | - | - | - | - |
| | PE5 | TIM21_CH1 | - | TIM3_CH3 | - | - | - | - | - |
| | PE6 | TIM21_CH2 | - | TIM3_CH4 | - | - | - | - | - |
| | PE7 | - | | - | - | - | - | USART5_CK/USART5_RTS_DE | - |
| | PE8 | - | | - | - | - | - | USART4_TX | - |
| | PE9 | TIM2_CH1 | | TIM2_ETR | - | - | - | USART4_RX | - |
| | PE10 | TIM2_CH2 | | - | - | - | - | USART5_TX | - |
| | PE11 | TIM2_CH3 | - | - | - | - | - | USART5_RX | - |
| | PE12 | TIM2_CH4 | - | SPI1_NSS | - | - | - | - | - |
| | PE13 | - | | SPI1_SCK | - | - | - | - | - |
| | PE14 | - | | SPI1_MISO | - | - | - | - | - |
| | PE15 | - | | SPI1_MOSI | - | - | - | - | - |

**Table 34. Current consumption in Low-power run mode**

| Symbol | Parameter | Condition | | | $f_{HCLK}$ (MHz) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Run) | Supply current in Low-power run mode | All peripherals OFF, code executed from RAM, Flash memory switched OFF, $V_{DD}$ from 1.65 to 3.6 V | MSI clock = 65 kHz, $f_{HCLK}$= 32 kHz | $T_A$ = − 40 to 25°C | 0,032 | 9,45 | 12 | µA |
| | | | | $T_A$ = 85°C | | 14 | 58 | |
| | | | | $T_A$ = 105°C | | 21 | 64 | |
| | | | | $T_A$ = 125°C | | 36,5 | 160 | |
| | | | MSI clock = 65 kHz, $f_{HCLK}$= 65kHz | $T_A$ = − 40 to 25°C | 0,065 | 14,5 | 18 | |
| | | | | $T_A$ = 85°C | | 19,5 | 60 | |
| | | | | $T_A$ = 105°C | | 26 | 65 | |
| | | | | $T_A$ = 125°C | | 42 | 160 | |
| | | | MSI clock=131 kHz, $f_{HCLK}$= 131 kHz | $T_A$ = − 40 to 25°C | 0,131 | 26,5 | 30 | |
| | | | | $T_A$ = 55°C | | 27,5 | 60 | |
| | | | | $T_A$ = 85°C | | 31 | 66 | |
| | | | | $T_A$ = 105°C | | 37,5 | 77 | |
| | | | | $T_A$ = 125°C | | 53,5 | 170 | |
| | | All peripherals OFF, code executed from Flash memory, VDD from 1.65 V to 3.6 V | MSI clock = 65 kHz, $f_{HCLK}$= 32 kHz | $T_A$ = − 40 to 25°C | 0,032 | 24,5 | 34 | |
| | | | | $T_A$ = 85°C | | 30 | 82 | |
| | | | | $T_A$ = 105°C | | 38,5 | 90 | |
| | | | | $T_A$ = 125°C | | 58 | 120 | |
| | | | MSI clock = 65 kHz, $f_{HCLK}$= 65 kHz | $T_A$ = − 40 to 25°C | 0,065 | 30,5 | 40 | |
| | | | | $T_A$ = 85°C | | 36,5 | 88 | |
| | | | | $T_A$ = 105°C | | 45 | 96 | |
| | | | | $T_A$ = 125°C | | 64,5 | 120 | |
| | | | MSI clock = 131 kHz, $f_{HCLK}$= 131 kHz | $T_A$ = − 40 to 25°C | 0,131 | 45 | 56 | |
| | | | | $T_A$ = 55°C | | 48 | 96 | |
| | | | | $T_A$ = 85°C | | 51 | 110 | |
| | | | | $T_A$ = 105°C | | 59,5 | 120 | |
| | | | | $T_A$ = 125°C | | 79,5 | 150 | |

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

**Table 40. Peripheral current consumption in Stop and Standby mode(1)**

| Symbol | Peripheral | Typical consumption, $T_A$ = 25 °C | | Unit |
|---|---|---|---|---|
| | | $V_{DD}$=1.8 V | $V_{DD}$=3.0 V | |
| $I_{DD(PVD / BOR)}$ | - | 0.7 | 1.2 | µA |
| $I_{REFINT}$ | - | - | 1.7 | |
| - | LSE Low drive(2) | 0.11 | 0,13 | |
| - | LSI | 0.27 | 0.31 | |
| - | IWDG | 0.2 | 0.3 | |
| - | LPTIM1, Input 100 Hz | 0.01 | 0,01 | |
| - | LPTIM1, Input 1 MHz | 11 | 12 | |
| - | LPUART1 | - | 0,5 | |
| - | RTC | 0.16 | 0,3 | |

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

### 6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 25*.

**Table 41. Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | $f_{HCLK}$ = 32 MHz | 7 | 8 | Number of clock cycles |
| $t_{WUSLEEP\_LP}$ | Wakeup from Low-power sleep mode, $f_{HCLK}$ = 262 kHz | $f_{HCLK}$ = 262 kHz<br>Flash memory enabled | 7 | 8 | |
| | | $f_{HCLK}$ = 262 kHz<br>Flash memory switched OFF | 9 | 10 | |

**Table 41. Low-power mode wakeup timings (continued)**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUSTOP}$ | Wakeup from Stop mode, regulator in Run mode | $f_{HCLK} = f_{MSI}$ = 4.2 MHz | 5.0 | 8 | µs |
| | | $f_{HCLK} = f_{HSI}$ = 16 MHz | 4.9 | 7 | |
| | | $f_{HCLK} = f_{HSI}/4$ = 4 MHz | 8.0 | 11 | |
| | Wakeup from Stop mode, regulator in low-power mode | $f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1 | 5.0 | 8 | |
| | | $f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2 | 5.0 | 8 | |
| | | $f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3 | 5.0 | 8 | |
| | | $f_{HCLK} = f_{MSI}$ = 2.1 MHz | 7.3 | 13 | |
| | | $f_{HCLK} = f_{MSI}$ = 1.05 MHz | 13 | 23 | |
| | | $f_{HCLK} = f_{MSI}$ = 524 kHz | 28 | 38 | |
| | | $f_{HCLK} = f_{MSI}$ = 262 kHz | 51 | 65 | |
| | | $f_{HCLK} = f_{MSI}$ = 131 kHz | 100 | 120 | |
| | | $f_{HCLK}$ = MSI = 65 kHz | 190 | 260 | |
| | | $f_{HCLK} = f_{HSI}$ = 16 MHz | 4.9 | 7 | |
| | | $f_{HCLK} = f_{HSI}/4$ = 4 MHz | 8.0 | 11 | |
| | Wakeup from Stop mode, regulator in low-power mode, code running from RAM | $f_{HCLK} = f_{HSI}$ = 16 MHz | 4.9 | 7 | |
| | | $f_{HCLK} = f_{HSI}/4$ = 4 MHz | 7.9 | 10 | |
| | | $f_{HCLK} = f_{MSI}$ = 4.2 MHz | 4.7 | 8 | |
| $t_{WUSTDBY}$ | Wakeup from Standby mode FWU bit = 1 | $f_{HCLK}$ = MSI = 2.1 MHz | 65 | 130 | |
| | Wakeup from Standby mode FWU bit = 0 | $f_{HCLK}$ = MSI = 2.1 MHz | 2.2 | 3 | ms |

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 53*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 53. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 32 MHz conforms to IEC 61000-4-2 | 3B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 32 MHz conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Figure 26. $V_{IH}/V_{IL}$ versus VDD (CMOS I/Os)**

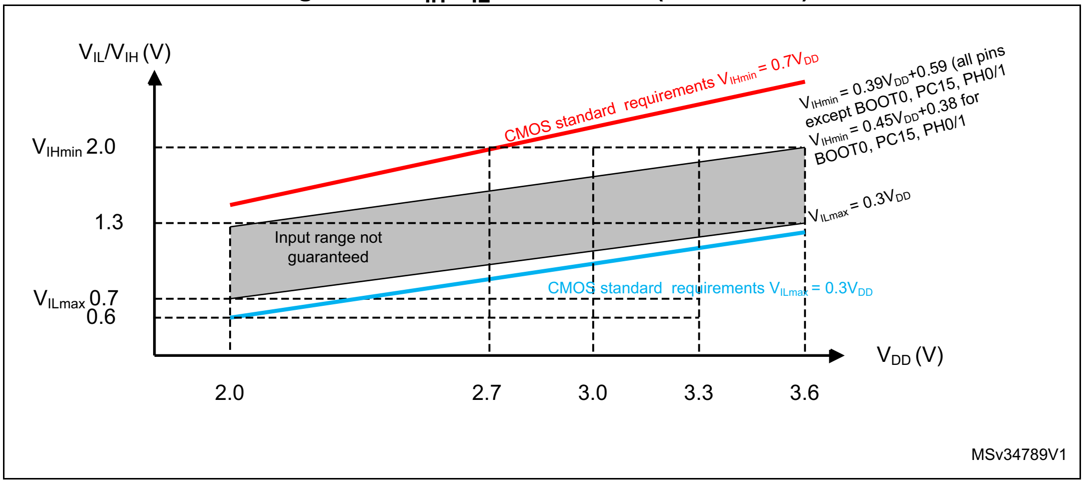
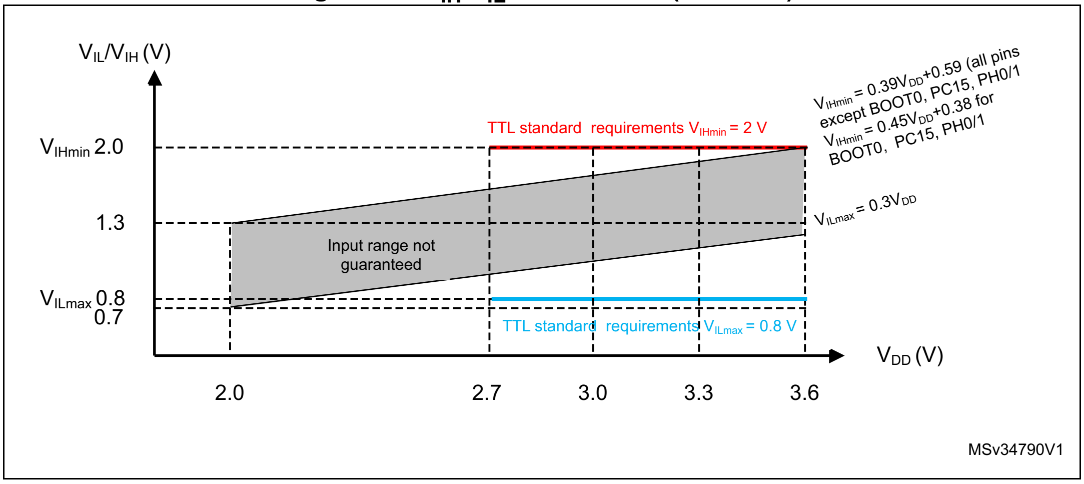



**Figure 27. $V_{IH}/V_{IL}$ versus VDD (TTL I/Os)**




### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard $V_{OL}/V_{OH}$ specifications given in *Table 59*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 23*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 23*).

**Table 62. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{ADC}$(3) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$(3)(5) | Calibration time | $f_{ADC}$ = 16 MHz | 5.2 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |
| $W_{LATENCY}$(6) | ADC_DR register write latency | ADC clock = HSI16 | 1.5 ADC cycles + 2 $f_{PCLK}$ cycles | - | 1.5 ADC cycles + 3 $f_{PCLK}$ cycles | - |
| | | ADC clock = PCLK/2 | - | 4.5 | - | $f_{PCLK}$ cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | $f_{PCLK}$ cycle |
| $t_{latr}$(3) | Trigger conversion latency | $f_{ADC} = f_{PCLK}/2$ = 16 MHz | 0.266 | | | µs |
| | | $f_{ADC} = f_{PCLK}/2$ | 8.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{PCLK}/4$ = 8 MHz | 0.516 | | | µs |
| | | $f_{ADC} = f_{PCLK}/4$ | 16.5 | | | $1/f_{PCLK}$ |
| | | $f_{ADC} = f_{HSI16}$ = 16 MHz | 0.252 | - | 0.260 | µs |
| $Jitter_{ADC}$ | ADC jitter on trigger conversion | $f_{ADC} = f_{HSI16}$ | - | 1 | - | $1/f_{HSI16}$ |
| $t_S$(3) | Sampling time | $f_{ADC}$ = 16 MHz | 0.093 | - | 10.03 | µs |
| | | - | 1.5 | - | 160.5 | $1/f_{ADC}$ |
| $t_{UP\_LDO}$(3)(5) | Internal LDO power-up time | - | - | - | 10 | µs |
| $t_{STAB}$(3)(5) | ADC stabilization time | - | 14 | | | $1/f_{ADC}$ |
| $t_{ConV}$(3) | Total conversion time (including sampling time) | $f_{ADC}$ = 16 MHz, 12-bit resolution | 0.875 | - | 10.81 | µs |
| | | 12-bit resolution | 14 to 173 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. $V_{DDA}$ minimum value can be decreased in specific temperature conditions. Refer to *Table 63: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 39: Peripheral current consumption in Run or Sleep mode*).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 63: RAIN max for fADC = 16 MHz*.
5. This parameter only includes the ADC timing. It does not take into account register access latency.
6. This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

## 6.3.17 Comparators

**Table 67. Comparator 1 characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | | 3.6 | V |
| $R_{400K}$ | $R_{400K}$ value | - | - | 400 | - | kΩ |
| $R_{10K}$ | $R_{10K}$ value | - | - | 10 | - | |
| $V_{IN}$ | Comparator 1 input voltage range | - | 0.6 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | - | - | 7 | 10 | µs |
| td | Propagation delay(2) | - | - | 3 | 10 | |
| Voffset | Comparator offset | - | - | ±3 | ±10 | mV |
| $d_{Voffset}/dt$ | Comparator offset variation in worst voltage stress conditions | $V_{DDA}$ = 3.6 V, $V_{IN+}$ = 0 V, $V_{IN-}$ = $V_{REFINT}$, $T_A$ = 25 °C | 0 | 1.5 | 10 | mV/1000 h |
| $I_{COMP1}$ | Current consumption(3) | - | - | 160 | 260 | nA |

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

**Table 68. Comparator 2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | - | 3.6 | V |
| $V_{IN}$ | Comparator 2 input voltage range | - | 0 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | Fast mode | - | 15 | 20 | µs |
| | | Slow mode | - | 20 | 25 | |
| $t_{d\ slow}$ | Propagation delay(2) in slow mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 1.8 | 3.5 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 2.5 | 6 | |
| $t_{d\ fast}$ | Propagation delay(2) in fast mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 0.8 | 2 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 1.2 | 4 | |
| $V_{offset}$ | Comparator offset error | | - | ±4 | ±20 | mV |
| dThreshold/ dt | Threshold voltage temperature coefficient | $V_{DDA}$ = 3.3V, $T_A$ = 0 to 50 °C, V- = $V_{REFINT}$, 3/4 $V_{REFINT}$, 1/2 $V_{REFINT}$, 1/4 $V_{REFINT}$. | - | 15 | 30 | ppm /°C |
| $I_{COMP2}$ | Current consumption(3) | Fast mode | - | 3.5 | 5 | µA |
| | | Slow mode | - | 0.5 | 2 | |

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

## 6.3.18 Timer characteristics

### TIM timer characteristics

The parameters given in the *Table 69* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 69. TIMx characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 31.25 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 32 MHz | 0 | 16 | MHz |
| $Res_{TIM}$ | Timer resolution | - | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected (timer's prescaler disabled) | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 0.0312 | 2048 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | - | 134.2 | s |

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

## 6.3.19 Communications interfaces

### I$^2$C interface characteristics

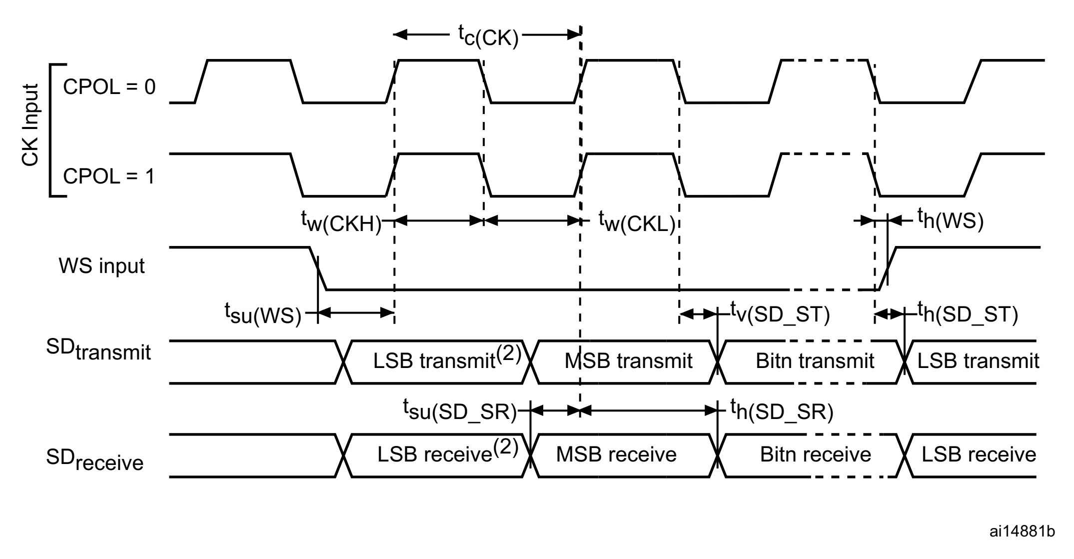
The I$^2$C interface meets the timings requirements of the I$^2$C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I$^2$C timing requirements are guaranteed by design when the I$^2$C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

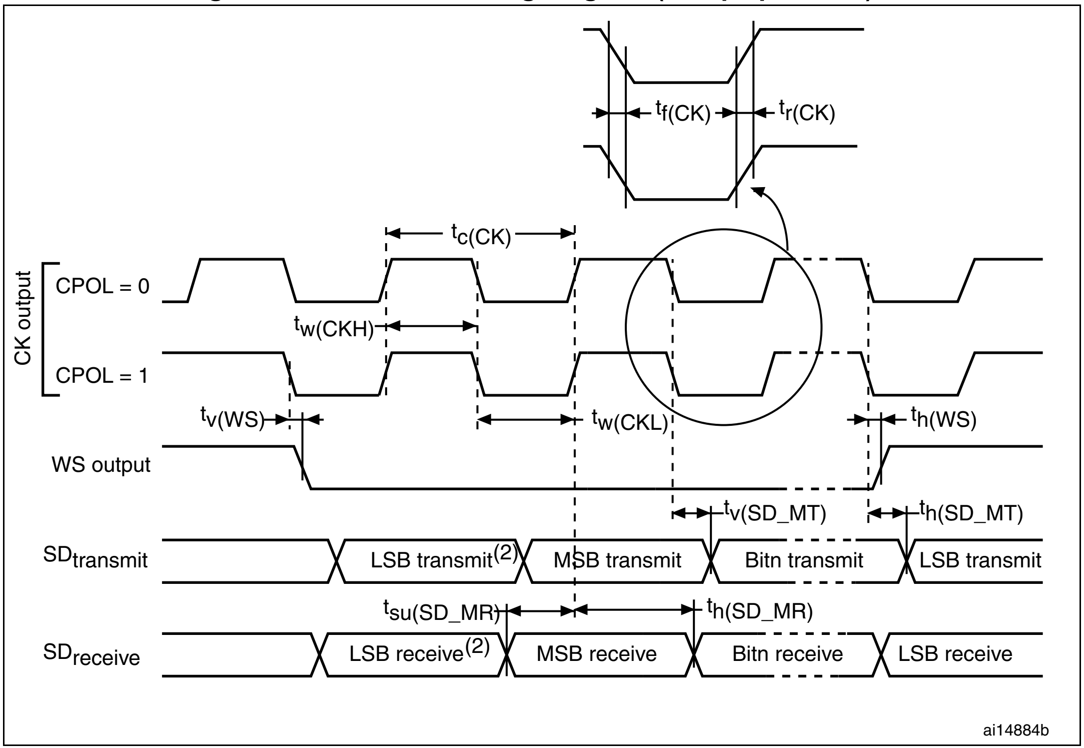
All I$^2$C SDA and SCL I/Os embed an analog filter (see *Table 70* for the analog filter characteristics).

**Figure 37. I²S slave timing diagram (Philips protocol)(1)**




1. Measurement points are done at CMOS levels: 0.3 × $V_{DD}$ and 0.7 × $V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 38. I²S master timing diagram (Philips protocol)(1)**



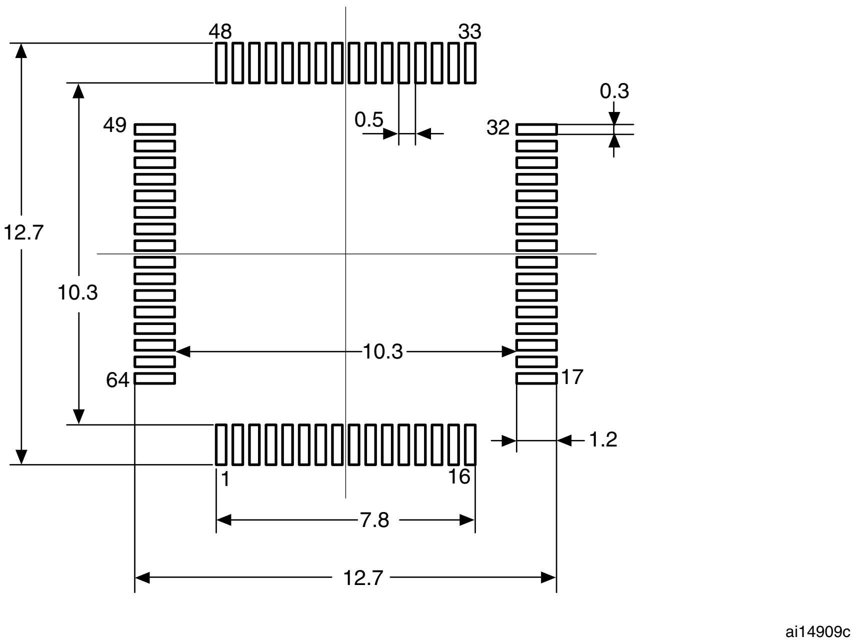

1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 45. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint**




1. Dimensions are expressed in millimeters.

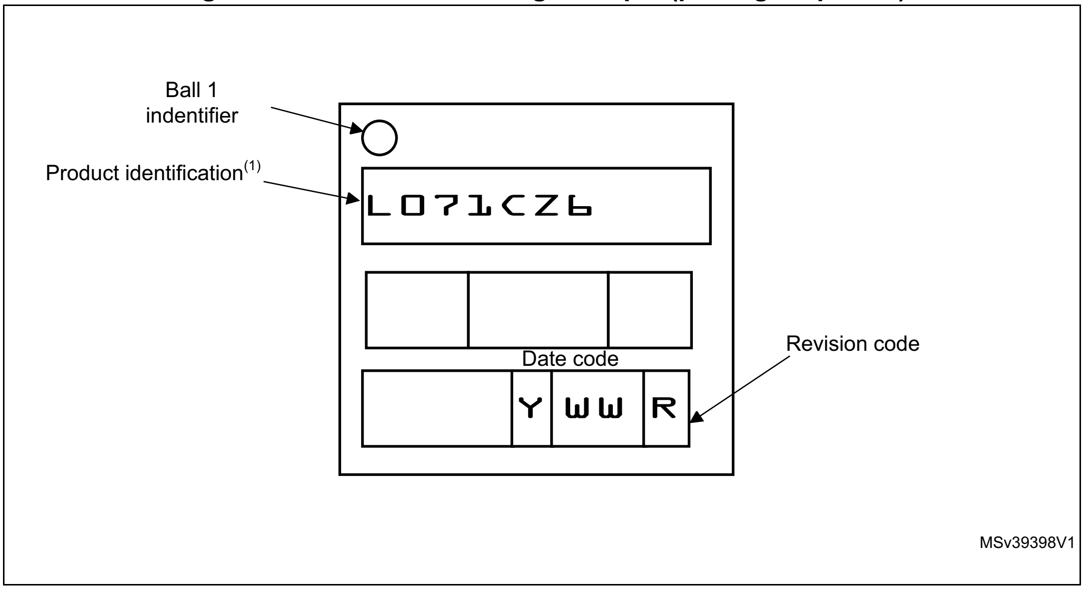
**Table 83. WLCSP49 recommended PCB design rules (0.4 mm pitch)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 |
| Dpad | 260 µm max. (circular) |
| | 220 µm recommended |
| Dsm | 300 µm min. (for 260 µm diameter pad) |
| PCB pad design | Non-solder mask defined via underbump allowed. |

### Device marking for WLCSP49

The following figure gives an example of topside marking versus ball A 1 position identifier location.

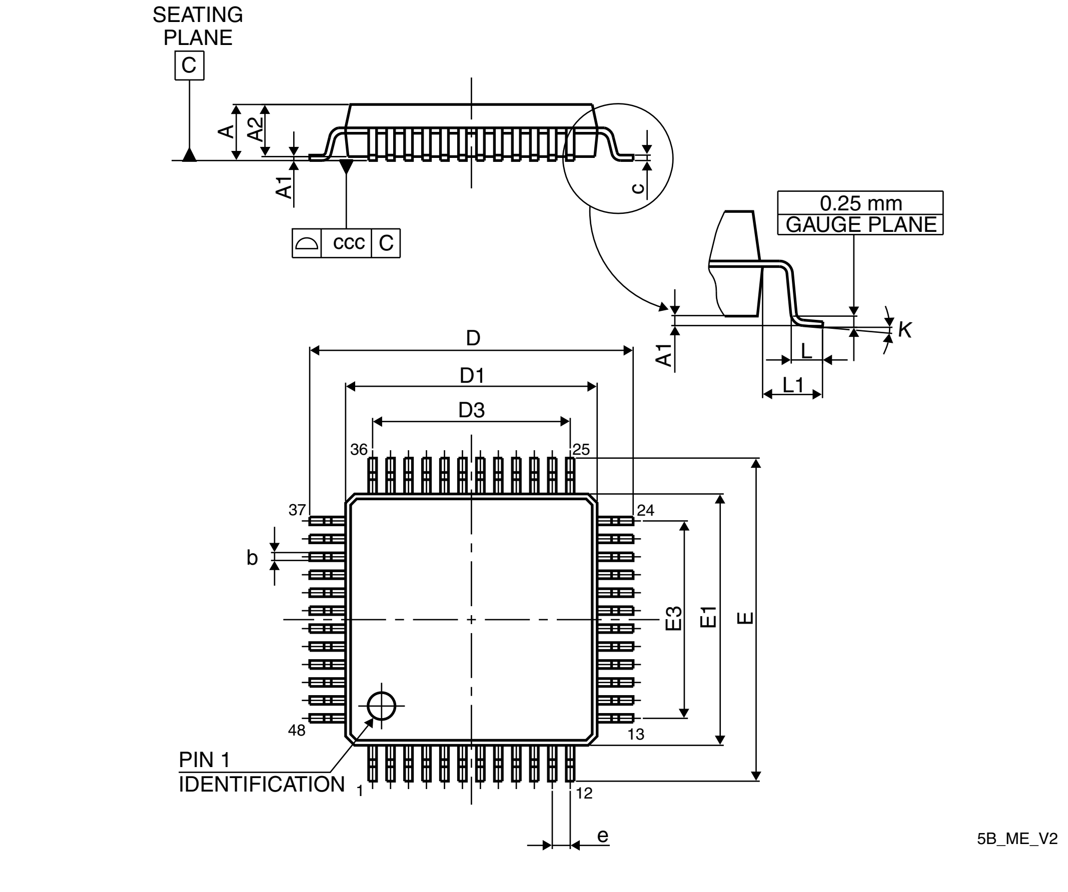
**Figure 52. WLCSP49 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.6 LQFP48 package information

**Figure 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**



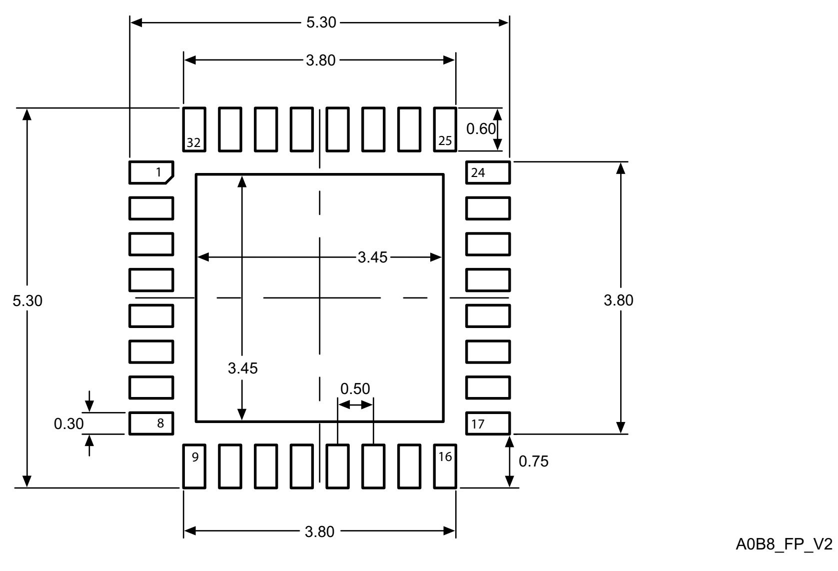

1. Drawing is not to scale.

**Table 86. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.0060 | - |
| b | 0.180 | 0.230 | 0.280 | 0.0071 | 0.0091 | 0.0110 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| D1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| D2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| E1 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| E2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 60. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint**




1. Dimensions are expressed in millimeters.

# 9 Revision history

**Table 89. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Sep-2015 | 1 | Initial release |
| 26-Oct-2015 | 2 | Changed confidentiality level to public.<br>Updated datasheet status to “production data”.<br>Modified ultra-low-power platform features on cover page.<br>In *Table 15: STM32L071xxx pin definition*:<br>– changed pin name to VDDIO2 for the following pins: UFQFPN32 pin 24, LQFP48 pin 36, LQFP64 pin 48, UFBGA64 pin E5, WLCSP49 pin A1, LQFP100 pin 75 and UFBGA100 pin G11.<br>– Added note related to UFQFPN32.<br>In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization.<br>Updated $\|\Delta V_{SS}\|$ definition to include $V_{REF-}$ in *Table 22: Voltage characteristics*.<br>Updated $f_{TRIG}$ and $V_{AIN}$ maximum value, added $V_{REF+}$ and $V_{REF-}$ in *Table 62: ADC characteristics*.<br>Added *Section : Device marking for LQFP100*.<br>Updated *Figure 42: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 76: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*.<br>Added *Section : Device marking for LQFP100*, *Section : Device marking for LQFP64*, *Section : Device marking for TFBGA64* and *Section : Device marking for WLCSP49*.<br>Updated *Figure 55: LQFP48 marking example (package top view)*. |