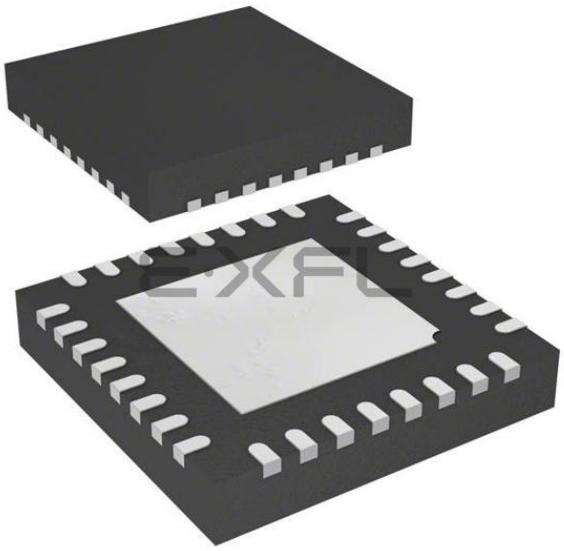

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071kzu3

Contents

2.1 Device overview

Table 2. Ultra-low-power STM32L071xx device features and peripheral counts

Peripheral		STM32L 071K8	STM32L 071C8	STM32L 071V8	STM32L 071KB	STM32L 071CB	STM32L 071VB	STM32L 071RB	STM32L 071KZ	STM32L 071CZ	STM32L 071VZ	STM32L 071RZ
Flash (Kbytes)		64 Kbytes			128 Kbytes				192 Kbytes			
Data EEPROM (Kbytes)		3 Kbytes			6 Kbytes							
RAM (Kbytes)		20 Kbytes										
Timers	General-purpose	4										
	Basic	2										
	LPTIMER	1										
RTC/SYSTICK/IWDG /WWDG		1/1/1/1										
Com. interfaces	SPI/I2S	4(3)[1]/0	6(4)[2]/1		4(3)[1]/0	6(4)[2]/1			4(3)[1]/0	6(4)[2]/1		
	I^2C	2	3		2	3			2	3		
	USART	3	4		3	4			3	4		
	LPUART	1										
GPIOs		23	37	84	25[3]	40[4]	84	51[5]	25[3]	40[4]	84	51[5]
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1										
12-bit synchronized ADC Number of channels		1 10	1 13	1 16	1 10	1 13[4]	1 16	1 16[5]	1 10	1 13[4]	1 16	1 16[5]
Comparators		2										
Max. CPU frequency		32 MHz										
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option										
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C										
Packages		UFQFPN 32	LQFP48	LQFP/ UFBGA 100	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64

1. 3 SPI interfaces are USARTs operating in SPI master mode.
2. 4 SPI interfaces are USARTs operating in SPI master mode.
3. UFQFPN32 has 2 GPIOs less than LQFP32.
4. LQFP48 has three GPIOs less than WLCSP49.
5. TFBGA64 has one GPIO, one ADC input less than LQFP64.

  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC clock source**

  The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.
- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.15 Communication interfaces

3.15.1 I²C bus

Up to three I²C interfaces (I2C1 and I2C3) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 10. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 and I2C3 provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1/I2C3 also have a clock domain independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

Refer to *Table 11* for an overview of I2C interface features.

Table 11. STM32L071xx I²C implementation

I2C features(1)	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X(2)	X
Independent clock	X	-	X
SMBus	X	-	X
Wakeup from STOP	X	-	X

1. X = supported.
2. See *Table 15: STM32L071xxx pin definition on page 39* for the list of I/Os that feature Fast Mode Plus capability

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	11	-	-	18	K2	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD	ADC_IN13
-	4	8	12	F1	-	19	J1	VSSA	S		-	-	-
-	-	-	-	-	-	20	K1	VREF-	S		-	-	-
-	-	-	-	G1	E6	21	L1	VREF+	S		-	-	-
5	5	9	13	H1	F7	22	M1	VDDA	S		-	-	-
6	6	10	14	G2	E5	23	L2	PA0	I/O	TTa	-	TIM2_CH1, USART2_CTS, TIM2_ETR, USART4_TX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1
7	7	11	15	H2	E4	24	M2	PA1	I/O	FT	-	EVENTOUT, TIM2_CH2, USART2_RTS_DE, TIM21_ETR, USART4_RX	COMP1_INP, ADC_IN1
8	8	12	16	F3	F6	25	K3	PA2	I/O	FT	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2
9	9	13	17	G3	G7	26	L3	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
-	-	-	18	C2	-	27	D3	VSS	S	-	-	-	-
-	-	-	19	D2	-	28	H3	VDD	S	-	-	-	-
10	10	14	20	H3	F5	29	M3	PA4	I/O	TC	-	SPI1_NSS, USART2_CK, TIM22_ETR	COMP1_INM, COMP2_INM, ADC_IN4
11	11	15	21	F4	G6	30	K4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	-	-	54	B5	-	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, TIM3_ETR, USART5_RX	-
-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, SPI2_MISO/I2S2_MCK	-
-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS_DE, SPI2_MOSI/I2S2_SD	-
-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX	-
-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX	-
-	-	-	-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, TIM21_CH2	-
26	-	39	55	A5	A3	89	A8	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, EVENTOUT, USART1_RTS_DE, USART5_TX	COMP2_INM
27	26	40	56	A4	B3	90	A7	PB4	I/O	FTf	-	SPI1_MISO, TIM3_CH1, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
28	27	41	57	C4	A4	91	C5	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_RTS_DE	COMP2_INP
29	28	42	58	D3	B4	92	B5	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR,	COMP2_INP

Table 16. Alternate functions port A

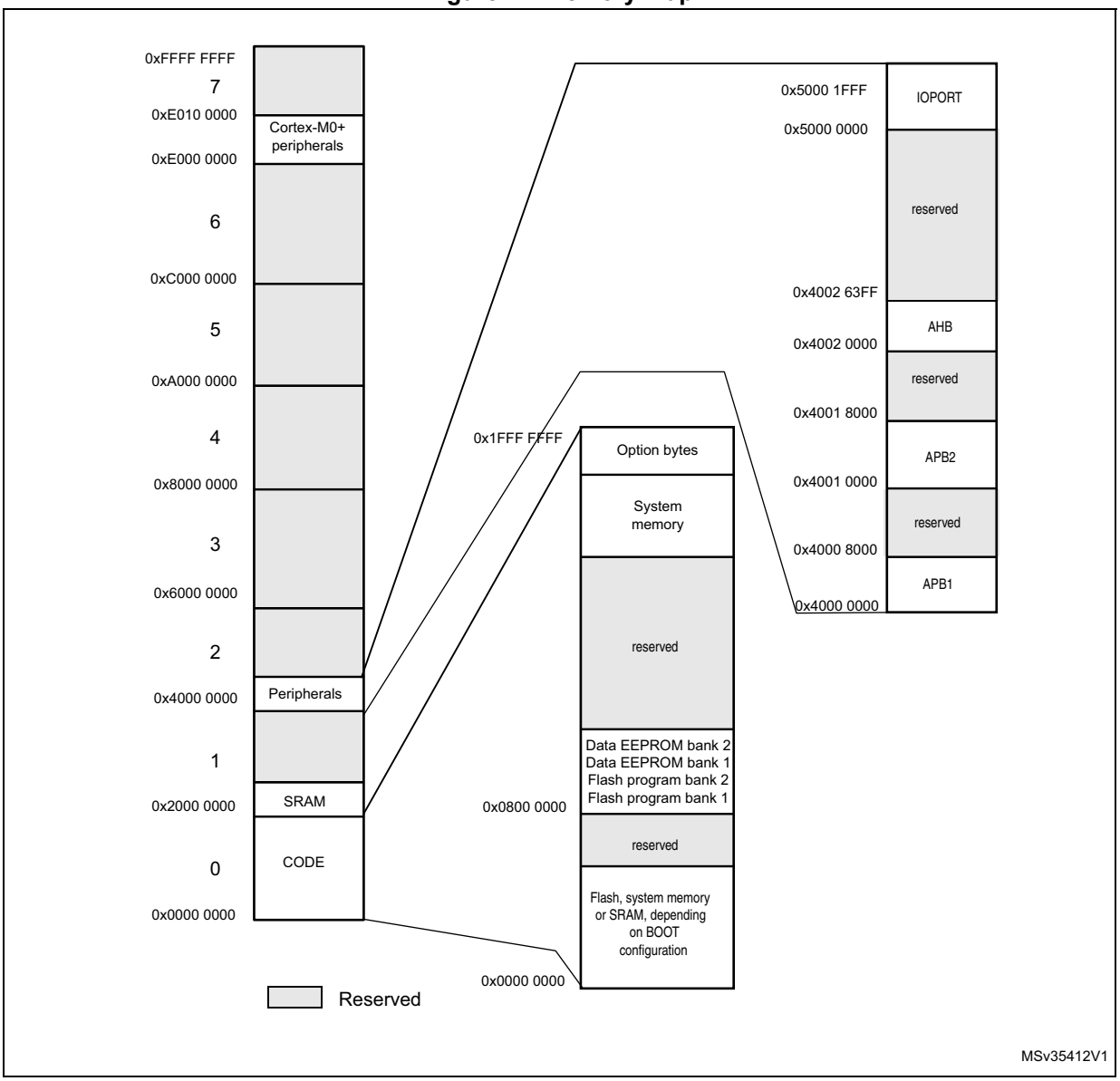
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/USART1/2/LPUART1/LPTIM1/TIM2/21/22/EVENTOUT/SYS_AF	SPI1/SPI2/I2S2/I2C1/TIM2/21	SPI1/SPI2/I2S2/LPUART1/USART5/LPTIM1/TIM2/3/EVENTOUT/SYS_AF	I2C1/EVENTOUT	I2C1/USART1/2/LPUART1/TIM3/22/EVENTOUT	SPI2/I2S2/I2C2/USART1/TIM2/21/22	I2C1/2/LPUART1/USART4/UASRT5/TIM21/EVENTOUT	I2C3/LPUART1/COMP1/2/TIM3
Port A	PA0	-	-	TIM2_CH1		USART2_CTS	TIM2_ETR	USART4_TX	COMP1_OUT
	PA1	EVENTOUT		TIM2_CH2		USART2_RTS_DE	TIM21_ETR	USART4_RX	-
	PA2	TIM21_CH1		TIM2_CH3		USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2		TIM2_CH4		USART2_RX	-	LPUART1_RX	-
	PA4	SPI1_NSS	-	-		USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR			TIM2_CH1	-	-
	PA6	SPI1_MISO		TIM3_CH1		LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI		TIM3_CH2		-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO			EVENTOUT	USART1_CK	-	-	I2C3_SCL
	PA9	MCO		-		USART1_TX	-	I2C1_SCL	I2C3_SMBA
	PA10	-		-		USART1_RX	-	I2C1_SDA	-
	PA11	SPI1_MISO	-	EVENTOUT		USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT		USART1_RTS_DE	-	-	COMP2_OUT
	PA13	SWDIO	-		-	-	-	LPUART1_RX	-
	PA14	SWCLK	-	-	-	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS		TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	USART4_RTS_DE	-

Table 19. Alternate functions port D

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1/ TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Port D	PD0	TIM21_CH1	SPI2_NSS/I2S2_WS	-	-	-	-	-	-
	PD1	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-
	PD2	LPUART1_RTS_ DE		TIM3_ETR	-	-	-	USART5_RX	-
	PD3	USART2_CTS		SPI2_MISO/ I2S2_MCK	-	-	-	-	-
	PD4	USART2_RTS_D E	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-
	PD5	USART2_TX	-	-	-	-	-	-	-
	PD6	USART2_RX	-	-	-	-	-	-	-
	PD7	USART2_CK	TIM21_CH2	-	-	-	-	-	-
	PD8	LPUART1_TX		-	-	-	-	-	-
	PD9	LPUART1_RX		-	-	-	-	-	-
	PD10	-		-	-	-	-	-	-
	PD11	LPUART1_CTS		-	-	-	-	-	-
	PD12	LPUART1_RTS_ DE		-	-	-	-	-	-
	PD13	-		-	-	-	-	-	-
	PD14	-		-	-	-	-	-	-
	PD15			-	-	-	-	-	-

5 Memory mapping

Figure 11. Memory map



1. Refer to the STM32L071xx reference manual for details on the Flash memory organization for each memory size.

6.3 Operating conditions

6.3.1 General operating conditions

Table 25. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}	Analog operating voltage (all features)	Must be the same voltage as V_{DD}(1)	1.65	3.6	V
V_{DDIO2}	Standard operating voltage	-	1.65	3.6	V
V_{IN}	Input voltage on FT, FTf and RST pins(2)	2.0 V ≤ V_{DD} ≤ 3.6 V	-0.3	5.5	V
		1.65 V ≤ V_{DD} ≤ 2.0 V	-0.3	5.2	
	Input voltage on BOOT0 pin	-	0	5.5	
	Input voltage on TC pin	-	-0.3	V_{DD}+0.3	
P_D	Power dissipation at T_A = 85 °C (range 6) or T_A =105 °C (rage 7) (3)	UFBGA100 package	-	351	mW
		LQFP100 package	-	488	
		TFBGA64 package	-	313	
		LQFP64 package	-	435	
		WLCSP49 package	-	417	
		LQFP48 package	-	370	
		UFQFPN32 package	-	556	
		LQFP32 package	-	333	
	Power dissipation at T_A = 125 °C (range 3) (3)	UFBGA100 package	-	88	
		LQFP100 package	-	122	
		TFBGA64 package	-	78	
		LQFP64 package	-	109	
		WLCSP49 package	-	104	
		LQFP48 package	-	93	
		UFQFPN32 package	-	139	
		LQFP32 package	-	83	

Figure 16. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS

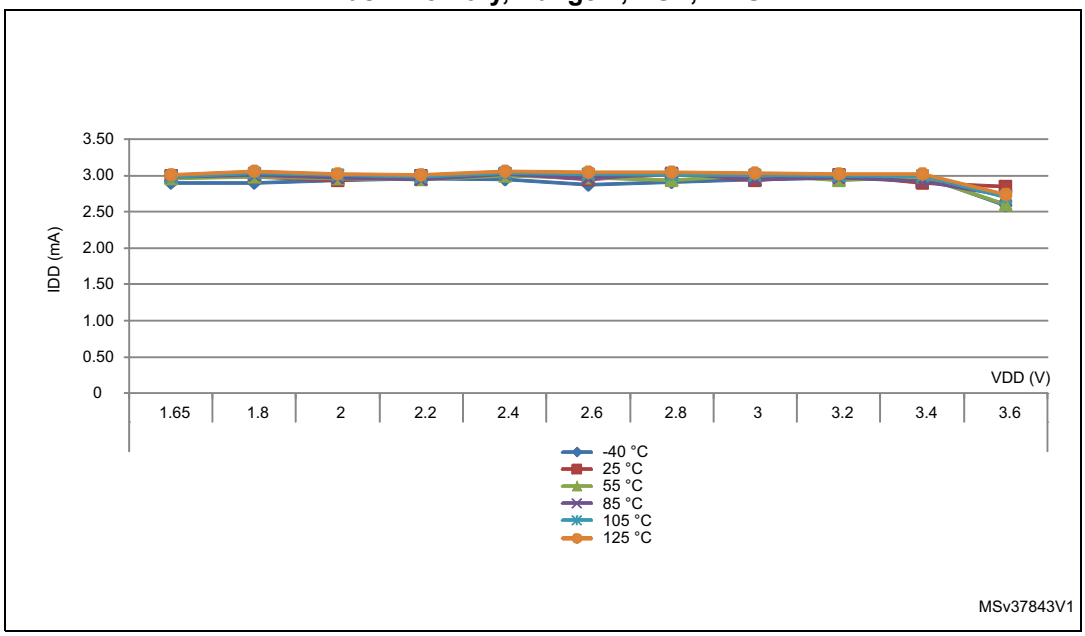


Figure 17. I_{DD} vs V_{DD}, at T_A= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS

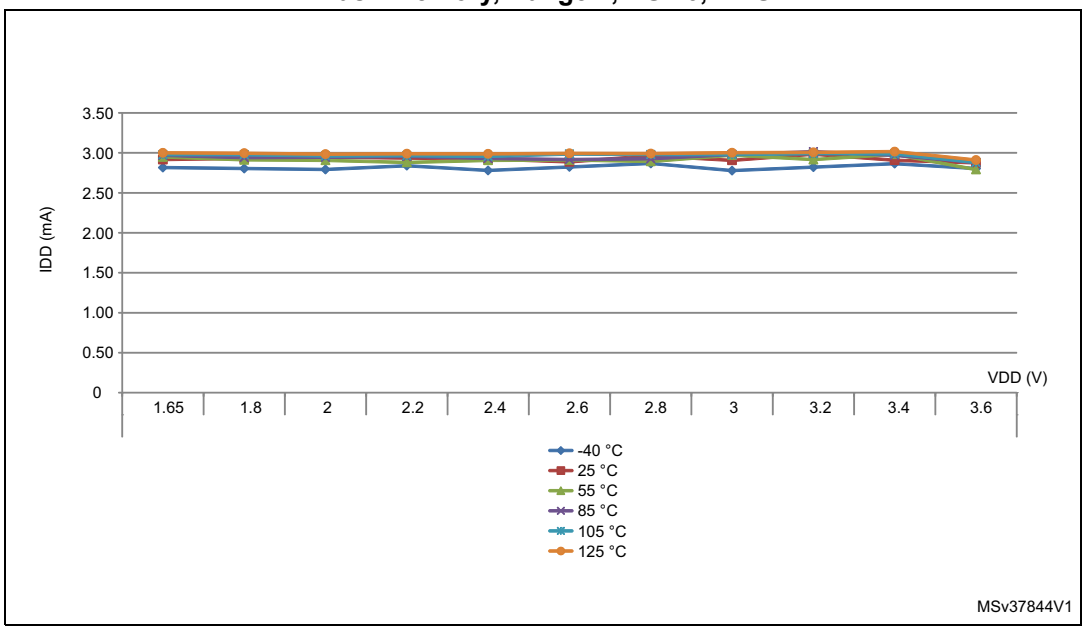


Table 34. Current consumption in Low-power run mode

Symbol	Parameter	Condition			f_{HCLK} (MHz)	Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash memory switched OFF, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK}= 32 kHz	T_A = − 40 to 25°C	0,032	9,45	12	µA
				T_A = 85°C		14	58	
				T_A = 105°C		21	64	
				T_A = 125°C		36,5	160	
			MSI clock = 65 kHz, f_{HCLK}= 65kHz	T_A = − 40 to 25°C	0,065	14,5	18	
				T_A = 85°C		19,5	60	
				T_A = 105°C		26	65	
				T_A = 125°C		42	160	
			MSI clock=131 kHz, f_{HCLK}= 131 kHz	T_A = − 40 to 25°C	0,131	26,5	30	
				T_A = 55°C		27,5	60	
				T_A = 85°C		31	66	
				T_A = 105°C		37,5	77	
				T_A = 125°C		53,5	170	
		All peripherals OFF, code executed from Flash memory, VDD from 1.65 V to 3.6 V	MSI clock = 65 kHz, f_{HCLK}= 32 kHz	T_A = − 40 to 25°C	0,032	24,5	34	
				T_A = 85°C		30	82	
				T_A = 105°C		38,5	90	
				T_A = 125°C		58	120	
			MSI clock = 65 kHz, f_{HCLK}= 65 kHz	T_A = − 40 to 25°C	0,065	30,5	40	
				T_A = 85°C		36,5	88	
				T_A = 105°C		45	96	
				T_A = 125°C		64,5	120	
			MSI clock = 131 kHz, f_{HCLK}= 131 kHz	T_A = − 40 to 25°C	0,131	45	56	
				T_A = 55°C		48	96	
				T_A = 85°C		51	110	
				T_A = 105°C		59,5	120	
				T_A = 125°C		79,5	150	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Table 41. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	5.0	8	µs
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	7.3	13	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	13	23	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	28	38	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	51	65	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	100	120	
		f_{HCLK} = MSI = 65 kHz	190	260	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	7.9	10	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	65	130	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.2	3	ms

6.3.7 Internal clock source characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

High-speed internal 16 MHz (HSI16) RC oscillator

Table 46. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$ACC_{HSI16}^{(2)}$	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = − 40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 25. HSI16 minimum and maximum value versus temperature

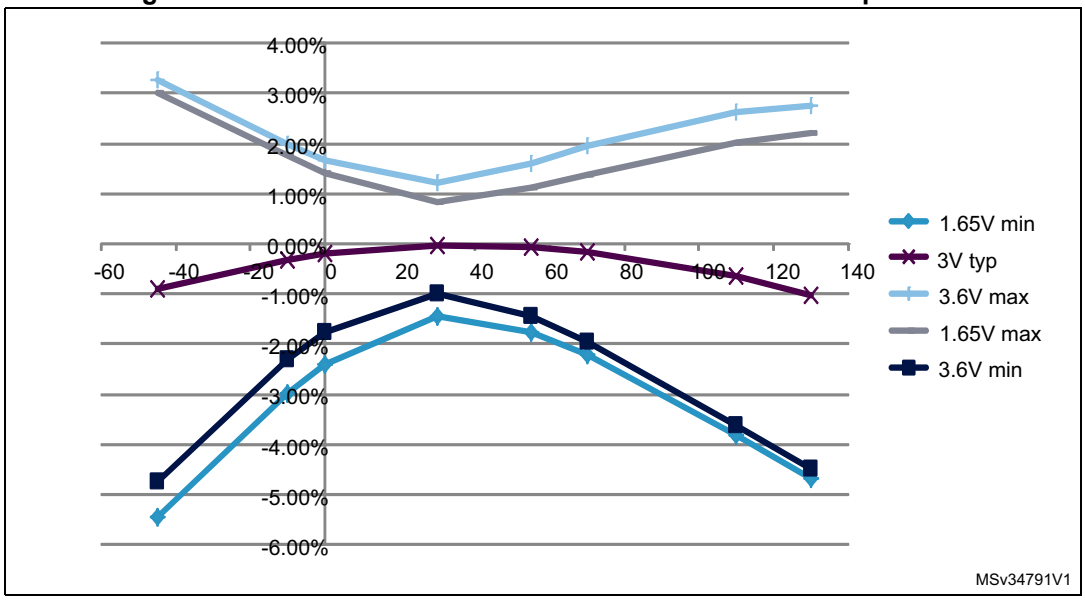


Figure 26. V_{IH}/V_{IL} versus VDD (CMOS I/Os)

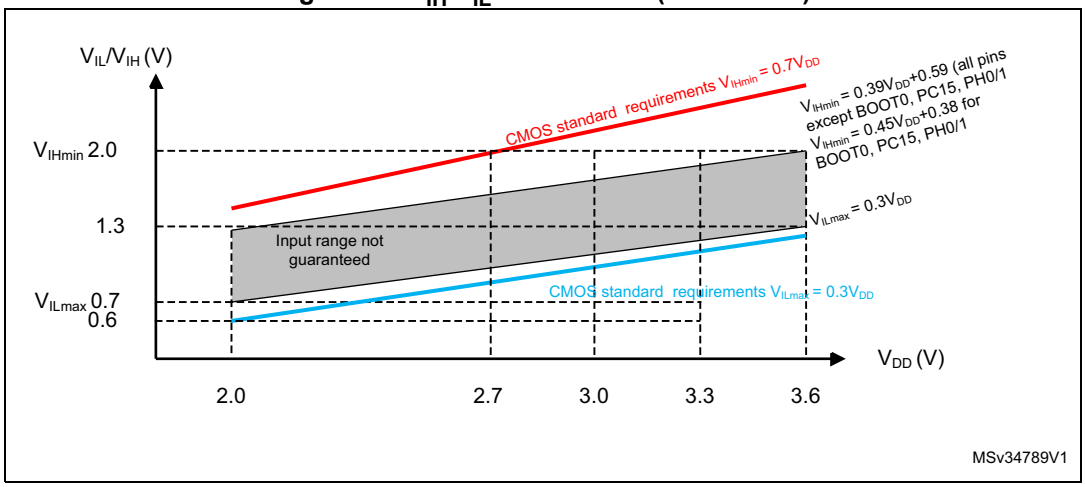
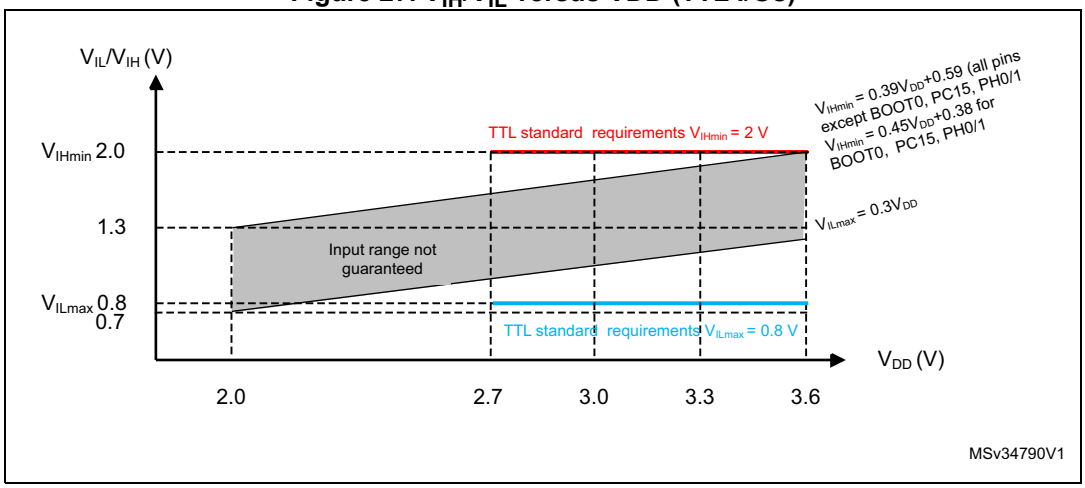


Figure 27. V_{IH}/V_{IL} versus VDD (TTL I/Os)



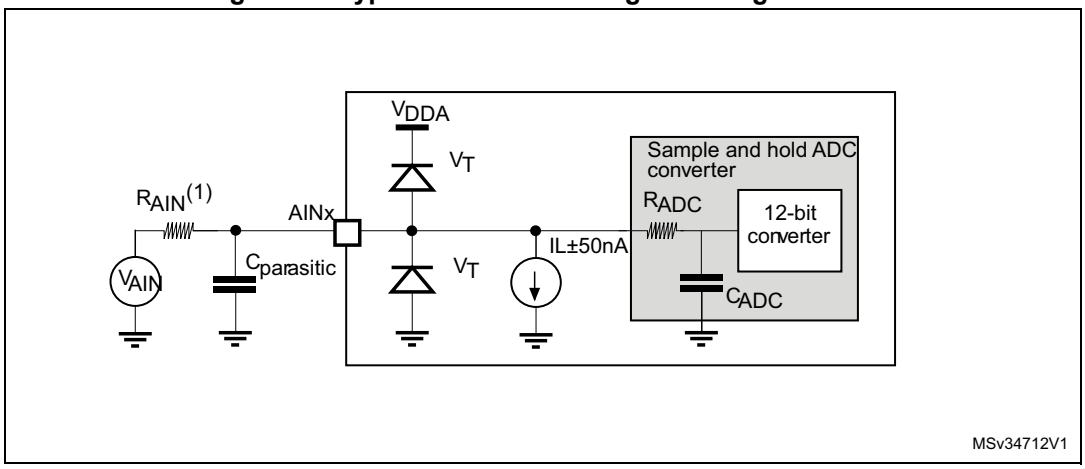
Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 59*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 23*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 23*).

Figure 31. Typical connection diagram using the ADC



1. Refer to *Table 62: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 32* or *Figure 33*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 32. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

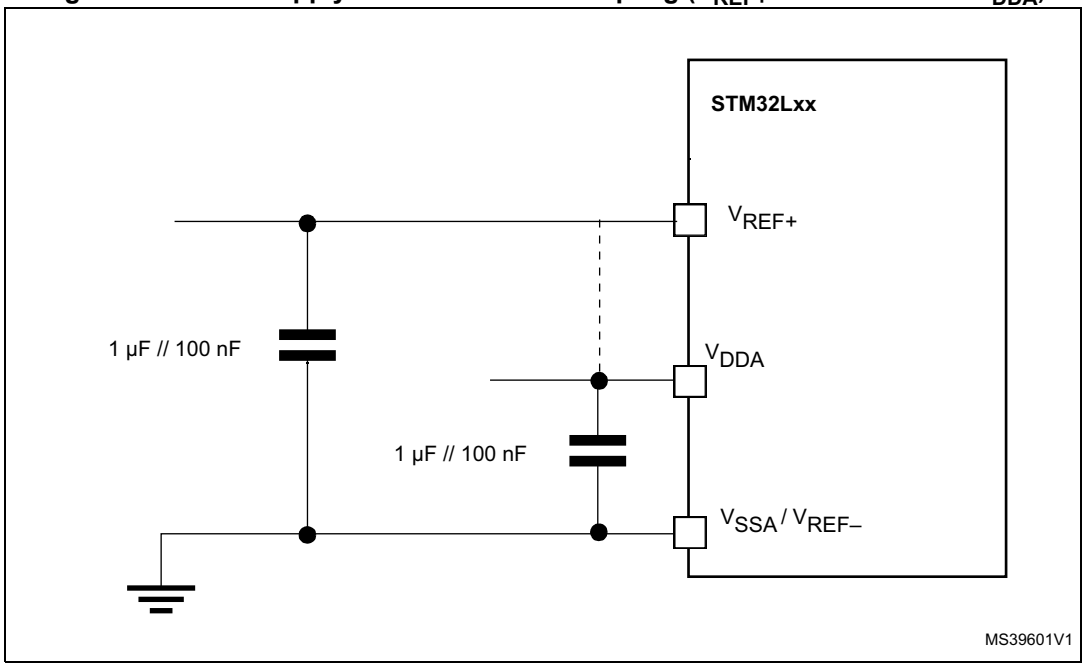
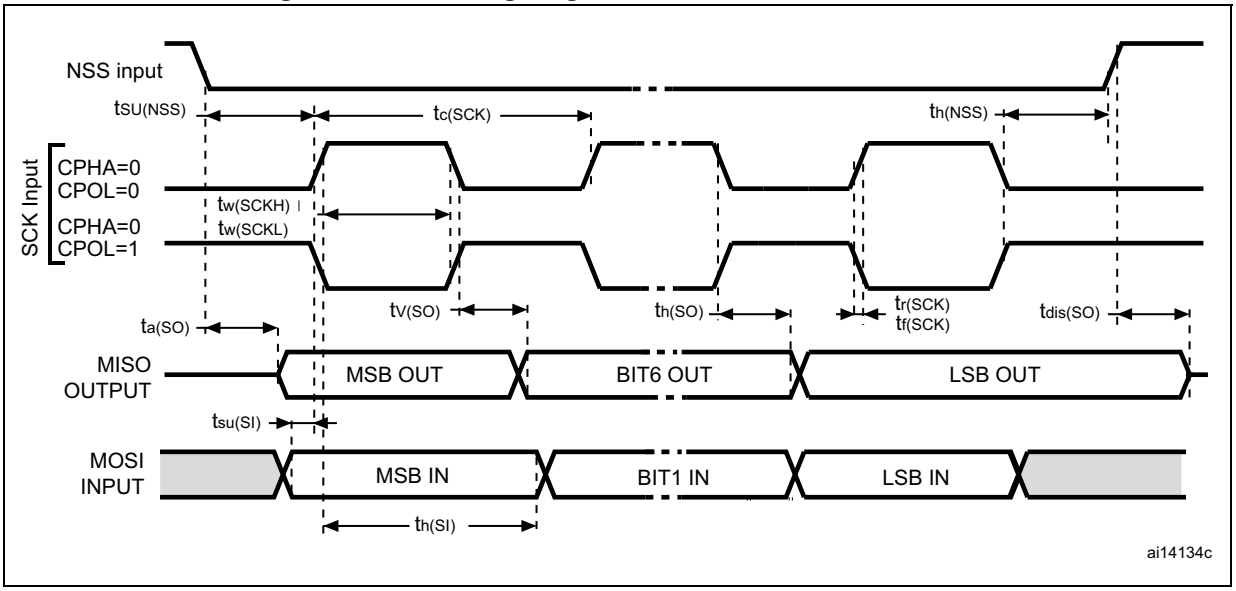


Table 74. SPI characteristics in voltage Range 3 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			2(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	
$t_{su(SI)}$		Slave mode	6	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	13.5	-	-	
$t_{h(SI)}$		Slave mode	16	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	30	70	
$t_{v(MO)}$		Master mode	-	7	9	
$t_{h(SO)}$	Data output hold time	Slave mode	25	-	-	
$t_{h(MO)}$		Master mode	8	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

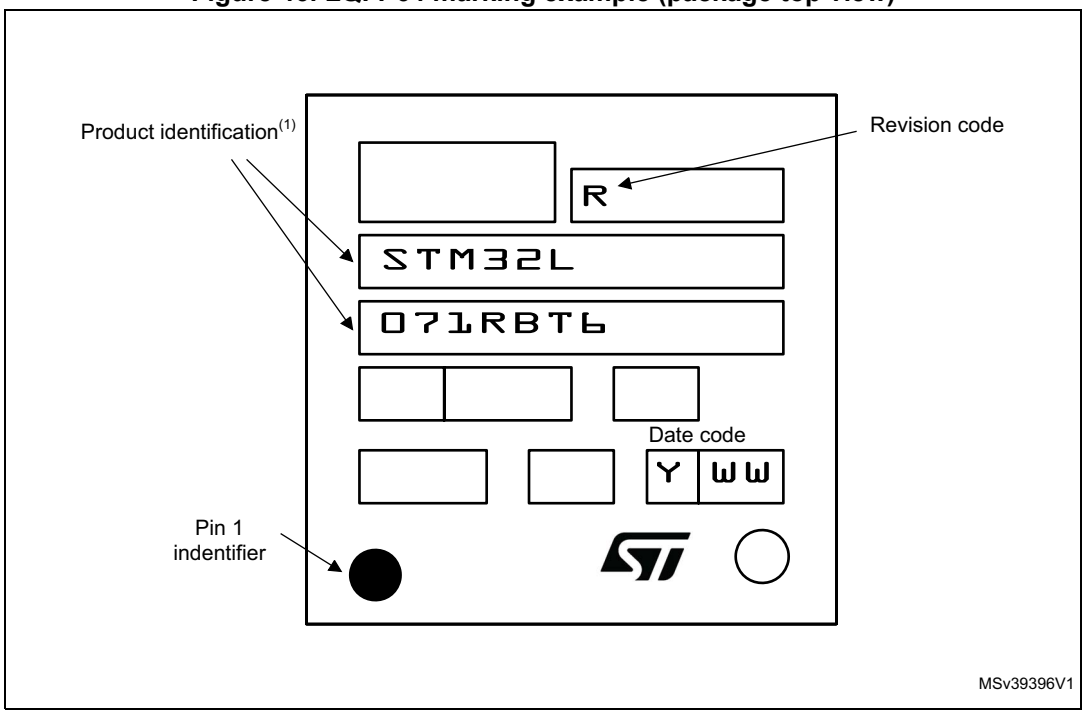
Figure 34. SPI timing diagram - slave mode and CPHA = 0



Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 46. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 80. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball ,grid array recommended footprint

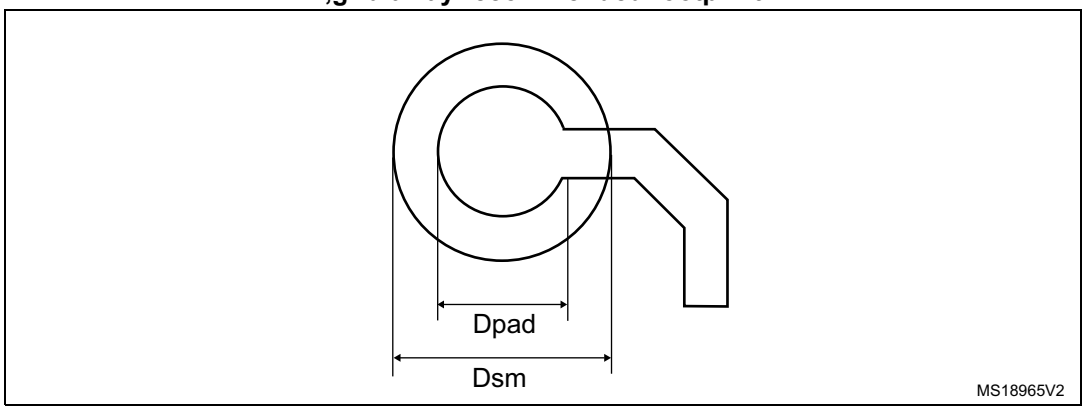


Table 81. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

Table 82. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.259	3.294	3.329	0.1283	0.1297	0.1311
E	3.223	3.258	3.293	0.1269	0.1283	0.1296
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.447	-	-	0.0176	-
G	-	0.429	-	-	0.0169	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 51. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale recommended footprint