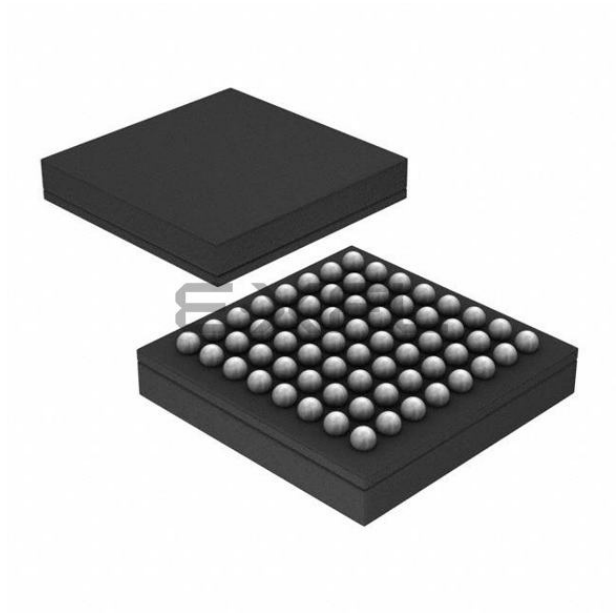

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071rbh6

2.1 Device overview

Table 2. Ultra-low-power STM32L071xx device features and peripheral counts

Peripheral		STM32L 071K8	STM32L 071C8	STM32L 071V8	STM32L 071KB	STM32L 071CB	STM32L 071VB	STM32L 071RB	STM32L 071KZ	STM32L 071CZ	STM32L 071VZ	STM32L 071RZ
Flash (Kbytes)		64 Kbytes			128 Kbytes				192 Kbytes			
Data EEPROM (Kbytes)		3 Kbytes			6 Kbytes							
RAM (Kbytes)		20 Kbytes										
Timers	General-purpose	4										
	Basic	2										
	LPTIMER	1										
RTC/SYSTICK/IWDG /WWDG		1/1/1/1										
Com. interfaces	SPI/I2S	4(3)[1]/0	6(4)[2]/1		4(3)[1]/0	6(4)[2]/1			4(3)[1]/0	6(4)[2]/1		
	I^2C	2	3		2	3			2	3		
	USART	3	4		3	4			3	4		
	LPUART	1										
GPIOs		23	37	84	25[3]	40[4]	84	51[5]	25[3]	40[4]	84	51[5]
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1										
12-bit synchronized ADC Number of channels		1 10	1 13	1 16	1 10	1 13[4]	1 16	1 16[5]	1 10	1 13[4]	1 16	1 16[5]
Comparators		2										
Max. CPU frequency		32 MHz										
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 to 3.6 V without BOR option										
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C										
Packages		UFQFPN 32	LQFP48	LQFP/ UFBGA 100	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64	UFQFPN/ LQFP32	LQFP48, WLCSP49	LQFP/ UFBGA 100	LQFP/ TFBGA 64

1. 3 SPI interfaces are USARTs operating in SPI master mode.
2. 4 SPI interfaces are USARTs operating in SPI master mode.
3. UFQFPN32 has 2 GPIOs less than LQFP32.
4. LQFP48 has three GPIOs less than WLCSP49.
5. TFBGA64 has one GPIO, one ADC input less than LQFP64.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L071xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

  Stop mode with RTC

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

3.8 Memories

The STM32L071xx devices have the following features:

- 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 64, 128 or 192 Kbytes of embedded Flash program memory
  - 6 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 8 Kbytes of system memory

Flash program and data EEPROM are divided into two banks. This allows writing in one bank while running code or reading data from the other bank.

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1(PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), I2C1 (PB6, PB7) or I2C2 (PB10, PB11), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	11	-	-	18	K2	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD	ADC_IN13
-	4	8	12	F1	-	19	J1	VSSA	S		-	-	-
-	-	-	-	-	-	20	K1	VREF-	S		-	-	-
-	-	-	-	G1	E6	21	L1	VREF+	S		-	-	-
5	5	9	13	H1	F7	22	M1	VDDA	S		-	-	-
6	6	10	14	G2	E5	23	L2	PA0	I/O	TTa	-	TIM2_CH1, USART2_CTS, TIM2_ETR, USART4_TX, COMP1_OUT	COMP1_INM, ADC_IN0, RTC_TAMP2/WKUP1
7	7	11	15	H2	E4	24	M2	PA1	I/O	FT	-	EVENTOUT, TIM2_CH2, USART2_RTS_DE, TIM21_ETR, USART4_RX	COMP1_INP, ADC_IN1
8	8	12	16	F3	F6	25	K3	PA2	I/O	FT	-	TIM21_CH1, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT	COMP2_INM, ADC_IN2
9	9	13	17	G3	G7	26	L3	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
-	-	-	18	C2	-	27	D3	VSS	S	-	-	-	-
-	-	-	19	D2	-	28	H3	VDD	S	-	-	-	-
10	10	14	20	H3	F5	29	M3	PA4	I/O	TC	-	SPI1_NSS, USART2_CK, TIM22_ETR	COMP1_INM, COMP2_INM, ADC_IN4
11	11	15	21	F4	G6	30	K4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
12	12	16	22	G4	G5	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM3_CH1, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
13	13	17	23	H4	F4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM3_CH2, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	-	-	24	H5	-	33	K5	PC4	I/O	FT	-	EVENTOUT, LPUART1_TX	ADC_IN14
-	-	-	25	H6	-	34	L5	PC5	I/O	FT	-	LPUART1_RX	ADC_IN15
14	14	18	26	F5	G4	35	M5	PB0	I/O	FT	-	EVENTOUT, TIM3_CH3	ADC_IN8, VREF_OUT
15	15	19	27	G5	D3	36	M6	PB1	I/O	FT	-	TIM3_CH4, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
-	-	20	28	G6	E3	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, I2C3_SMBA	-
-	-	-	-	-	-	38	M7	PE7	I/O	FT	-	USART5_CK/USART5_RTS_DE	-
-	-	-	-	-	-	39	L7	PE8	I/O	FT	-	USART4_TX	-
-	-	-	-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, TIM2_ETR, USART4_RX	-
-	-	-	-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, USART5_TX	-
-	-	-	-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	-
-	-	-	-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	-
-	-	-	-	-	-	44	M10	PE13	I/O	FT	-	SPI1_SCK	-
-	-	-	-	-	-	45	M11	PE14	I/O	FT	-	SPI1_MISO	-
-	-	-	-	-	-	46	M12	PE15	I/O	FT	-	SPI1_MOSI	-

Table 15. STM32L071xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64	WLCSP49	LQFP100	UFBG100						
30	29	43	59	C3	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	60	B4	A5	94	A4	BOOT0	I		-	-	-
-	-	45	61	B3	B5	95	A3	PB8	I/O	FTf	-	I2C1_SCL	-
-	-	46	62	A3	A6	96	B3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	31	47	63	D4	-	99	D3	VSS	S		-	-	-
-	32	48	64	E4	A7	100	C4	VDD	S		-	-	-

1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 25*.

Table 26. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Figure 20. I_{DD} vs V_{DD}, at T_A= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off

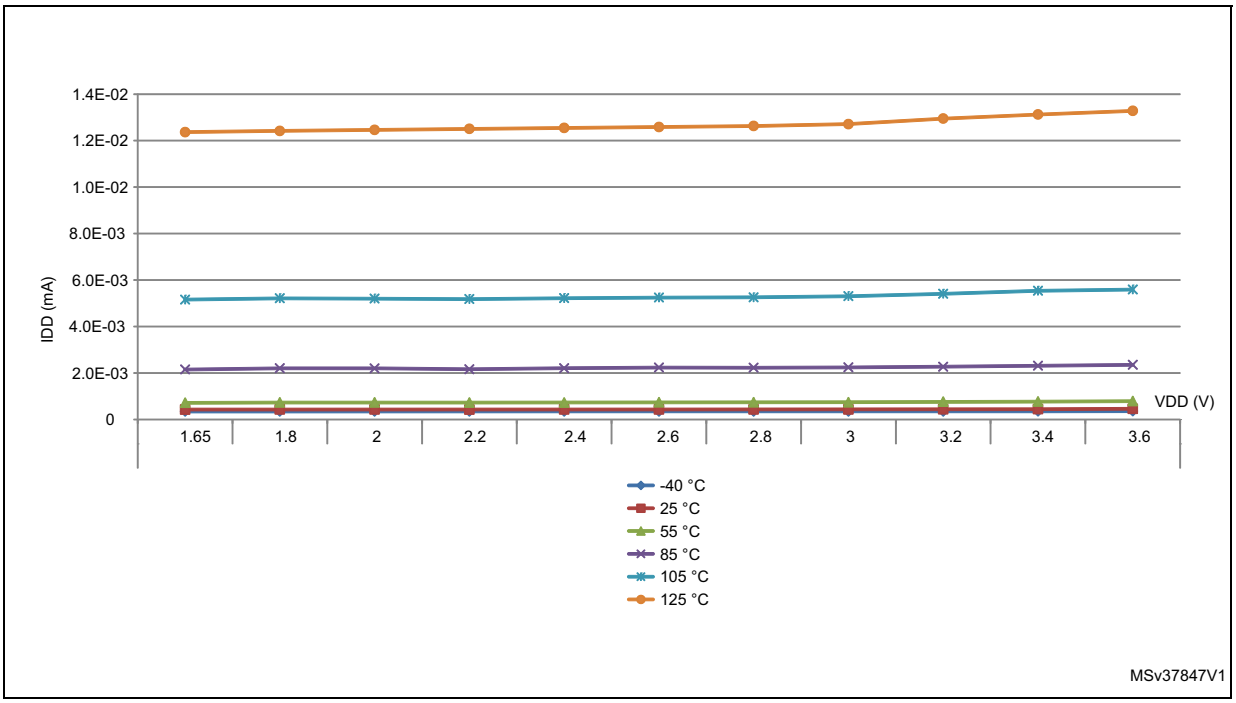


Table 37. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
I_{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	T_A = − 40 to 25°C	0,855	1,70	µA
			T_A = 55 °C	-	2,90	
			T_A= 85 °C	-	3,30	
			T_A = 105 °C	-	4,10	
			T_A = 125 °C	-	8,50	
		Independent watchdog and LSI off	T_A = − 40 to 25°C	0,29	0,60	
			T_A = 55 °C	0,32	1,20	
			T_A = 85 °C	0,5	2,30	
			T_A = 105 °C	0,94	3,00	
			T_A = 125 °C	2,6	7,00	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
G_m	Maximum critical crystal transconductance	Startup	-	-	700	µA /V
$t_{SU(HSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 23*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 23. HSE oscillator circuit diagram

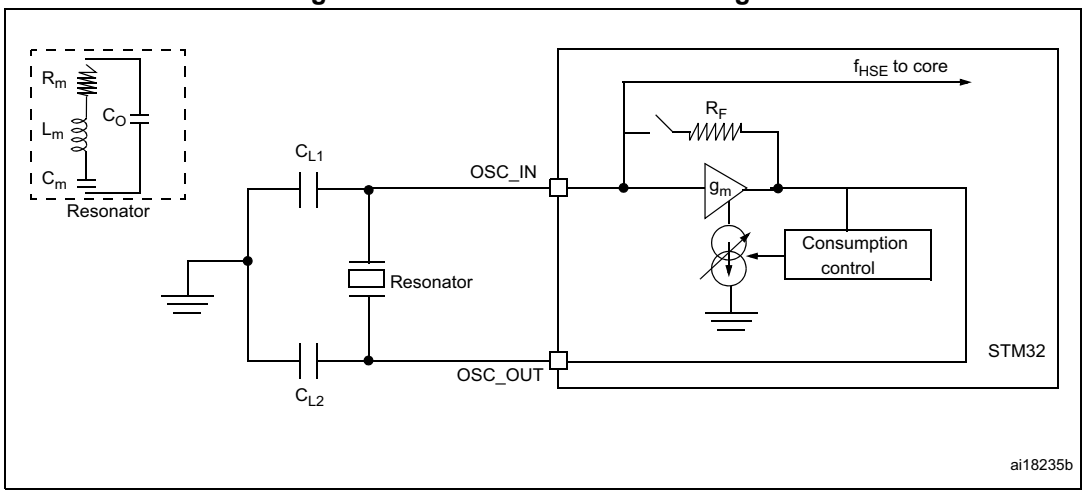


Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

Table 51. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 52. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T_A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T_A = 105 °C			
	Data retention (program memory) after 200 cycles at T_A = 125 °C	T_{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T_A = 125 °C			

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

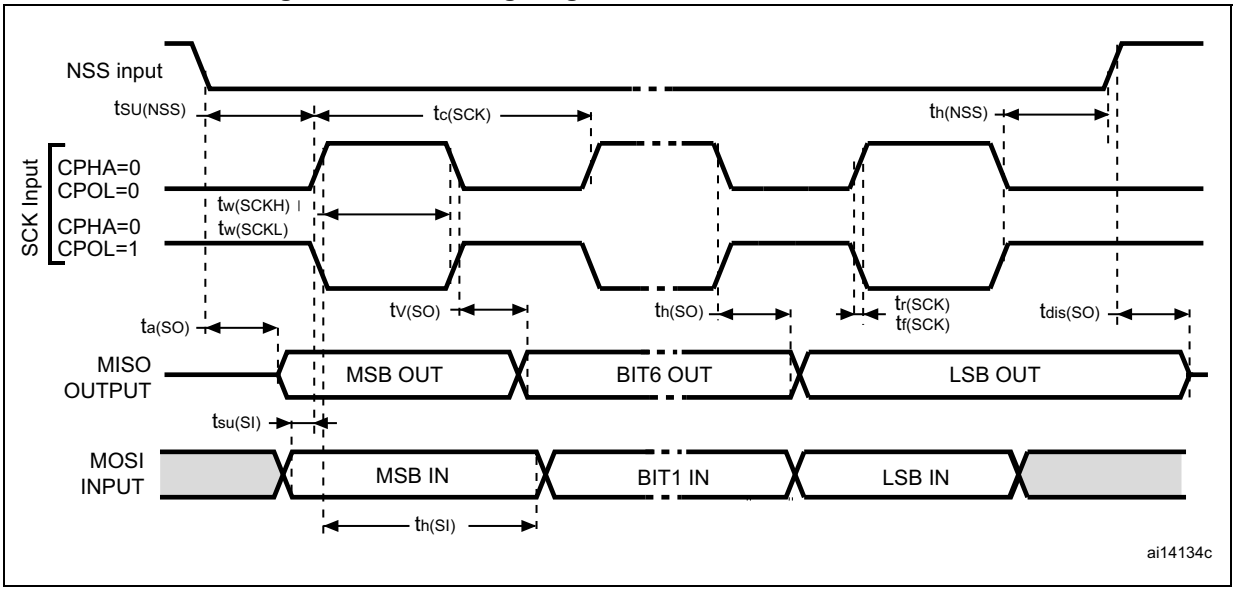
Susceptibility tests are performed on a sample basis during device characterization.

Table 74. SPI characteristics in voltage Range 3 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			2(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	
$t_{su(SI)}$		Slave mode	6	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	13.5	-	-	
$t_{h(SI)}$		Slave mode	16	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	30	70	
$t_{v(MO)}$		Master mode	-	7	9	
$t_{h(SO)}$	Data output hold time	Slave mode	25	-	-	
$t_{h(MO)}$		Master mode	8	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 34. SPI timing diagram - slave mode and CPHA = 0



I2S characteristics

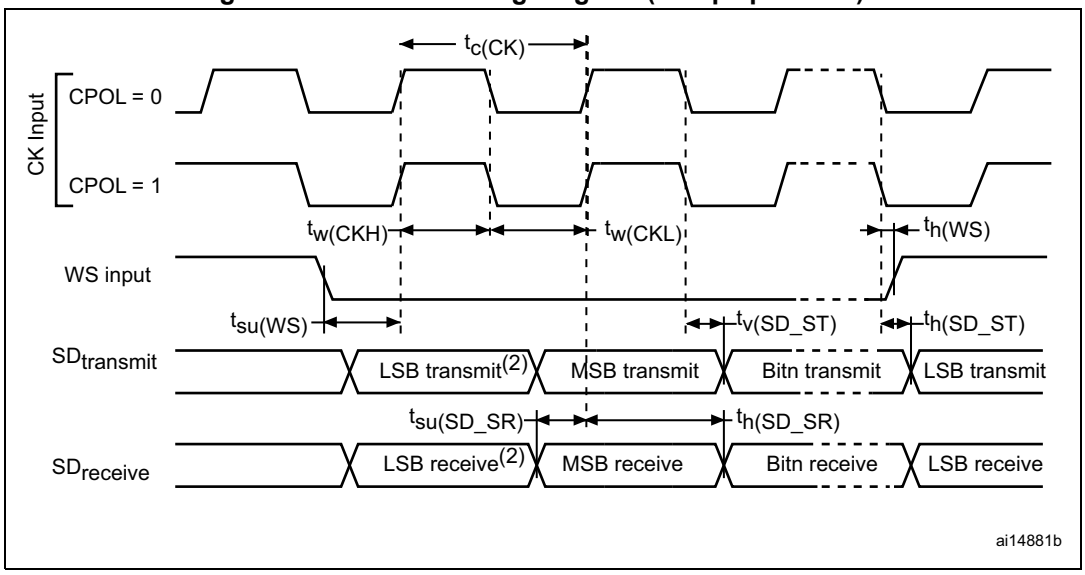
Table 75. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	15	ns
$t_{h(WS)}$	WS hold time	Master mode	11	-	
$t_{su(WS)}$	WS setup time	Slave mode	6	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	6.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	18	-	
$t_{h(SD\_SR)}$		Slave receiver	15.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	77	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	8	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	18	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1.5	-	

1. Guaranteed by characterization results.
2. 256xFs maximum value is equal to the maximum clock frequency.

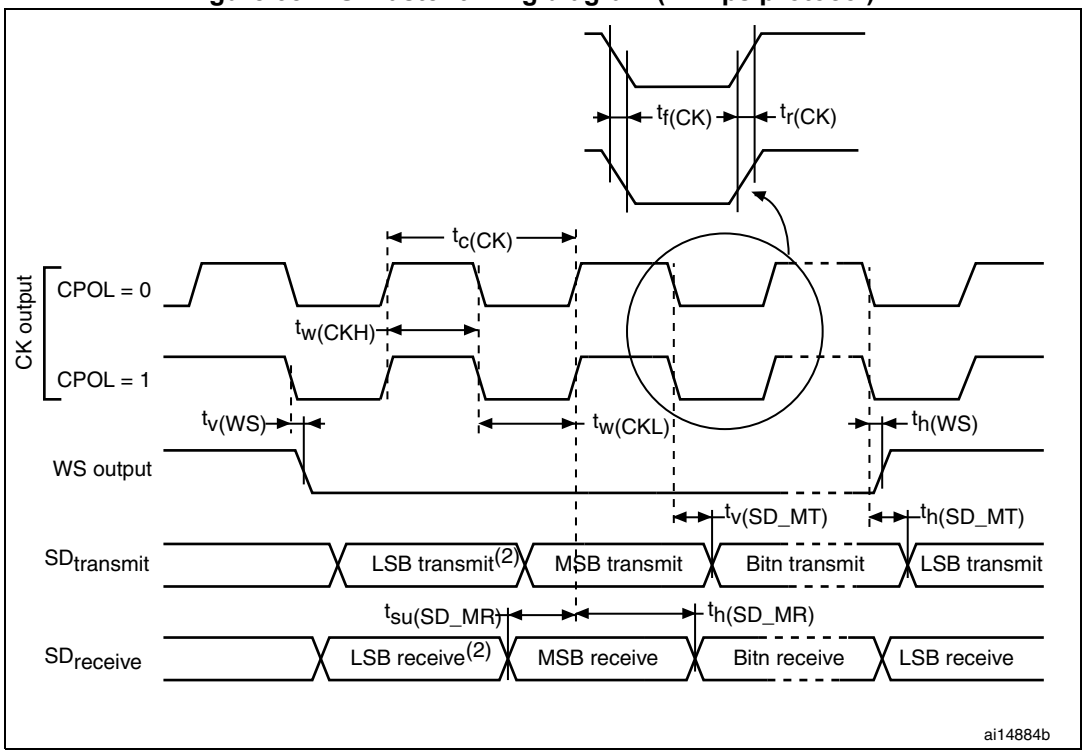
*Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 37. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 38. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 76. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

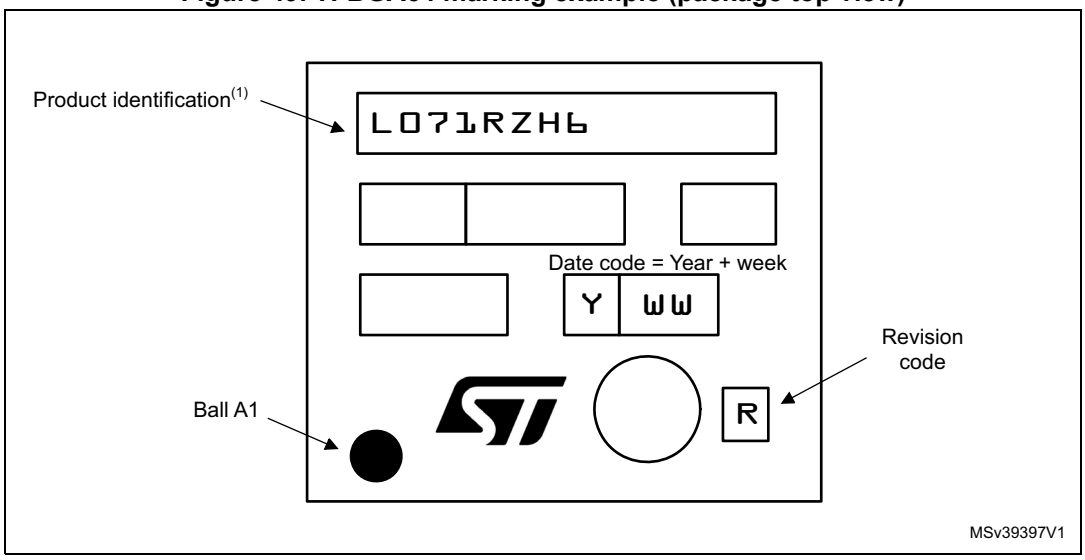
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 49. TFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

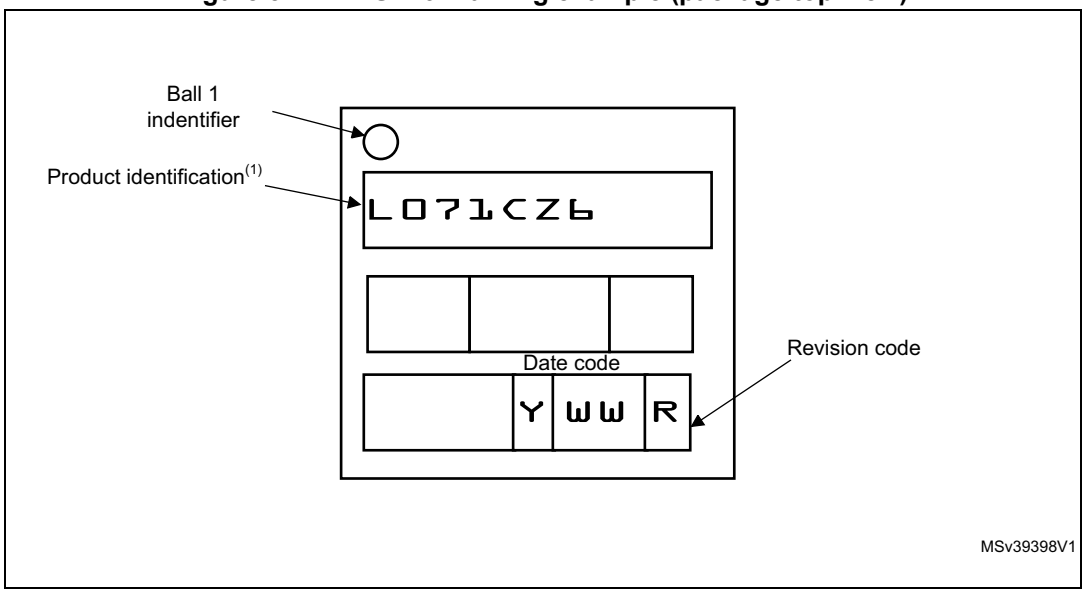
Table 83. WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Device marking for WLCSP49

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 52. WLCSP49 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.9 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 87. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	36	°C/W
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	54	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	48	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	64	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm / 0.5 mm pitch	57	