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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 6K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071rbt6tr |

# 3 Functional overview

## 3.1 Low-power modes

The ultra-low-power STM32L071xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 ($V_{DD}$ range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full $V_{DD}$ range), with a maximum CPU frequency of 16 MHz
- Range 3 (full $V_{DD}$ range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

  **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the $V_{CORE}$ domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USART/I2C/LPUART/LPTIMER wakeup events.

**Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]**

| IPs | Run/Active | Sleep | Low-power run | Low-power sleep | Stop | | Standby | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Wakeup capability | | Wakeup capability |
| High Speed External (HSE) | O | O | O | O | -- | | -- | |
| Low Speed Internal (LSI) | O | O | O | O | O | | O | |
| Low Speed External (LSE) | O | O | O | O | O | | O | |
| Multi-Speed Internal (MSI) | O | O | Y | Y | -- | | -- | |
| Inter-Connect Controller | Y | Y | Y | Y | Y | | -- | |
| RTC | O | O | O | O | O | O | O | |
| RTC Tamper | O | O | O | O | O | O | O | O |
| Auto WakeUp (AWU) | O | O | O | O | O | O | O | O |
| USART | O | O | O | O | O[4] | O | -- | |
| LPUART | O | O | O | O | O[4] | O | -- | |
| SPI | O | O | O | O | -- | | -- | |
| I2C | O | O | O | O | O[5] | O | -- | |
| ADC | O | O | -- | -- | -- | | -- | |
| Temperature sensor | O | O | O | O | O | | -- | |
| Comparators | O | O | O | O | O | O | -- | |
| 16-bit timers | O | O | O | O | -- | | -- | |
| LPTIMER | O | O | O | O | O | O | | |
| IWDG | O | O | O | O | O | O | O | O |
| WWDG | O | O | O | O | -- | | -- | |
| SysTick Timer | O | O | O | O | | | -- | |
| GPIOs | O | O | O | O | O | O | | 2 pins |
| Wakeup time to Run mode | 0 µs | 0.36 µs | 3 µs | 32 µs | 3.5 µs | | 50 µs | |

**Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)[1][2]**

| IPs | Run/Active | Sleep | Low-power run | Low-power sleep | Stop | Standby |
|---|---|---|---|---|---|---|
| | | | | | Wakeup capability | Wakeup capability |
| Consumption $V_{DD}$=1.8 to 3.6 V (Typ) | Down to 140 µA/MHz (from Flash memory) | Down to 37 µA/MHz (from Flash memory) | Down to 8 µA | Down to 4.5 µA | 0.4 µA (No RTC) $V_{DD}$=1.8 V | 0.28 µA (No RTC) $V_{DD}$=1.8 V |
| | | | | | 0.8 µA (with RTC) $V_{DD}$=1.8 V | 0.65 µA (with RTC) $V_{DD}$=1.8 V |
| | | | | | 0.4 µA (No RTC) $V_{DD}$=3.0 V | 0.29 µA (No RTC) $V_{DD}$=3.0 V |
| | | | | | 1 µA (with RTC) $V_{DD}$=3.0 V | 0.85 µA (with RTC) $V_{DD}$=3.0 V |

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional can be enabled/disabled by software)
   "-" = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

## 3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

**Table 6. STM32L0xx peripherals interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action | Run | Sleep | Low-power run | Low-power sleep | Stop |
|---|---|---|---|---|---|---|---|
| COMPx | TIM2,TIM21, TIM22 | Timer input channel, trigger from analog signals comparison | Y | Y | Y | Y | - |
| | LPTIM | Timer input channel, trigger from analog signals comparison | Y | Y | Y | Y | Y |
| TIMx | TIMx | Timer triggered by other timer | Y | Y | Y | Y | - |

## 3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

## 3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

### Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 84 GPIOs can be connected to the 16 configurable interrupt/event lines. The 13 other lines are connected to PVD, RTC, USARTs, I2C, LPUART, LPTIMER or comparator events.

### 3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The four USART interfaces (USART1, USART2, USART4 and USART5) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

*Table 12* for the supported modes and features of USART interfaces.

**Table 12. USART implementation**

| USART modes/features(1) | USART1 and USART2 | USART4 and USART5 |
|---|---|---|
| Hardware flow control for modem | X | X |
| Continuous communication using DMA | X | X |
| Multiprocessor communication | X | X |
| Synchronous mode(2) | X | X |
| Smartcard mode | X | - |
| Single-wire half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | - |
| LIN mode | X | - |
| Dual clock domain and wakeup from Stop mode | X | - |
| Receiver timeout interrupt | X | - |
| Modbus communication | X | - |
| Auto baud rate detection (4 modes) | X | - |
| Driver Enable | X | X |

1. X = supported.
2. This mode allows using the USART as an SPI master.

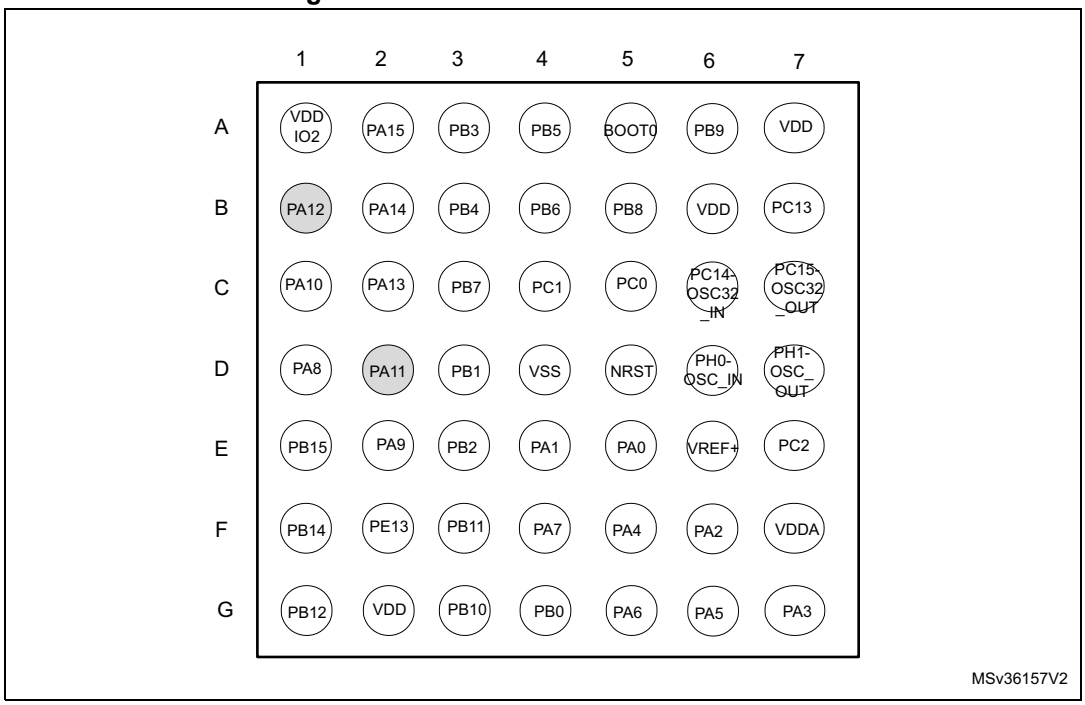
### 3.15.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

**Figure 7. STM32L071xx WLCSP49 ballout**




1. The above figure shows the package top view.
2. I/O supplied by VDDIO2.

Table 15. STM32L071xxx pin definition (continued)

| Pin number | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Note | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP32 | UFQFPN32[1] | LQFP48 | LQFP64 | UFBGA64 | WLCSP49 | LQFP100 | UFBG100 | | | | | | |
| - | - | - | 39 | E8 | - | 65 | E10 | PC8 | I/O | FT | - | TIM22_ETR, TIM3_CH3 | - |
| - | - | - | 40 | D8 | - | 66 | D12 | PC9 | I/O | FTf | - | TIM21_ETR, TIM3_CH4, I2C3_SDA | - |
| 18 | 18 | 29 | 41 | D7 | D1 | 67 | D11 | PA8 | I/O | FTf | - | MCO, EVENTOUT, USART1_CK, I2C3_SCL | - |
| 19 | 19 | 30 | 42 | C7 | E2 | 68 | D10 | PA9 | I/O | FTf | - | MCO, USART1_TX, I2C1_SCL, I2C3_SMBA | - |
| 20 | 20 | 31 | 43 | C6 | C1 | 69 | C12 | PA10 | I/O | FTf | - | USART1_RX, I2C1_SDA | - |
| 21 | 21 | 32 | 44 | C8 | D2 | 70 | B12 | PA11 | I/O | FT | - | SPI1_MISO, EVENTOUT, USART1_CTS, COMP1_OUT | - |
| 22 | 22 | 33 | 45 | B8 | B1 | 71 | A12 | PA12 | I/O | FT | - | SPI1_MOSI, EVENTOUT, USART1_RTS_DE, COMP2_OUT | - |
| 23 | 23 | 34 | 46 | A8 | C2 | 72 | A11 | PA13 | I/O | FT | - | SWDIO, LPUART1_RX | - |
| - | - | - | - | - | - | 73 | C11 | VDD | S | | - | - | - |
| - | - | 35 | 47 | D5 | - | 74 | F11 | VSS | S | | - | - | - |
| - | 24 | 36 | 48 | E5 | A1 | 75 | G11 | VDDIO2 | S | | - | - | - |
| 24 | 25 | 37 | 49 | A7 | B2 | 76 | A10 | PA14 | I/O | FT | - | SWCLK, USART2_TX, LPUART1_TX | - |
| 25 | - | 38 | 50 | A6 | A2 | 77 | A9 | PA15 | I/O | FT | - | SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE | - |
| - | - | - | 51 | B7 | - | 78 | B11 | PC10 | I/O | FT | - | LPUART1_TX, USART4_TX | - |
| - | - | - | 52 | B6 | - | 79 | C10 | PC11 | I/O | FT | - | LPUART1_RX, USART4_RX | - |
| - | - | - | 53 | C5 | - | 80 | B10 | PC12 | I/O | FT | - | USART5_TX, USART4_CK | - |

Table 16. Alternate functions port A

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/I2S2/USART1/2/LPUART1/LPTIM1/TIM2/21/22/EVENTOUT/SYS_AF | SPI1/SPI2/I2S2/I2C1/TIM2/21 | SPI1/SPI2/I2S2/LPUART1/USART5/LPTIM1/TIM2/3/EVENTOUT/SYS_AF | I2C1/EVENTOUT | I2C1/USART1/2/LPUART1/TIM3/22/EVENTOUT | SPI2/I2S2/I2C2/USART1/TIM2/21/22 | I2C1/2/LPUART1/USART4/UASRT5/TIM21/EVENTOUT | I2C3/LPUART1/COMP1/2/TIM3 |
| Port A | PA0 | - | - | TIM2_CH1 | | USART2_CTS | TIM2_ETR | USART4_TX | COMP1_OUT |
| | PA1 | EVENTOUT | | TIM2_CH2 | | USART2_RTS_DE | TIM21_ETR | USART4_RX | - |
| | PA2 | TIM21_CH1 | | TIM2_CH3 | | USART2_TX | - | LPUART1_TX | COMP2_OUT |
| | PA3 | TIM21_CH2 | | TIM2_CH4 | | USART2_RX | - | LPUART1_RX | - |
| | PA4 | SPI1_NSS | - | - | | USART2_CK | TIM22_ETR | - | - |
| | PA5 | SPI1_SCK | - | TIM2_ETR | | | TIM2_CH1 | - | - |
| | PA6 | SPI1_MISO | | TIM3_CH1 | | LPUART1_CTS | TIM22_CH1 | EVENTOUT | COMP1_OUT |
| | PA7 | SPI1_MOSI | | TIM3_CH2 | | - | TIM22_CH2 | EVENTOUT | COMP2_OUT |
| | PA8 | MCO | | | EVENTOUT | USART1_CK | - | - | I2C3_SCL |
| | PA9 | MCO | | - | | USART1_TX | - | I2C1_SCL | I2C3_SMBA |
| | PA10 | - | | - | | USART1_RX | - | I2C1_SDA | - |
| | PA11 | SPI1_MISO | - | EVENTOUT | | USART1_CTS | - | - | COMP1_OUT |
| | PA12 | SPI1_MOSI | - | EVENTOUT | | USART1_RTS_DE | - | - | COMP2_OUT |
| | PA13 | SWDIO | - | | - | - | - | LPUART1_RX | - |
| | PA14 | SWCLK | - | - | - | USART2_TX | - | LPUART1_TX | - |
| | PA15 | SPI1_NSS | | TIM2_ETR | EVENTOUT | USART2_RX | TIM2_CH1 | USART4_RTS_DE | - |

**Table 17. Alternate functions port B**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2/I 2C1/TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/LPTIM 1/TIM2/3/EVENT OUT/ SYS_AF | I2C1/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2/I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT | I2C3/LPUART1/ COMP1/2/ TIM3 |
| Port B | PB0 | EVENTOUT | | TIM3_CH3 | | - | - | - | - |
| | PB1 | - | | TIM3_CH4 | | LPUART1_RTS_DE | - | - | - |
| | PB2 | - | - | LPTIM1_OUT | | - | - | - | I2C3_SMBA |
| | PB3 | SPI1_SCK | | TIM2_CH2 | | EVENTOUT | USART1_RTS_DE | USART5_TX | - |
| | PB4 | SPI1_MISO | | TIM3_CH1 | | TIM22_CH1 | USART1_CTS | USART5_RX | I2C3_SDA |
| | PB5 | SPI1_MOSI | | LPTIM1_IN1 | I2C1_SMBA | TIM3_CH2/ TIM22_CH2 | USART1_CK | USART5_CK/ USART5_RTS_D E | - |
| | PB6 | USART1_TX | I2C1_SCL | LPTIM1_ETR | | - | - | - | - |
| | PB7 | USART1_RX | I2C1_SDA | LPTIM1_IN2 | | - | - | USART4_CTS | - |
| | PB8 | - | | - | | I2C1_SCL | - | - | - |
| | PB9 | - | | EVENTOUT | - | I2C1_SDA | SPI2_NSS/ I2S2_WS | - | - |
| | PB10 | - | | TIM2_CH3 | | LPUART1_TX | SPI2_SCK | I2C2_SCL | LPUART1_RX |
| | PB11 | EVENTOUT | | TIM2_CH4 | | LPUART1_RX | - | I2C2_SDA | LPUART1_TX |
| | PB12 | SPI2_NSS/I2S2_WS | | LPUART1_RTS_ DE | | | I2C2_SMBA | EVENTOUT | - |
| | PB13 | SPI2_SCK/I2S2_CK | | MCO | | LPUART1_CTS | I2C2_SCL | TIM21_CH1 | - |
| | PB14 | SPI2_MISO/ I2S2_MCK | | RTC_OUT | | LPUART1_RTS_DE | I2C2_SDA | TIM21_CH2 | - |
| | PB15 | SPI2_MOSI/ I2S2_SD | | RTC_REFIN | - | - | - | - | - |

**Table 19. Alternate functions port D**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1/SPI2/I2S2/ USART1/2/ LPUART1/ LPTIM1/ TIM2/21/22/ EVENTOUT/ SYS_AF | SPI1/SPI2/I2S2/I2C1/ TIM2/21 | SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF | I2C1/ EVENTOUT | I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT | SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22 | I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/E VENTOUT | I2C3/LPUART1/ COMP1/2/TIM3 |
| Port D | PD0 | TIM21_CH1 | SPI2_NSS/I2S2_WS | - | - | - | - | - | - |
| | PD1 | - | SPI2_SCK/I2S2_CK | - | - | - | - | - | - |
| | PD2 | LPUART1_RTS_ DE | | TIM3_ETR | - | - | - | USART5_RX | - |
| | PD3 | USART2_CTS | | SPI2_MISO/ I2S2_MCK | - | - | - | - | - |
| | PD4 | USART2_RTS_D E | SPI2_MOSI/I2S2_SD | - | - | - | - | - | - |
| | PD5 | USART2_TX | - | - | - | - | - | - | - |
| | PD6 | USART2_RX | - | - | - | - | - | - | - |
| | PD7 | USART2_CK | TIM21_CH2 | - | - | - | - | - | - |
| | PD8 | LPUART1_TX | | - | - | - | - | - | - |
| | PD9 | LPUART1_RX | | - | - | - | - | - | - |
| | PD10 | - | | - | - | - | - | - | - |
| | PD11 | LPUART1_CTS | | - | - | - | - | - | - |
| | PD12 | LPUART1_RTS_ DE | | - | - | - | - | - | - |
| | PD13 | - | | - | - | - | - | - | - |
| | PD14 | - | | - | - | - | - | - | - |
| | PD15 | | | - | - | - | - | - | - |

## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 22: Voltage characteristics*, *Table 23: Current characteristics*, and *Table 24: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 22. Voltage characteristics**

| Symbol | Definition | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DDIO2}$ $V_{DD}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on FT and FTf pins | $V_{SS}$ − 0.3 | $V_{DD}$+4.0 | |
| | Input voltage on TC pins | $V_{SS}$ − 0.3 | 4.0 | |
| | Input voltage on BOOT0 | $V_{SS}$ | $V_{DD}$ + 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ − 0.3 | 4.0 | |
| $\lvert\Delta V_{DD}\rvert$ | Variations between different $V_{DDx}$ power pins | - | 50 | mV |
| $\lvert V_{DDA}-V_{DDx}\rvert$ | Variations between any $V_{DDx}$ and $V_{DDA}$ power pins(3) | - | 300 | |
| $\lvert\Delta V_{SS}\rvert$ | Variations between all different ground pins including $V_{REF-}$ pin | - | 50 | |
| $V_{REF+}$ –$V_{DDA}$ | Allowed voltage difference for $V_{REF+}$ > $V_{DDA}$ | - | 0.4 | V |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.11* | | |

1. All main power ($V_{DD}$,, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 23* for maximum allowed injected current values.
3. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and device operation. $V_{DDIO2}$ is independent from $V_{DD}$ and $V_{DDA}$: its value does not need to respect this rule.

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 25. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 32 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 32 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 32 | |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| | | BOR detector enabled, at power on | 1.8 | 3.6 | |
| | | BOR detector disabled, after power on | 1.65 | 3.6 | |
| $V_{DDA}$ | Analog operating voltage (all features) | Must be the same voltage as $V_{DD}$(1) | 1.65 | 3.6 | V |
| $V_{DDIO2}$ | Standard operating voltage | - | 1.65 | 3.6 | V |
| $V_{IN}$ | Input voltage on FT, FTf and RST pins(2) | 2.0 V ≤ $V_{DD}$ ≤ 3.6 V | -0.3 | 5.5 | V |
| | | 1.65 V ≤ $V_{DD}$ ≤ 2.0 V | -0.3 | 5.2 | |
| | Input voltage on BOOT0 pin | - | 0 | 5.5 | |
| | Input voltage on TC pin | - | -0.3 | $V_{DD}$+0.3 | |
| $P_D$ | Power dissipation at $T_A$ = 85 °C (range 6) or $T_A$ =105 °C (rage 7) (3) | UFBGA100 package | - | 351 | mW |
| | | LQFP100 package | - | 488 | |
| | | TFBGA64 package | - | 313 | |
| | | LQFP64 package | - | 435 | |
| | | WLCSP49 package | - | 417 | |
| | | LQFP48 package | - | 370 | |
| | | UFQFPN32 package | - | 556 | |
| | | LQFP32 package | - | 333 | |
| | Power dissipation at $T_A$ = 125 °C (range 3) (3) | UFBGA100 package | - | 88 | |
| | | LQFP100 package | - | 122 | |
| | | TFBGA64 package | - | 78 | |
| | | LQFP64 package | - | 109 | |
| | | WLCSP49 package | - | 104 | |
| | | LQFP48 package | - | 93 | |
| | | UFQFPN32 package | - | 139 | |
| | | LQFP32 package | - | 83 | |

**Table 40. Peripheral current consumption in Stop and Standby mode(1)**

| Symbol | Peripheral | Typical consumption, $T_A$ = 25 °C | | Unit |
|---|---|---|---|---|
| | | $V_{DD}$=1.8 V | $V_{DD}$=3.0 V | |
| $I_{DD(PVD / BOR)}$ | - | 0.7 | 1.2 | µA |
| $I_{REFINT}$ | - | - | 1.7 | |
| - | LSE Low drive(2) | 0.11 | 0,13 | |
| - | LSI | 0.27 | 0.31 | |
| - | IWDG | 0.2 | 0.3 | |
| - | LPTIM1, Input 100 Hz | 0.01 | 0,01 | |
| - | LPTIM1, Input 1 MHz | 11 | 12 | |
| - | LPUART1 | - | 0,5 | |
| - | RTC | 0.16 | 0,3 | |

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

### 6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 25*.

**Table 41. Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{WUSLEEP}$ | Wakeup from Sleep mode | $f_{HCLK}$ = 32 MHz | 7 | 8 | Number of clock cycles |
| $t_{WUSLEEP\_LP}$ | Wakeup from Low-power sleep mode, $f_{HCLK}$ = 262 kHz | $f_{HCLK}$ = 262 kHz Flash memory enabled | 7 | 8 | |
| | | $f_{HCLK}$ = 262 kHz Flash memory switched OFF | 9 | 10 | |

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

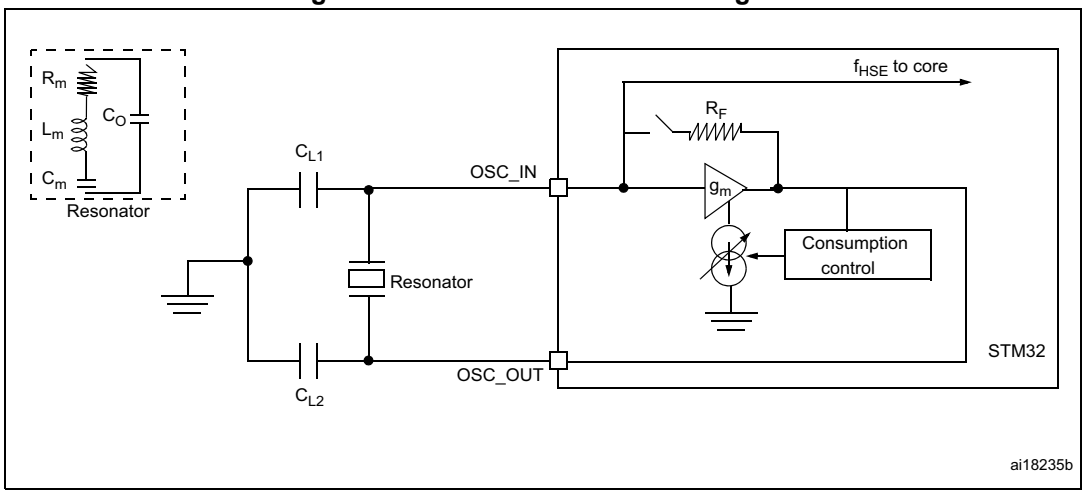
**Table 44. HSE oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 1 | | 25 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $G_m$ | Maximum critical crystal transconductance | Startup | - | - | 700 | µA /V |
| $t_{SU(HSE)}$ (2) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 23*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

**Figure 23. HSE oscillator circuit diagram**



### 6.3.8 PLL characteristics

The parameters given in *Table 49* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 25*.

**Table 49. PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max(1) | |
| $f_{PLL\_IN}$ | PLL input clock(2) | 2 | - | 24 | MHz |
| | PLL input clock duty cycle | 45 | - | 55 | % |
| $f_{PLL\_OUT}$ | PLL output clock | 2 | - | 32 | MHz |
| $t_{LOCK}$ | PLL input = 16 MHz<br>PLL VCO = 96 MHz | - | 115 | 160 | µs |
| Jitter | Cycle-to-cycle jitter | - | | ±600 | ps |
| $I_{DDA}$(PLL) | Current consumption on $V_{DDA}$ | - | 220 | 450 | µA |
| $I_{DD}$(PLL) | Current consumption on $V_{DD}$ | - | 120 | 150 | |

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

### 6.3.9 Memory characteristics

#### RAM memory

**Table 50. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VRM | Data retention mode(1) | STOP mode (or RESET) | 1.65 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

#### Flash memory and data EEPROM

**Table 51. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage<br>Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming time for word or half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |

Figure 26. $V_{IH}/V_{IL}$ versus VDD (CMOS I/Os)

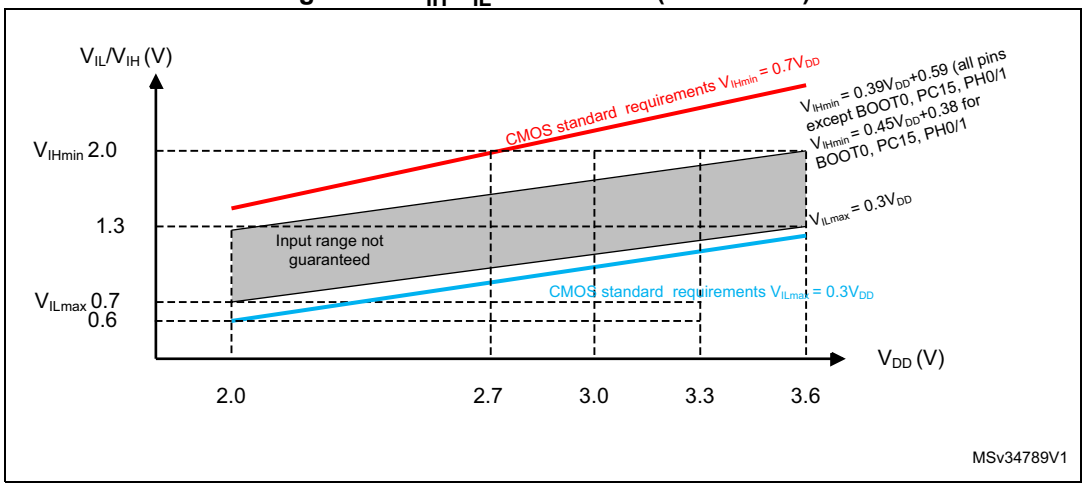
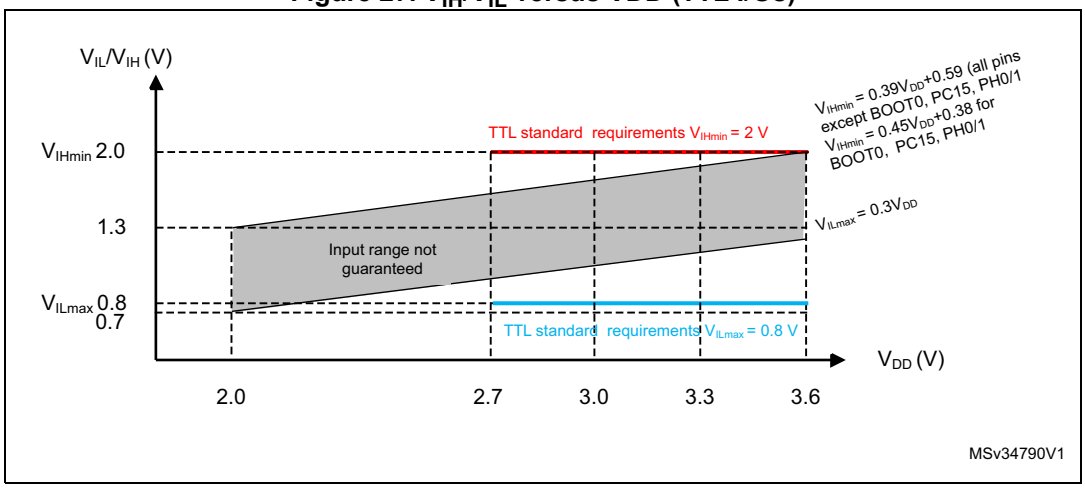



Figure 27. $V_{IH}/V_{IL}$ versus VDD (TTL I/Os)




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±15 mA with the non-standard $V_{OL}/V_{OH}$ specifications given in *Table 59*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 23*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 23*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 25*. All I/Os are CMOS and TTL compliant.

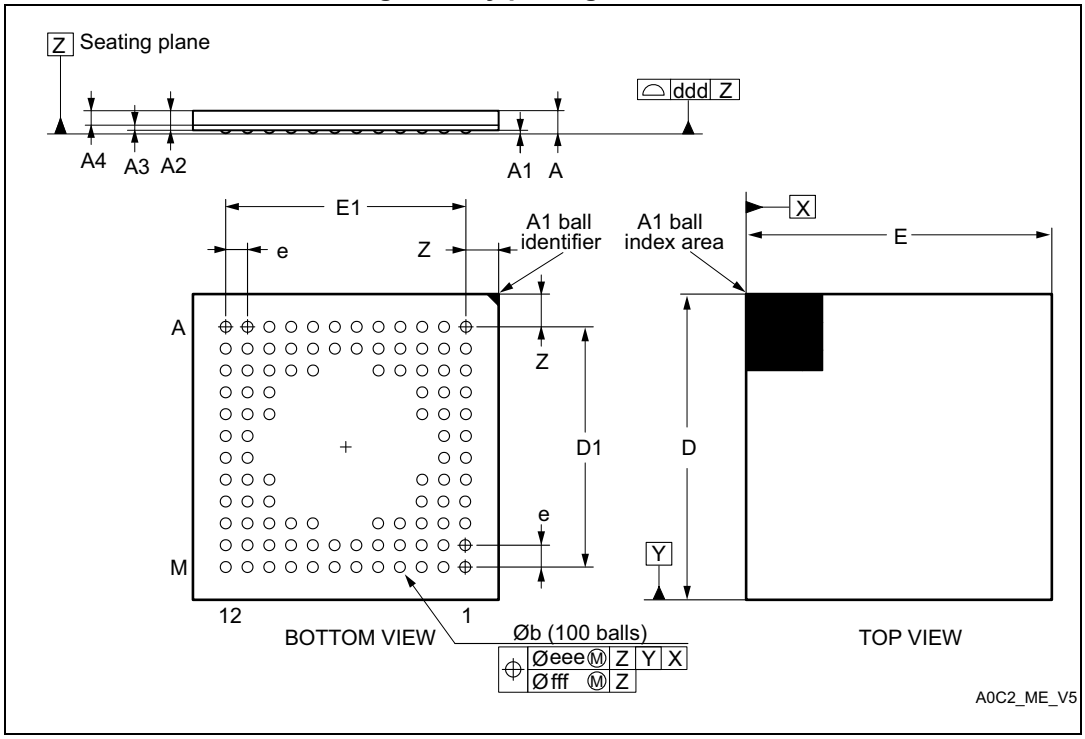
**Table 59. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | CMOS port(2), $I_{IO}$ = +8 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin | | $V_{DD}$-0.4 | - | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | TTL port(2), $I_{IO}$ =+ 8 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | |
| $V_{OH}$ (3)(4) | Output high level voltage for an I/O pin | TTL port(2), $I_{IO}$ = -6 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 2.4 | - | |
| $V_{OL}$ (1)(4) | Output low level voltage for an I/O pin | $I_{IO}$ = +15 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 1.3 | |
| $V_{OH}$ (3)(4) | Output high level voltage for an I/O pin | $I_{IO}$ = -15 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-1.3 | - | |
| $V_{OL}$ (1)(4) | Output low level voltage for an I/O pin | $I_{IO}$ = +4 mA 1.65 V ≤ $V_{DD}$ < 3.6 V | - | 0.45 | |
| $V_{OH}$ (3)(4) | Output high level voltage for an I/O pin | $I_{IO}$ = -4 mA 1.65 V ≤ $V_{DD}$ ≤ 3.6 V | $V_{DD}$-0.45 | - | |
| $V_{OLFM+}$ (1)(4) | Output low level voltage for an FTf I/O pin in Fm+ mode | $I_{IO}$ = 20 mA 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | |
| | | $I_{IO}$ = 10 mA 1.65 V ≤ $V_{DD}$ ≤ 3.6 V | - | 0.4 | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 23*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 23*. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

## 7.2 UFBGA100 package information

**Figure 42. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 77. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data**

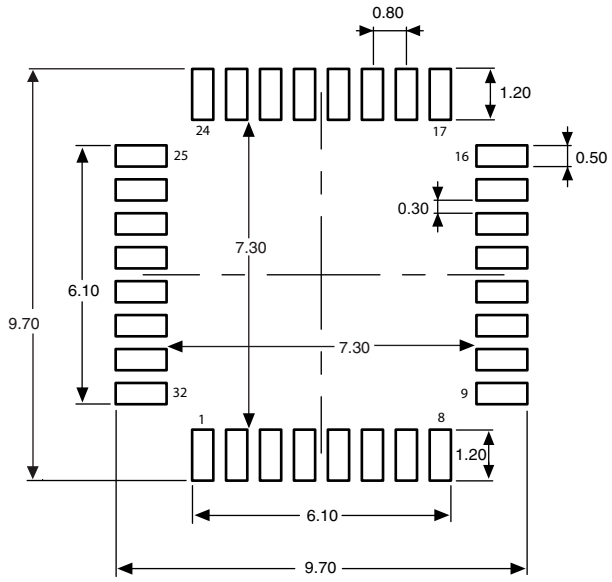
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 0.600 | - | - | 0.0236 |
| A1 | - | - | 0.110 | - | - | 0.0043 |
| A2 | - | 0.450 | - | - | 0.0177 | - |
| A3 | - | 0.130 | - | - | 0.0051 | 0.0094 |
| A4 | - | 0.320 | - | - | 0.0126 | - |
| b | 0.240 | 0.290 | 0.340 | 0.0094 | 0.0114 | 0.0134 |
| D | 6.850 | 7.000 | 7.150 | 0.2697 | 0.2756 | 0.2815 |
| D1 | - | 5.500 | - | - | 0.2165 | - |
| E | 6.850 | 7.000 | 7.150 | 0.2697 | 0.2756 | 0.2815 |
| E1 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| Z | - | 0.750 | - | - | 0.0295 | - |

**Table 85. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.600 | - | - | 0.2205 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.600 | - | - | 0.2205 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 57. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint**




1. Dimensions are expressed in millimeters.

**Table 89. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 22-Mar-2016 | 3 | Updated number of SPIs on cover page and in *Table 2: Ultra-low-power STM32L071xx device features and peripheral counts*.<br>Changed minimum comparator supply voltage to 1.65 V on cover page.<br>Added number of fast and standard channels in *Section 3.11: Analog-to-digital converter (ADC)*.<br>Updated *Section 3.15.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.15.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces.<br>Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.15.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.15.3: Low-power universal asynchronous receiver transmitter (LPUART)*.<br>Changed $V_{DDA}$ minimum value to 1.65 V in *Table 25: General operating conditions*.<br>*Section 6.3.15: 12-bit ADC characteristics*:<br>– *Table 62: ADC characteristics*:<br>Distinction made between $V_{DDA}$ for fast and standard channels; added note *1.*<br>Added note *4.* related to $R_{ADC}$.<br>Updated $f_{TRIG}$, and $V_{AIN}$ maximum value.<br>Updated $t_S$ and $t_{CONV}$.<br>Added $V_{REF+}$.<br>– Updated equation 1 description.<br>– Updated *Table 63: RAIN max for fADC = 16 MHz* for $f_{ADC}$ = 16 MHz and distinction made between fast and standard channels.<br>Added *Table 71: USART/LPUART characteristics*. |