



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l071rzh6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- 32.768 kHz low-speed external crystal (LSE)
- 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

• RTC clock source

The LSI, LSE or HSE sources can be chosen to clock the RTC, whatever the system clock.

• Startup clock

After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

• Clock security system (CSS)

This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled. Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

• Clock-out capability (MCO: microcontroller clock output)

It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.



To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V _{DDA} = 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C V _{DDA} = 3 V	0x1FF8 007E - 0x1FF8 007F

 Table 7. Temperature sensor calibration values

3.12.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+} , is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V _{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 8. Internal voltage reference measured values

3.13 Ultra-low-power comparators and reference voltage

The STM32L071xx embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
 - External I/O pins
 - Internal reference voltage (V_{REFINT})
 - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 μ A typical).



3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The four USART interfaces (USART1, USART2, USART4 and USART5) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

Table 12 for the supported modes and features of USART interfaces.

USART modes/features ⁽¹⁾	USART1 and USART2	USART4 and USART5
Hardware flow control for modem	Х	Х
Continuous communication using DMA	Х	Х
Multiprocessor communication	Х	Х
Synchronous mode ⁽²⁾	Х	Х
Smartcard mode	Х	-
Single-wire half-duplex communication	Х	Х
IrDA SIR ENDEC block	Х	-
LIN mode	Х	-
Dual clock domain and wakeup from Stop mode	Х	-
Receiver timeout interrupt	Х	-
Modbus communication	Х	-
Auto baud rate detection (4 modes)	Х	-
Driver Enable	Х	Х

Table 12. USART implementation

1. X = supported.

2. This mode allows using the USART as an SPI master.

3.15.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame



	1	2	3	4	5	6	7	8
А	₽ĊĨ 4 OSC32 `_₩	(PC13)	(PB9)	(PB4)	(PB3)	(PA15)	(PA14)	(PA13)
В	PC75- OSC32 _QUT		(PB8)		(PD2)	(PC11)	(PC10)	(PA12)
С	VPHO-1 OSC_IN	(vss)	(PB7)	(PB5)	(PC12)	(PA10)	(PA9)	(PA11)
D	(OSC) \OSC) \QUT		(PB6)	(vss)	(vss)	(vss)	(PA8)	(PC9)
E	(NRST)	(PC1)	(PC0)				(PC7)	(PC8)
F	(VSSA)	(PC2)	(PA2)	(PA5)	(PB0)	(PC6)	(PB15)	(PB14)
G	(VREF)	(PA0)	(PA3)	(PA6)	(PB1)	(PB2)	(PB10)	(PB13)
н	(VDDA)	(PA1)	(PA4)	(PA7)	(PC4)	(PC5)	(PB11)	(PB12)
	L							

Figure 6. STM32L071xx TFBGA64 ballout - 5x 5 mm

1. The above figure shows the package top view.

2. I/O supplied by VDDIO2.





Figure 7. STM32L071xx WLCSP49 ballout

1. The above figure shows the package top view.

2. I/O supplied by VDDIO2.



50/					Table 20.	Alternate fur	ctions port E			
136			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	F	Port	SPI1/SPI2/I2S2/ USART1/2/ LPUART1/LPTI M1/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1 /TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
		PE0	-		EVENTOUT	-	-	-	-	-
		PE1	-		EVENTOUT	-	-	-	-	-
		PE2	-		TIM3_ETR	-	-	-	-	-
		PE3	TIM22_CH1		TIM3_CH1	-	-	-	-	-
_		PE4	TIM22_CH2	-	TIM3_CH2	-	-	-	-	-
Doc		PE5	TIM21_CH1	-	TIM3_CH3	-	-	-	-	-
Doz		PE6	TIM21_CH2	-	TIM3_CH4	-	-	-	-	-
27101 Re	oort E	PE7	-		-	-	-	-	USART5_CK/U SART5_RTS_D E	-
< ω		PE8	-		-	-	-	-	USART4_TX	-
		PE9	TIM2_CH1		TIM2_ETR	-	-	-	USART4_RX	-
		PE10	TIM2_CH2		-	-	-	-	USART5_TX	-
		PE11	TIM2_CH3	-	-	-	-	-	USART5_RX	-
		PE12	TIM2_CH4	-	SPI1_NSS	-	-	-	-	-
		PE13	-		SPI1_SCK	-	-	-	-	-
		PE14	-		SPI1_MISO	-	-	-	-	-
		PE15	-		SPI1_MOSI	-	-	-	-	-

STM32L071xx

5

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25$ °C and $T_A = T_Amax$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V \leq V_{DD} \leq 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.





Power supply scheme 6.1.6



Figure 14. Power supply scheme

6.1.7 **Current consumption measurement**



Figure 15. Current consumption measurement scheme



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{LPBUF} ⁽⁴⁾	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V _{REFINT_DIV1} ⁽⁴⁾	1/4 reference voltage	-	24	25	26	
V _{REFINT_DIV2} ⁽⁴⁾	1/2 reference voltage	-	49	50	51	% Vrefinit
V _{REFINT_DIV3} ⁽⁴⁾	3/4 reference voltage	-	74	75	76	

Table 28. Embedded internal reference voltage⁽¹⁾ (continued)

1. Refer to *Table 40: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).

2. Guaranteed by test in production.

3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

4. Guaranteed by design.

5. Shortest sampling time can be determined in the application by multiple iterations.

6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 15: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 42: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 49*, *Table 25* and *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.



Symbol	Parameter	Conditions	Тур	Max ⁽¹⁾	Unit
		$T_A = -40$ to 25°C	0,43	1,00	
		T _A = 55°C	0,735	2,50	
I _{DD} (Stop)	Supply current in Stop mode	T _A = 85°C	2,25	4,90	μA
		T _A = 105°C	5,3	13,00	
		T _A = 125°C	12,5	28,00	

Table 36. Typical and maximum current consumptions in Stop mode

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.







Symbol	parameter	System frequency	Current consumption during wakeup	Unit
		HSI	1	
		HSI/4	0,7	
I _{DD} (Wakeup from Stop)	akeup from Supply current during Wakeup from	MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	mA
I _{DD} (Reset)	Reset pin pulled down	-	0,21	
I _{DD} (Power-up)	BOR on	-	0,23	
I _{DD} (Wakeup from	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
StandBy)	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Table 38. Average current consumption during Wakeup



Symbol	Parameter	Conditions	Тур	Мах	Unit
		f _{HCLK} = f _{MSI} = 4.2 MHz	5.0	8	
	Wakeup from Stop mode, regulator in Run mode	f _{HCLK} = f _{HSI} = 16 MHz	4.9	7	
		f _{HCLK} = f _{HSI} /4 = 4 MHz	8.0	11	
		f _{HCLK} = f _{MSI} = 4.2 MHz Voltage range 1	5.0	8	
		f _{HCLK} = f _{MSI} = 4.2 MHz Voltage range 2	5.0	8	
	t _{WUSTOP} Wakeup from Stop mode, regulator in low-	f _{HCLK} = f _{MSI} = 4.2 MHz Voltage range 3	5.0	8	
		f _{HCLK} = f _{MSI} = 2.1 MHz	7.3	13	
t _{WUSTOP}		f _{HCLK} = f _{MSI} = 1.05 MHz	13	23	
	r	f _{HCLK} = f _{MSI} = 524 kHz	28	38	μs
		f _{HCLK} = f _{MSI} = 262 kHz	51	65	
		f _{HCLK} = f _{MSI} = 131 kHz	100	120	
		f _{HCLK} = MSI = 65 kHz	190	260	
		f _{HCLK} = f _{HSI} = 16 MHz	4.9	7	
		f _{HCLK} = f _{HSI} /4 = 4 MHz	8.0	11	
		f _{HCLK} = f _{HSI} = 16 MHz	4.9	7	
	power mode, code running from RAM	f _{HCLK} = f _{HSI} /4 = 4 MHz	7.9	10	
		f _{HCLK} = f _{MSI} = 4.2 MHz	4.7	8	
twillotopy	Wakeup from Standby mode FWU bit = 1	f _{HCLK} = MSI = 2.1 MHz	65	130	
WUSIDBY	Wakeup from Standby mode FWU bit = 0	f _{HCLK} = MSI = 2.1 MHz	2.2	3	ms

Table 41. Low-power mode wakeup timings (continued)



6.3.7 Internal clock source characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

High-speed internal 16 MHz (HSI16) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI16}	Frequency	V _{DD} = 3.0 V	-	16	-	MHz
(1)(2)	HSI16 user-	Trimming code is not a multiple of 16	-	±0.4	0.7	%
TRIM	trimmed resolution	Trimming code is a multiple of 16	-	-	± 1.5	%
		V _{DDA} = 3.0 V, T _A = 25 °C	-1 ⁽³⁾	-	1 ⁽³⁾	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
ACC .	Accuracy of the	V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
(2)	factory-calibrated	V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V _{DDA} = 1.65 V to 3.6 V T _A = − 40 to 125 °C	-5.45	-	3.25	%
t _{SU(HSI16)} ⁽²⁾	HSI16 oscillator startup time	-	-	3.7	6	μs
I _{DD(HSI16)} ⁽²⁾	HSI16 oscillator power consumption	-	-	100	140	μA

Table 46. 16 MHz HSI16 oscillator char
--

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Guaranteed by test in production.



Figure 25. HSI16 minimum and maximum value versus temperature



6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5 \mu A/+0 \mu A$ range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the Table 57.

		Functional s		
Symbol	Description	Negative injection	Positive injection	Unit
I _{INJ}	Injected current on BOOT0	-0	NA	
	Injected current on PA0, PA4, PA5, PC15, PH0 and PH1	-5	0	mA
	Injected current on any other FT, FTf pins	-5 ⁽¹⁾	NA	
	Injected current on any other pins	-5 ⁽¹⁾	+5	

Table 57. I/O current injection susceptibility

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.



6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the conditions summarized in *Table 25*. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
VII	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	0.3V _{DD}	
		BOOT0 pin	-	-	0.14V _{DD} ⁽¹⁾	
V _{IH}	Input high level voltage	All I/Os	0.7 V _{DD}	-	-	V
V.	I/O Schmitt trigger voltage hysteresis	Standard I/Os	-	10% V _{DD} ⁽³⁾	-	
V hys	(2)	BOOT0 pin	-	0.01	-	
		$\label{eq:VSS} \begin{array}{l} V_{SS} \leq V_{IN} \leq V_{DD} \\ \mbox{All I/Os except for} \\ \mbox{PA11, PA12, BOOT0} \\ \mbox{and FTf I/Os} \end{array}$	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$, PA11 and PA12 I/Os	-	-	-50/+250	nA
		V _{SS} ≤V _{IN} ≤V _{DD} FTf I/Os	-	-	±100	
l _{ikg}	Input leakage current ⁽⁴⁾	$\label{eq:VDD} \begin{array}{c} V_{DD} \leq V_{IN} \leq 5 \ V \\ \mbox{All I/Os except for} \\ \mbox{PA11, PA12, BOOT0} \\ \mbox{and FTf I/Os} \end{array}$	-	-	200	nA
		V _{DD} ≤ V _{IN} ≤ 5 V FTf I/Os	-	-	500	
		$V_{DD} \le V_{IN} \le 5 V$ PA11, PA12 and BOOT0	-	-	10	μA
R _{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	30	45	60	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	30	45	60	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

Table 58.	I/O	static	characteristics

1. Guaranteed by characterization.

2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

3. With a minimum of 200 mV. Guaranteed by characterization results.

4. The max. value may be exceeded if negative current is injected on adjacent pins.

 Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).



Cumhal	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Мах	Min	Тур	Max
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
с	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
CCC	-	-	0.080	-	-	0.0031

Table 76. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat packagemechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



Table 80. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Мах	Min	Тур	Мах
е	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball ,grid array recommended footprint



Table 81. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note:Non solder mask defined (NSMD) pads are recommended.4 to 6 mils solder paste screen printing process.



7.6 LQFP48 package information

Figure 53. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.



Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
е	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
CCC	-	-	0.080	-	-	0.0031

Table 84. LQFP48 - 4	8-pin. 7 x 7	mm low-profile o	puad flat packad	pe mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.

