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### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f47k40-i-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	_
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	iown	-n/n = Value a	at POR and BO	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	EXTOEN: Ex	ternal Oscillato	r Manual Requ	iest Enable bit			
	1 = EXTOS	C is explicitly e	nabled, operat	ing as specifie	d by FEXTOSC	;	
	0 = EXIOS	C could be ena	bled by reques	sting periphera			
bit 6	HFOEN: HFI	NTOSC Oscilla	tor Manual Re	quest Enable b	pit		
	1 = HFINIC	SC is explicitly	enabled, oper	ating as specif		Q (Register 4-	5)
6.4 F					idi Ianual Daguag	t Enchla hit i	Derived from
DIL D	HEINTOSC)	1030 (500	КП2/31.23 КП2	c) Oscillator iv	ianuai Reques		
	1 = MFINTC	DSC is explicitly	enabled				
	0 = MFINTC	SC could be e	nabled by requ	lesting periphe	eral		
bit 4	LFOEN: LFIN	ITOSC (31 kHz	) Oscillator Ma	anual Request	Enable bit		
	1 = LFINTO	SC is explicitly	enabled				
	0 = LFINTO	SC could be er	nabled by requ	esting peripher	ral		
bit 3 SOSCEN: Secondary Oscillator Manual Request Enable bit							
	1 = Seconda	ary Oscillator is	explicitly enabled	oled, operating	as specified by	y SOSCPWR	
	0 = Seconda	ary Oscillator c	ould be enable	d by requestin	g peripheral		
bit 2	ADOEN: ADO	C Oscillator Ma	nual Request I	Enable bit			
	1 = ADC os	cillator is explic	atly enabled	aucotina norin	horal		
h# 4 0				equesting penp			
dit 1-0	Unimplemen	tea: Read as '	0.				

# REGISTER 4-7: OSCEN: OSCILLATOR MANUAL ENABLE REGISTER

# 4.3 Clock Source Types

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

A 4x PLL is provided that can be used in conjunction with the external clock. When used with the HFINTOSC the 4x PLL has input frequency limitations.See **Section 4.3.1.4 "4x PLL"** for more details.

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce 1, 2, 4, 8, 12, 16, 32, 48 and 64 MHz clock. The frequency can be controlled through the OSCFRQ register (Register 4-5). The Low-Frequency Internal Oscillator (LFINTOSC) generates a fixed 31 kHz frequency.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 4.4 "Clock Switching"** for additional information. The system clock can be made available on the OSC2/CLKOUT pin for any of the modes that do not use the OSC2 pin. The clock out functionality is governed by the CLKOUTEN bit in the CONFIG1H register (Register 3-2). If enabled, the clock out signal is always at a frequency of Fosc/4.

# 4.3.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> and FEXTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> and NDIV<3:0> bits in the OSCCON1 register to switch the system clock source.

See **Section 4.4 "Clock Switching"** for more information.

# 4.3.1.1 EC Mode

The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 4-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH High power, above 8 MHz
- ECM Medium power, 100 kHz-8 MHz
- ECL Low power, below 100 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC<sup>®</sup> MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

#### FIGURE 4-2: EXTERNAL CLOCK (EC) MODE OPERATION



# 4.3.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

**LP** Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification (above 100 kHz - 8 MHz).

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting (above 8 MHz).

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

# 11.1.2 CONTROL REGISTERS

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the following registers:

- NVMCON1 register
- NVMCON2 register
- TABLAT register
- TBLPTR registers

### 11.1.2.1 NVMCON1 and NVMCON2 Registers

The NVMCON1 register (Register 11-1) is the control register for memory accesses. The NVMCON2 register is not a physical register; it is used exclusively in the memory write and erase sequences. Reading NVMCON2 will read all '0's.

The NVMREG<1:0> control bits determine if the access will be to Data EEPROM Memory locations. PFM locations or User IDs, Configuration bits, Rev ID and Device ID. When NVMREG<1:0> = 00, any subsequent operations will operate on the Data EEPROM Memory. When NVMREG<1:0> = 10, any subsequent operations will operate on the program memory. When NVMREG<1:0> = x1, any subsequent operations will operate on the Data IDS, Rev ID and Device ID.

The FREE bit allows the program memory erase operation. When the FREE bit is set, an erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled. This bit is applicable only to the PFM and not to data EEPROM.

When set, the WREN bit will allow a program/erase operation. The WREN bit is cleared on power-up.

The WRERR bit is set by hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is successfully complete.

The WR control bit initiates erase/write cycle operation when the NVMREG<1:0> bits point to the Data EEPROM Memory location, and it initiates a write operation when the NVMREG<1:0> bits point to the PFM location. The WR bit cannot be cleared by firmware; it can only be set by firmware. Then the WR bit is cleared by hardware at the completion of the write operation.

The NVMIF Interrupt Flag bit of the PIR7 register is set when the write is complete. The NVMIF flag stays set until cleared by firmware.

### 11.1.2.2 TABLAT – Table Latch Register

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch register is used to hold 8-bit data during data transfers between program memory and data RAM.

# 11.1.2.3 TBLPTR – Table Pointer Register

The Table Pointer (TBLPTR) register addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low-order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22<sup>nd</sup> bit allows access to the Device ID, the User ID and the Configuration bits.

The Table Pointer register, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations on the TBLPTR affect only the low-order 21 bits.

### 11.1.2.4 Table Pointer Boundaries

TBLPTR is used in reads, writes and erases of the Program Flash Memory.

When a TBLRD is executed, all 22 bits of the TBLPTR determine which byte is read from program memory directly into the TABLAT register.

When a TBLWT is executed the byte in the TABLAT register is written, not to Flash memory but, to a holding register in preparation for a program memory write. The holding registers constitute a write block which varies depending on the device (see Table 11-3). The 3, 4, or 5 LSbs of the TBLPTRL register determine which specific address within the holding register block is written to. The MSBs of the Table Pointer have no effect during TBLWT operations.

When a program memory write is executed the entire holding register block is written to the Flash memory at the address determined by the MSbs of the TBLPTR. The 3, 4, or 5 LSBs are ignored during Flash memory writes. For more detail, see **Section 11.1.6 "Writing to Program Flash Memory"**.

Figure 11-3 describes the relevant boundaries of TBLPTR based on Program Flash Memory operations.

# 18.1 Timer0 Operation

Timer0 can operate as either an 8-bit timer/counter or a 16-bit timer/counter. The mode is selected with the T016BIT bit of the T0CON register.

### 18.1.1 16-BIT MODE

The register pair TMR0H:TMR0L, increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

# 18.1.1.1 Timer0 Reads and Writes in 16-Bit Mode

In 16-bit mode, to avoid rollover between reading high and low registers, the TMR0H register is a buffered copy of the actual high byte of Timer0, which is neither directly readable nor writable (see Figure 18-1). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte was valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

# 18.1.2 8-BIT MODE

In normal operation, TMR0 increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS<3:0> in the T0CON1 register).

In 8-bit mode, the value of TMR0L is compared to that of the Period buffer, a copy of TMR0H, on each clock cycle. When the two values match, the following events happen:

- TMR0\_out goes high for one prescaled clock period
- TMR0L is reset
- The contents of TMR0H are copied to the period buffer

In 8-bit mode, the TMR0L and TMR0H registers are both directly readable and writable. The TMR0L register is cleared on any device Reset, while the TMR0H register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset Power-on Reset (POR), MCLR Reset, Watchdog Timer Reset (WDTR) or
- Brown-out Reset (BOR)

# 18.1.3 COUNTER MODE

In Counter mode, the prescaler is normally disabled by setting the T0CKPS bits of the T0CON1 register to '0000'. Each rising edge of the clock input (or the output of the prescaler if the prescaler is used) increments the counter by '1'.

# 18.1.4 TIMER MODE

In Timer mode, the Timer0 module will increment every instruction cycle as long as there is a valid clock signal and the T0CKPS bits of the T0CON1 register (Register 18-2) are set to '0000'. When a prescaler is added, the timer will increment at the rate based on the prescaler value.

# 18.1.5 ASYNCHRONOUS MODE

When the TOASYNC bit of the TOCON1 register is set (TOASYNC = '1'), the counter increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows the counter to continue operation during Sleep mode provided that the clock also continues to operate during Sleep.

### 18.1.6 SYNCHRONOUS MODE

When the T0ASYNC bit of the T0CON1 register is clear (T0ASYNC = 0), the counter clock is synchronized to the system clock (Fosc/4). When operating in Synchronous mode, the counter clock frequency cannot exceed Fosc/4.

# 18.2 Clock Source Selection

The T0CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 18-2 displays the clock source selections.

# 18.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

### 18.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.

# **REGISTER 19-4: TMRxGATE: TIMERx GATE ISM REGISTER**

U-0	U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
_	—	—	_		GSS	<3:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as	s 'O'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	u = unchanged

#### bit 7-4 Unimplemented: Read as '0'

bit 3-0 **GSS<3:0>:** Timerx Gate Source Selection bits

688	Timer1	Timer3	Timer5
033	Gate Source	Gate Source	Gate Source
1111	Reserved	Reserved	Reserved
1110	ZCDOUT	ZCDOUT	ZCDOUT
1101	CMP2OUT	CMP2OUT	CMP2OUT
1100	CMP1OUT	CMP1OUT	CMP1OUT
1011	PWM4OUT	PWM4OUT	PWM4OUT
1010	PWM3OUT	PWM3OUT	PWM3OUT
1001	CCP2OUT	CCP2OUT	CCP2OUT
1000	CCP1OUT	CCP10UT	CCP1OUT
0111	TMR6OUT (post-scaled)	TMR6OUT (post-scaled)	TMR6OUT (post-scaled)
0110	TMR5 overflow	TMR5 overflow	Reserved
0101	TMR4OUT (post-scaled)	TMR4OUT (post-scaled)	TMR4OUT (post-scaled)
0100	TMR3 overflow	Reserved	TMR3 overflow
0011	TMR2OUT (post-scaled)	TMR2OUT (post-scaled)	TMR2OUT (post-scaled)
0010	Reserved	TMR1 overflow	TMR1 overflow
0001	TMR0 overflow	TMR0 overflow	TMR0 overflow
0000	Pin selected by T1GPPS	Pin selected by T3GPPS	Pin selected by T5GPPS

# PIC18(L)F27/47K40

FIGURE 19-5:	TIMER1/3/5 GATE TOGGLE MODE
TMRxGE	
TxGPOL	
TxGTM	
TxTxG_IN	
ТхСКІ	
TxGVAL	
TIMER1/3/5	$N \qquad \qquad$

# FIGURE 19-6: TIMER1/3/5 GATE SINGLE-PULSE MODE



# 25.1 Register Definitions: Modulation Control

Long bit name prefixes for the Modulation peripheral is shown in Table 25-1. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

# TABLE 25-1:

Peripheral	Bit Name Prefix
MD	MD

# REGISTER 25-1: MDCON0: MODULATION CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
EN	—	OUT	OPOL	—	—	—	BIT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	EN: Modulator Module Enable bit
	<ul> <li>1 = Modulator module is enabled and mixing input signals</li> <li>0 = Modulator module is disabled and has no output</li> </ul>
bit 6	Unimplemented: Read as '0'
bit 5	OUT: Modulator Output bit
	Displays the current output value of the Modulator module. <sup>(1)</sup>
bit 4	OPOL: Modulator Output Polarity Select bit
	<ul> <li>1 = Modulator output signal is inverted; idle high output</li> <li>0 = Modulator output signal is not inverted; idle low output</li> </ul>
bit 3-1	Unimplemented: Read as '0'
bit 0	BIT: Allows software to manually set modulation source input to module <sup>(2)</sup>
Note 1:	The modulated output frequency can be greater and asynchronous from the clock that updates this register bit, the bit value may not be valid for higher speed modulator or carrier signals.
2:	MDBIT must be selected as the modulation source in the MDSRC register for this operation.

# 25.6 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCON1 register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCON1 register.

# 25.7 Programmable Modulator Data

The MDBIT of the MDCON0 register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

# 25.8 Modulated Output Polarity

The modulated output signal provided on the DSM pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON0 register.

# 25.9 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep. Refer to **Section 6.0 "Power-Saving Operation Modes"** for more details.

# 25.10 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

# 25.11 Peripheral Module Disable

The DSM module can be completely disabled using the PMD module to achieve maximum power saving. The DSMMD bit of PMD5 (Register 7-6) when set disables the DSM module completely. When enabled again all the registers of the DSM module default to POR status.

The transition of a data bit is always performed while the SCL line is held low. Transitions that occur while the SCL line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, then it repeatedly sends out a byte of data, with the slave responding after each byte with an  $\overline{ACK}$  bit. In this example, the master device is in Master Transmit mode and the slave is in Slave Receive mode.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an  $\overrightarrow{ACK}$  bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last ACK bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last ACK bit when it is in receive mode.

The I<sup>2</sup>C bus specifies three message protocols;

- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.
- Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.

When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

# 26.6.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

## 26.10.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 26-33).
- b) SCL is sampled low before SDA is asserted low (Figure 26-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- · the Start condition is aborted,
- the BCLxIF flag is set and
- the MSSP module is reset to its Idle state (Figure 26-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 26-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.





# 27.2 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 27-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

### 27.2.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 27-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXxREG register.

### 27.2.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXxSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXxSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCxSTA register enables the EUSART and automatically configures the TXx/CKx I/O pin as an output. If the TXx/CKx pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

**Note:** The TXxIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

# 27.2.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXxREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXxREG until the Stop bit of the previous character has been transmitted. The pending character in the TXxREG is then transferred to the TSR in one Tcy immediately following the Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXxREG.

### 27.2.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDxCON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 27.5.1.2 "Clock Polarity**".

# 27.2.1.4 Transmit Interrupt Flag

The TXxIF interrupt flag bit of the PIR3 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXxREG. In other words, the TXxIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXxREG. The TXxIF flag bit is not cleared immediately upon writing TXxREG. TXxIF becomes valid in the second instruction cycle following the write execution. Polling TXxIF immediately following the TXxREG write will return invalid results. The TXxIF bit is read-only, it cannot be set or cleared by software.

The TXxIF interrupt can be enabled by setting the TXxIE interrupt enable bit of the PIE3 register. However, the TXxIF flag bit will be set whenever the TXxREG is empty, regardless of the state of TXxIE enable bit.

To use interrupts when transmitting data, set the TXxIE bit only when there is more data to send. Clear the TXxIE interrupt enable bit upon writing the last character of the transmission to the TXxREG.

# 29.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200  $\mu$ s after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200  $\mu$ s between consecutive conversions of the temperature indicator output.

### TABLE 29-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVI	R<1:0>	ADFV	R<1:0>	423

Legend: — = Unimplemented location, read as '0'. Shaded cells are unused by the temperature indicator module.

# 31.2 ADC Operation

# 31.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. A conversion may be started by any of the following:

- Software setting the ADGO bit of ADCON0 to '1'
- An external trigger (selected by Register 31-3)
- A continuous-mode retrigger (see section Section 31.5.8 "Continuous Sampling mode")

Note: The ADGO bit should not be set in the same instruction that turns on the ADC. Refer to Section 31.2.6 "ADC Conversion Procedure (Basic Mode)".

# 31.2.2 COMPLETION OF A CONVERSION

When any individual conversion is complete, the value already in ADRES is written into ADPREV (if ADPSIS = 1) and the new conversion results appear in ADRES. When the conversion completes, the ADC module will:

- Clear the ADGO bit (unless the ADCONT bit of ADCON0 is set)
- · Set the ADIF Interrupt Flag bit
- Set the ADMATH bit
- Update ADACC

When ADDSEN = 0 then after every conversion, or when ADDSEN = 1 then after every other conversion, the following events occur:

- ADERR is calculated
- ADTIF is set if ADERR calculation meets threshold comparison

Importantly, filter and threshold computations occur after the conversion itself is complete. As such, interrupt handlers responding to ADIF should check ADTIF before reading filter and threshold results.

# 31.2.3 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

# 31.2.4 EXTERNAL TRIGGER DURING SLEEP

If the external trigger is received during sleep while ADC clock source is set to the FRC, ADC module will perform the conversion and set the ADIF bit upon completion.

If an external trigger is received when the ADC clock source is something other than FRC, the trigger will be recorded, but the conversion will not begin until the device exits Sleep.

# 31.2.5 AUTO-CONVERSION TRIGGER

The Auto-conversion Trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the ADGO bit is set by hardware.

The Auto-conversion Trigger source is selected with the ADACT<4:0> bits of the ADACT register.

Using the Auto-conversion Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met. See Table 31-2 for auto-conversion sources.

# TABLE 31-2: ADC AUTO-CONVERSION TABLE

Source Peripheral	Description
ADCACTPPS	Pin selected by ADCACTPPS
TMR0	Timer0 overflow condition
TMR1/3/5	Timer1/3/5 overflow condition
TMR2/4/6	Match between Timer2/4/6 postscaled value and PR2/4/6
CCP1/2	CCP1/2 output
PWM3/4	PWM3/4 output
C1/2	Comparator C1/2 output
IOC	Interrupt-on-change interrupt trigger
ADERR	Read of ADERRH register
ADRESH	Read of ADRESH register
ADPCH	Write of ADPCH register

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
— — ADPCH<5:0>									
bit 7							bit 0		
Legend:									
R = Readable b	it	W = Writable bit		U = Unimpleme	ented bit, read as	; 'O'			
u = Bit is unchar	nged	x = Bit is unknown		-n/n = Value at	POR and BOR/\	/alue at all other	Resets		
'1' = Bit is set		'0' = Bit is cleared							
bit 7-6	Unimplemen	ted: Read as '0'							
bit 5-0	ADPCH<5:0>	·: ADC Positive Input C	hannel Sel	ection bits					
	111111 =	Fixed Voltage Referer	nce (FVR) <sup>(2</sup>	.) 01011	1 = ANC7				
	111110 =	DAC1 output <sup>(1)</sup>		01011	0 = ANC6				
	111101 =	Temperature Indicator	-(3)	01010	1 = ANC5				
	111100 =	AVss (Analog Ground	)	01010	0 = ANC4				
	111011 =	Reserved. No channe	l connected	<b>d.</b> 01001	010011 <b>= ANC3</b>				
	•			01001	0 = ANC2				
	•			01000	1 = ANC1				
	•	(0)		01000	0 = ANC0				
	100010 =	ANE2 <sup>(4)</sup>		00111	1 = ANB7				
	100001 =	ANE1 <sup>(4)</sup>		00111	0 = ANB6				
	100000 =	ANE0 <sup>(4)</sup>		00110	1 = ANB5				
	011111 =	AND7 <sup>(4)</sup>		00110	0 = ANB4				
	011110 =	AND6 <sup>(4)</sup>		00101	1 = ANB3				
	011101 =	AND5(4)		00101	0 = ANB2				
	011100 =	AND4 <sup>(4)</sup>		00100	1 = ANB1				
	011011 =	AND3 <sup>(4)</sup>		00100	0 = ANB0				
	011010 =	AND2 <sup>(4)</sup>		00011	1 = ANA7				
	011001 =	AND1 <sup>(4)</sup>		00011	0 <b>= ANA6</b>				
	011000 =	AND0(4)		00010	1 = ANA5				
				00010	0 = ANA4				
				00001	1 = ANA3				
				00001	0 = ANA2				
				00000	1 = ANA1				
				00000	0 <b>= ANA0</b>				

# REGISTER 31-8: ADPCH: ADC POSITIVE CHANNEL SELECTION REGISTER

Note 1: See Section 30.0 "5-Bit Digital-to-Analog Converter (DAC) Module" for more information.

2: See Section 28.0 "Fixed Voltage Reference (FVR)" for more information.

3: See Section 29.0 "Temperature Indicator Module" for more information.

4: PIC18F47K40 only.

# PIC18(L)F27/47K40

CPFSGT Compare f with W, skip if f								
Synta	ax:	CPFSGT	f {,a}					
Oper	ands:	0 ≤ f ≤ 255 a ∈ [0,1]						
Oper	ation:	(f) – (W), skip if (f) > (unsigned c	(W) comparison)					
Statu	is Affected:	None						
Enco	oding:	0110	010a fff	f ffff				
Description:       0110       0100       1111       111         Description:       Compares the contents of data memory location 'f' to the contents of the W b performing an unsigned subtraction. If the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction. If 'a' is '0', the Access Bank is selected if 'a' is '0', the BSR is used to select 11 GPR bank.         If 'a' is '0' and the extended instruction set is enabled, this instruction operal in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Set tion 35.2.3 "Byte-Oriented and Bit Oriented Instructions in Indexed Literal Offset Medee" for dotails.								
Word	ls:	1						
Cycle	es:	1(2) <b>Note:</b> 3 cy	1(2) Note: 3 cycles if skip and followed					
		by a	a 2-word instru	ction.				
QC	ycle Activity:							
	Q1	Q2	Q3	Q4				
	Decode	Read	Process	No				
lf sk	in <sup>.</sup>	Tegister T	Dala	operation				
11 01	Q1	02	Q3	04				
	No	No	No	No				
	operation	operation	operation	operation				
lf sk	ip and followed	d by 2-word in	struction:					
	Q1	Q2	Q3	Q4				
	No	No	No	No				
	No	No	No	No				
	operation	operation	operation	operation				
<u>Example</u> :		HERE NGREATER GREATER	HERE CPFSGT REG, 0 NGREATER : GREATER :					
	Before Instruc	tion						
PC		= Ad	dress (HERE	)				
	W	= ?						
	After Instruction	n						
	If REG	> W;						
	PC If REG	= Ad ≤ W;	<pre>= Address (GREATER) ≤ W;</pre>					
	PC	= Ad	UIESS (NGREA	ATER)				

CPF	SLT	Compare	Compare f with W, skip if f < W					
Synta	ax:	CPFSLT	f {,a}					
Oper	ands:	0 ≤ f ≤ 255 a ∈ [0,1]						
Oper	ation:	(f) – (W), skip if (f) < (unsigned o	(W) comparison)					
Statu	s Affected:	None	. ,					
Enco	ding:	0110	000a ff	ff ffff				
Desc	ription:	Compares location 'f' 1 performing If the conte contents of instruction executed ir 2-cycle inst If 'a' is '0', t If 'a' is '1', t GPR bank.	Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the					
Word	ls:	1						
Cycle	es:	1(2) Note: 3 c by	1(2) <b>Note:</b> 3 cycles if skip and followed by a 2-word instruction.					
QC	ycle Activity:							
	Q1	Q2	Q3	Q4				
	Decode	Read	Process	No				
lf sk	ip <sup>.</sup>	register i	Dala	operation				
ii on	Q1	Q2	Q3	Q4				
	No	No	No	No				
	operation	operation	operation	operation				
lf sk	ip and followed	d by 2-word in	struction:	04				
	No	Q2 No	Q3 No	Q4				
	operation	operation	operation	operation				
	No	No	No	No				
	operation	operation	operation	operation				
Example:		HERE NLESS LESS	HERE CPFSLT REG, 1 NLESS : LESS :					
	Before Instruc	tion						
	PC W	= Ac = ?	dress (HERE	:)				
	After Instructio	on .						
	If REG	< W	,					
	PC	= Ac	dress (LESS	:)				
	If REG	≥ W	; idroee (\mmmo	(C)				
		- A						

# PIC18(L)F27/47K40

MUL	_LW	Multiply	Multiply literal with W							
Synta	ax:	MULLW	MULLW k							
Oper	ands:	$0 \le k \le 25$	5							
Oper	ation:	(W) x k $\rightarrow$	PRODH:	PROD	L					
Statu	is Affected:	None								
Enco	oding:	0000	1101	kkkl	k kkkk					
Desc	ription:	An unsign out betwe 8-bit litera placed in pair. PRO W is unch None of th Note that possible in is possible	An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in the PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged. None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.							
Word	ls:	1								
Cycle	es:	1								
QC	ycle Activity:									
	Q1	Q2	Q3		Q4					
	Decode	Read literal 'k'	Proce Data	ess a	Write registers PRODH: PRODL					
<u>Exan</u>	nple: Before Instruc	MULLW	0C4h							
	W	= F	2h							
	PRODH PRODL After Instructio	= ? = ? = ?	211							
	W PRODH PRODL	= E = A = 0	2h Dh 8h							

MULWF		Multiply	Multiply W with f					
Syntax:		MULWF	f {,a}					
Operands	8:	0 ≤ f ≤ 25 a ∈ [0,1]	5					
Operation	n:	(W) x (f) –	→ PRODH	:PRODL				
Status Af	fected:	None						
Encoding	:	0000	001a	ffff	ffff			
Descriptio	on:	An unsign out betwe register fil result is st register pa high byte. unchange None of tt Note that possible in result is p If 'a' is '0', selected. to select t If 'a' is '0' set is ena operates i Addressin $f \le 95$ (5F <b>35.2.3 "By</b> ented Ins Offset Mo	0000001affffffffAn unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged.None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 35.2.3 "Byte-Oriented and Bit-Ori-					
Words:		1						
Cycles:		1						
Q Cycle	Activity:							
	Q1	Q2	Q3		Q4			
D	ecode	Read register 'f'	Proces Data	ss F F	Write egisters PRODH: PRODL			
Example:		MULWF	REG, 1					

Before Instruction

Defore manualion		
W REG PRODH PRODL	= = =	C4h B5h ? ?
After Instruction		
W REG PRODH PRODL	= = =	C4h B5h 8Ah 94h

# **37.4** AC Characteristics





TABLE 37-9:	PLL SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) VDD $\ge 2.5V$							
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
PLL01	FPLLIN	PLL Input Frequency Range	4	_	16	MHz	
PLL02	FPLLOUT	PLL Output Frequency Range	16		64	MHz	Note 1
PLL03	TPLLST	PLL Lock Time from Start-up		200	_	μS	
PLL04	FPLLJIT	PLL Output Frequency Stability (Jitter)	-0.25	_	0.25	%	
*	These p	arameters are characterized but not tested.					

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance t only and are not tested.

**Note 1:** The output frequency of the PLL must meet the Fosc requirements listed in Parameter D002.





# TABLE 37-21: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
US120	TCKH2DTV	SYNC XMIT (Master and Slave)	_	80	ns	$3.0V \leq V\text{DD} \leq 5.5V$
		Clock high to data-out valid	_	100	ns	$1.8V \leq V\text{DD} \leq 5.5V$
US121	TCKRF	Clock out rise time and fall time		45	ns	$3.0V \le V\text{DD} \le 5.5V$
	(Master mode)	_	50	ns	$1.8V \leq V\text{DD} \leq 5.5V$	
US122	TDTRF	Data-out rise time and fall time	_	45	ns	$3.0V \leq V\text{DD} \leq 5.5V$
			_	50	ns	$1.8V \le V\text{DD} \le 5.5V$

# FIGURE 37-15: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



### TABLE 37-22: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions	
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-setup before CK $\downarrow$ (DT hold time)	10		ns		
US126	TCKL2DTL	Data-hold after CK $\downarrow$ (DT hold time)	15		ns		

# **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>[X]</u> <sup>(2)</sup> -	¥	<u>/xx</u>	<u>xxx</u>	Exar	nple	95:
Device	Tape and Reel Option	Temperature Range	Package	Pattern	a) b)	PIC PDII PIC	18F27K40-E/P 301 = Extended temp., P package, QTP pattern #301. 18F47K40-E/SO = Extended temp., SOIC age.
Device:	PIC18F27K40 PIC18F47K40	, PIC18LF27K40, , PIC18LF47K40,			c)	PIC <sup>2</sup> temp	18F47K40T-I/ML = Tape and reel, Industrial 5., QFN package.
Tape and Reel Option:	Blank = standa T = Tape and I	ard packaging (tub Reel <sup>(1), (2)</sup>	e or tray)				
Temperature Range:	E = -40 I = -40	°C to +125°C (I °C to +85°C (I	Extended) Industrial)		Note	1:	Tape and Reel option is available for ML,
Package:	ML = 28- ML = 44-1 P = 40-1 PT = 44-1 SO = 28-1 SP = 28-1 SS = 28-1	ead QFN 6x6mm ead QFN 8x8x0.9r ead UQFN 5x5x0. ead PDIP ead TQFP (Thin Q ead SOIC ead SKinny Plastic ead SSOP	nm 5mm uad Flatpack) . DIP			2:	MV, P1, SO and SS packages with industrial Temperature Range only. Tape and Reel identifier only appears in catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.
Pattern:	QTP, SQTP, C (blank otherwi	ode or Special Re se)	quirements				