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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf27k40-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

REGISTER 3-13:	REVI	SION ID: REVIS	ION ID R	EGISTER			
R	R	R	R	R	R	R	R
1	0	1	0		MJR	REV<5:2>	
bit 15		•		·			bit 8
R	R	R	R	R	R	R	R
MJRREV<1:0>				MNRRI	EV<5:0>		
bit 7							bit 0
l egend:							
R = Readable bit '1' = B		'1' = Bit is set		0' = Bit is clea	ared	x = Bit is unki	nown
bit 15-12 R e	ad as '10	010'					

 bit 11-6
 MJRREV<5:0>: Major Revision ID bits

 These bits are used to identify a major revision. A major revision is indicated by an all-layer revision (A0, B0, C0, etc.).

 Revision A = 6 'b00_0000

 bit 5-0
 MNRREV<5:0>: Minor Revision ID bits

These bits are used to identify a minor revision.

R-q/q	R-q/q	R-q/q	R-q/q	R-q/q	R-q/q	U-0	R-q/q
EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	iown	-n/n = Value	at POR and BC	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared	q = Reset va	lue is determine	ed by hardware	•
bit 7	EXTOR: EXT	OSC (external)	Oscillator Re	ady bit			
	1 = The os	cillator is ready	to be used	4 4			
h # 0		TOOO On sillator	abled, or is no	t yet ready to t	be used		
DIT 6	1 = The os	cillator is ready	to be used				
	0 = The oscillation	cillator is not en	abled, or is no	t yet ready to b	be used		
bit 5	MFOR: MFIN	TOSC Oscillate	or Ready				
	1 = The osc	cillator is ready	to be used				
	0 = The osc	cillator is not en	abled, or is no	t yet ready to b	be used		
bit 4	LFOR: LFIN	TOSC Oscillato	r Ready bit				
	1 = 1he os	cillator is ready	to be used	t vet ready to h			
hit 3	SOR: Second	dary (Timer1) (scillator Read	v hit			
Sito	1 = The os	cillator is ready	to be used	y bit			
	0 = The os	cillator is not en	abled, or is no	ot yet ready to	be used		
bit 2	ADOR: ADC	Oscillator Read	dy bit				
	1 = The os	cillator is ready	to be used				
1. 11. A	0 = The os	cillator is not en	abled, or is no	ot yet ready to	be used		
Dit 1	Unimplemen	ted: Read as	0.				
bit 0	PLLR: PLL is	s Ready bit	uppd				
	1 = The PL	L is not enabled	, the required	input source is	s not ready, or t	he PLL is not lo	ocked.
			.,				

REGISTER 4-4: OSCSTAT: OSCILLATOR STATUS REGISTER 1

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2: If the prefetched instruction clears the interrupt enable or GIEH/L, ISR vectoring will not occur, but DOZEN is cleared and the CPU will resume execution at full speed.

9.7 Operation During Sleep

When the device enters Sleep, the WWDT is cleared. If the WWDT is enabled during Sleep, the WWDT resumes counting. When the device exits Sleep, the WWDT is cleared again.

The WWDT remains clear until the Oscillator Start-up Timer (OST) completes, if enabled. See **Section 4.3.1.3 "Oscillator Start-up Timer (OST)**" for more information on the OST.

When a WWDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The TO and PD bits in the STATUS register are changed to indicate the event. The RWDT bit in the PCON0 register can also be used. See **Section 10.0 "Memory Organization"** for more information.

TABLE 9-2: WWDT CLEARING CONDITIONS

Conditions	WWDT	
WDTE<1:0> = 00		
WDTE<1:0> = 01 and SEN = 0		
WDTE<1:0> = 10 and enter Sleep	Cleared	
CLRWDT Command	Cleared	
Oscillator Fail Detected		
Exit Sleep + System Clock = SOSC, EXTRC, INTOSC, EXTCLK		
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST	
Change INTOSC divider (IRCF bits)	Unaffected	

FIGURE 9-2: WINDOW PERIOD AND DELAY



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10.6 Data Addressing Modes

Note:	The execution of some instructions in the
	core PIC18 instruction set are changed
	when the PIC18 extended instruction set is
	enabled. See Section 10.7 "Data Mem-
	ory and the Extended Instruction Set"
	for more information.

While the program memory can be addressed in only one way – through the program counter – information in the data memory space can be addressed in several ways. For most instructions, the addressing mode is fixed. Other instructions may use up to three modes, depending on which operands are used and whether or not the extended instruction set is enabled.

The addressing modes are:

- Inherent
- Literal
- Direct
- Indirect

An additional addressing mode, Indexed Literal Offset, is available when the extended instruction set is enabled (XINST Configuration bit = 1). Its operation is discussed in greater detail in **Section 10.7.1 "Indexed Addressing with Literal Offset**".

10.6.1 INHERENT AND LITERAL ADDRESSING

Many PIC18 control instructions do not need any argument at all; they either perform an operation that globally affects the device or they operate implicitly on one register. This addressing mode is known as Inherent Addressing. Examples include SLEEP, RESET and DAW.

Other instructions work in a similar way but require an additional explicit argument in the opcode. This is known as Literal Addressing mode because they require some literal value as an argument. Examples include ADDLW and MOVLW, which respectively, add or move a literal value to the W register. Other examples include CALL and GOTO, which include a 20-bit program memory address.

10.6.2 DIRECT ADDRESSING

Direct addressing specifies all or part of the source and/or destination address of the operation within the opcode itself. The options are specified by the arguments accompanying the instruction.

In the core PIC18 instruction set, bit-oriented and byteoriented instructions use some version of direct addressing by default. All of these instructions include some 8-bit literal address as their Least Significant Byte. This address specifies either a register address in one of the banks of data RAM (Section 10.4.3 "General Purpose Register File") or a location in the Access Bank (Section 10.4.2 "Access Bank") as the data source for the instruction. The Access RAM bit 'a' determines how the address is interpreted. When 'a' is '1', the contents of the BSR (Section 10.4.1 "Bank Select Register (BSR)") are used with the address to determine the complete 12-bit address of the register. When 'a' is '0', the address is interpreted as being a register in the Access Bank. Addressing that uses the Access RAM is sometimes also known as Direct Forced Addressing mode.

A few instructions, such as MOVFF, include the entire 12-bit address (either source or destination) in their opcodes. In these cases, the BSR is ignored entirely.

The destination of the operation's results is determined by the destination bit 'd'. When 'd' is '1', the results are stored back in the source register, overwriting its original contents. When 'd' is '0', the results are stored in the W register. Instructions without the 'd' argument have a destination that is implicit in the instruction; their destination is either the target register being operated on or the W register.

10.6.3 INDIRECT ADDRESSING

Indirect addressing allows the user to access a location in data memory without giving a fixed address in the instruction. This is done by using File Select Registers (FSRs) as pointers to the locations which are to be read or written. Since the FSRs are themselves located in RAM as Special File Registers, they can also be directly manipulated under program control. This makes FSRs very useful in implementing data structures, such as tables and arrays in data memory.

The registers for indirect addressing are also implemented with Indirect File Operands (INDFs) that permit automatic manipulation of the pointer value with auto-incrementing, auto-decrementing or offsetting with another value. This allows for efficient code, using loops, such as the example of clearing an entire RAM bank in Example 10-5.

EXAMPLE 10-5: HOW TO CLEAR RAM (BANK 1) USING INDIRECT ADDRESSING

	LFSR	FSR0,	10 0h	;	
NEXT	CLRF	POSTIN	C0	;	Clear INDF
				;	register then
				;	inc pointer
	BTFSS	FSROH,	1	;	All done with
				;	Bankl?
	BRA	NEXT		;	NO, clear next
CONTINUE				;	YES, continue

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11.1.6.1 Program Flash Memory Write Sequence

The sequence of events for programming an internal program memory location should be:

- 1. Read appropriate number of bytes into RAM. Refer to Table 11-2 for Write latch size.
- 2. Update data values in RAM as necessary.
- 3. Load Table Pointer register with address being erased.
- 4. Execute the block erase procedure.
- 5. Load Table Pointer register with address of first byte being written.
- Write the n-byte block into the holding registers with auto-increment. Refer to Table 11-2 for Write latch size.
- 7. Set NVMREG<1:0> bits to point to program memory.
- 8. Clear FREE bit and set WREN bit in NVMCON1 register.
- 9. Disable interrupts.
- 10. Execute the unlock sequence (see Section 11.1.4 "NVM Unlock Sequence").
- 11. WR bit is set in NVMCON1 register.
- 12. The CPU will stall for the duration of the write (about 2 ms using internal timer).
- 13. Re-enable interrupts.
- 14. Verify the memory (table read).

This procedure will require about 6 ms to update each write block of memory. An example of the required code is given in Example 11-4.

Note: Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the bytes in the holding registers.

13.3 CRC Functional Overview

The CRC module can be used to detect bit errors in the Flash memory using the built-in memory scanner or through user input RAM memory. The CRC module can accept up to a 16-bit polynomial with up to a 16-bit seed value. A CRC calculated check value (or checksum) will then be generated into the CRCACC<15:0> registers for user storage. The CRC module uses an XOR shift register implementation to perform the polynomial division required for the CRC calculation.

EXAMPLE 13-1: CRC EXAMPLE



corresponding CRCXOR<15:0> bits with the value of

0x8004. The actual value is 0x8005 because the

hardware sets the LSb to 1. However, the LSb of the

CRCXORL register is unimplemented and always

reads as '0'. Refer to Example 13-1.

13.4 CRC Polynomial Implementation

Any polynomial can be used. The polynomial and accumulator sizes are determined by the PLEN<3:0> bits. For an n-bit accumulator, PLEN = n-1 and the corresponding polynomial is n+1 bits. Therefore, the accumulator can be any size up to 16 bits with a corresponding polynomial up to 17 bits. The MSb and LSb of the polynomial are always '1' which is forced by hardware. All polynomial bits between the MSb and LSb are specified by the CRCXOR registers. For example, when using CRC16-ANSI, the polynomial is defined as $X^{16}+X^{15}+X^2+1$. The X^{16} and $X^0 = 1$ terms are the MSb and LSb controlled by hardware. The X^{15} and X^2 terms are specified by setting the





13.5 CRC Data Sources

Data can be input to the CRC module in two ways:

- User data using the CRCDATA registers (CRCDATH and CRCDATL)
- Flash using the Program Memory Scanner

To set the number of bits of data, up to 16 bits, the DLEN bits of CRCCON1 must be set accordingly. Only data bits in CRCDATA registers up to DLEN will be used, other data bits in CRCDATA registers will be ignored.

Data is moved into the CRCSHIFT as an intermediate to calculate the check value located in the CRCACC registers.

The SHIFTM bit is used to determine the bit order of the data being shifted into the accumulator. If SHIFTM is not set, the data will be shifted in MSb first (Big Endian). The value of DLEN will determine the MSb. If SHIFTM bit is set, the data will be shifted into the accumulator in reversed order, LSb first (Little Endian).

The CRC module can be seeded with an initial value by setting the CRCACC<15:0> registers to the appropriate value before beginning the CRC.

13.5.1 CRC FROM USER DATA

To use the CRC module on data input from the user, the user must write the data to the CRCDAT registers. The data from the CRCDAT registers will be latched into the shift registers on any write to the CRCDATL register.

13.5.2 CRC FROM FLASH

To use the CRC module on data located in Flash memory, the user can initialize the Program Memory Scanner as defined in Section 13.9, Program Memory Scan Configuration.

14.4 INTCON Registers

The INTCON registers are readable and writable registers, which contain various enable and priority bits.

14.5 PIR Registers

The PIR registers contain the individual flag bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are eight Peripheral Interrupt Request Flag registers (PIR0, PIR1, PIR2, PIR3, PIR4, PIR5, PIR6 and PIR7).

14.6 PIE Registers

The PIE registers contain the individual enable bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are eight Peripheral Interrupt Enable registers (PIE0, PIE1, PIE2, PIE3, PIE4, PIE5, PIE6 and PIE7). When IPEN = 0, the PEIE/GIEL bit must be set to enable any of these peripheral interrupts.

14.7 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are eight Peripheral Interrupt Priority registers (IPR0, IPR1, IPR2, IPR3, IPR4 and IPR5, IPR6 and IPR7). Using the priority bits requires that the Interrupt Priority Enable (IPEN) bit be set.

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20.5.6 EDGE-TRIGGERED ONE-SHOT MODE

The Edge-Triggered One-Shot modes start the timer on an edge from the external signal input, after the ON bit is set, and clear the ON bit when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 01001)
- Falling edge (MODE<4:0> = 01010)
- Rising or Falling edge (MODE<4:0> = 01011)

If the timer is halted by clearing the ON bit then another TMRx_ers edge is required after the ON bit is set to resume counting. Figure 20-9 illustrates operation in the rising edge One-Shot mode.

When Edge-Triggered One-Shot mode is used in conjunction with the CCP then the edge-trigger will activate the PWM drive and the PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated when the timer halts at the PRx period count match.

FIGURE 20-9: EDGE-TRIGGERED ONE-SHOT MODE TIMING DIAGRAM (MODE = 01001)



20.5.7 EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE

In Edge-Triggered Hardware Limit One-Shot modes the timer starts on the first external signal edge after the ON bit is set and resets on all subsequent edges. Only the first edge after the ON bit is set is needed to start the timer. The counter will resume counting automatically two clocks after all subsequent external Reset edges. Edge triggers are as follows:

- Rising edge start and Reset (MODE<4:0> = 01100)
- Falling edge start and Reset (MODE<4:0> = 01101)

The timer resets and clears the ON bit when the timer value matches the PRx period value. External signal edges will have no effect until after software sets the ON bit. Figure 20-10 illustrates the rising edge hardware limit one-shot operation.

When this mode is used in conjunction with the CCP then the first starting edge trigger, and all subsequent Reset edges, will activate the PWM drive. The PWM drive will deactivate when the timer matches the CCPRx pulse-width value and stay deactivated until the timer halts at the PRx period match unless an external signal edge resets the timer before the match occurs.

23.2 ZCD Logic Output

The ZCD module includes a Status bit, which can be read to determine whether the current source or sink is active. The ZCDOUT bit of the ZCDCON register is set when the current sink is active, and cleared when the current source is active. The ZCDOUT bit is affected by the polarity bit.

The ZCDOUT signal can also be used as input to other modules. This is controlled by the registers of the corresponding module. ZCDOUT can be used as follows:

- Gate source for TMR1/3/5
- Clock source for TMR2/4/6
- Reset source for TMR2/4/6

23.3 ZCD Logic Polarity

The ZCDPOL bit of the ZCDCON register inverts the ZCDOUT bit relative to the current source and sink output. When the ZCDPOL bit is set, a ZCDOUT high indicates that the current source is active, and a low output indicates that the current sink is active.

The ZCDPOL bit affects the ZCD interrupts.

23.4 ZCD Interrupts

An interrupt will be generated upon a change in the ZCD logic output when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in the ZCD for this purpose.

The ZCDIF bit of the PIR2 register will be set when either edge detector is triggered and its associated enable bit is set. The ZCDINTP enables rising edge interrupts and the ZCDINTN bit enables falling edge interrupts. Both are located in the ZCDCON register. Priority of the interrupt can be changed if the IPEN bit of the INTCON register is set. The ZCD interrupt can be made high or low priority by setting or clearing the ZCDIP bit of the IPR2 register.

To fully enable the interrupt, the following bits must be set:

- · ZCDIE bit of the PIE2 register
- ZCDINTP bit of the ZCDCON register (for a rising edge detection)
- ZCDINTN bit of the ZCDCON register (for a falling edge detection)
- · PEIE and GIE bits of the INTCON register

Changing the ZCDPOL bit will cause an interrupt, regardless of the level of the ZCDSEN bit.

The ZCDIF bit of the PIR2 register must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

23.5 Correcting for VCPINV offset

The actual voltage at which the ZCD switches is the reference voltage at the non-inverting input of the ZCD op amp. For external voltage source waveforms other than square waves, this voltage offset from zero causes the zero-cross event to occur either too early or too late.

23.5.1 CORRECTION BY AC COUPLING

When the external voltage source is sinusoidal, the effects of the ZCPINV offset can be eliminated by isolating the external voltage source from the ZCD pin with a capacitor, in addition to the voltage reducing resistor. The capacitor will cause a phase shift resulting in the ZCD output switch in advance of the actual zero-crossing event. The phase shift will be the same for both rising and falling zero crossings, which can be compensated for by either delaying the CPU response to the ZCD switch by a timer or other means, or selecting a capacitor value large enough that the phase shift is negligible.

To determine the series resistor and capacitor values for this configuration, start by computing the impedance, Z, to obtain a peak current of $300 \ \mu$ A. Next, arbitrarily select a suitably large non-polar capacitor and compute its reactance, Xc, at the external voltage source frequency. Finally, compute the series resistor, capacitor peak voltage, and phase shift by the formulas shown in Equation 23-2.

When this technique is used and the input signal is not present, the ZCD will tend to oscillate. To avoid this oscillation, connect the ZCD pin to VDD or GND with a high-impedance resistor such as 200K.



DEAD-BAND OPERATION, CWG1DBR = 0x01, CWG1DBF = 0x02

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TABLE 27-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDxCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	395
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	_	_	INT2EDG	INT1EDG	INT0EDG	170
PIE3	RC2IE	TX2IE	RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	174
PIR3	RC2IF	TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	174
IPR3	RC2IP	TX2IP	RC1IP	TX1IP	BCL2IP	SSP2IP	BCL1IP	SSP1IP	190
RCxSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	394
RxyPPS	—	—	_	- RxyPPS<4:0>					
TXxPPS	—	—	_	- TXPPS<4:0>					216
SPxBRGH	EUSARTx Baud Rate Generator, High Byte						404*		
SPxBRGL	EUSARTx Baud Rate Generator, Low Byte						404*		
TXxREG	EUSARTx Transmit Register						396*		
TXxSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	393

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous transmission. * Page provides register information.

FIGURE 27-7: AUTO-WAKE-UP BIT (WUE) TIMING DURING NORMAL OPERATION

64636463. 2022/12/12/13:03695 686/686 	204.00 90290 204.00 9070 297.2867			2909.0308 U.U.U.U.U. 		andre nan VAN VAN			union and an anna anna anna anna anna anna
						· · · · · · · · · · · · · · · · · · ·			
	: : !//////////////////////////////////	: : 21 230 2630	: ////////////////////////////////////			Stevenis Millinninninnin Millinninninninnin	ise is ipeer ie 11111111111111111111	996 (S. Ş. 1111111111	CAREAP IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII
FIGURE 27-8:	AUT	O-WAKE	-UP BIT	(WUE) T	IMINGS I		SLEEP		



St. - The SUBARY remains in the white the Vibe hit is set

31.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of
	every conversion, regardless of whether
	or not the ADC interrupt is enabled.

2: The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the ADIE bit of the PIE1 register and the PEIE bit of the INTCON register must both be set and the GIE bit of the INTCON register must be cleared. If all three of these bits are set, the execution will switch to the Interrupt Service Routine.

31.1.6 RESULT FORMATTING

The 10-bit ADC conversion result can be supplied in two formats, left justified or right justified. The ADFM bits of the ADCON0 register controls the output format.

Figure 31-3 shows the two output formats.

FIGURE 31-3: 10-BIT ADC CONVERSION RESULT FORMAT



32.9 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Table 37-15 and Table 37-17 for more details.

32.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 32-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10 \text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

- Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
 - 2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.



40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

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