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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	-
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-eTQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc570s40e1cefar

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2 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. Block diagram

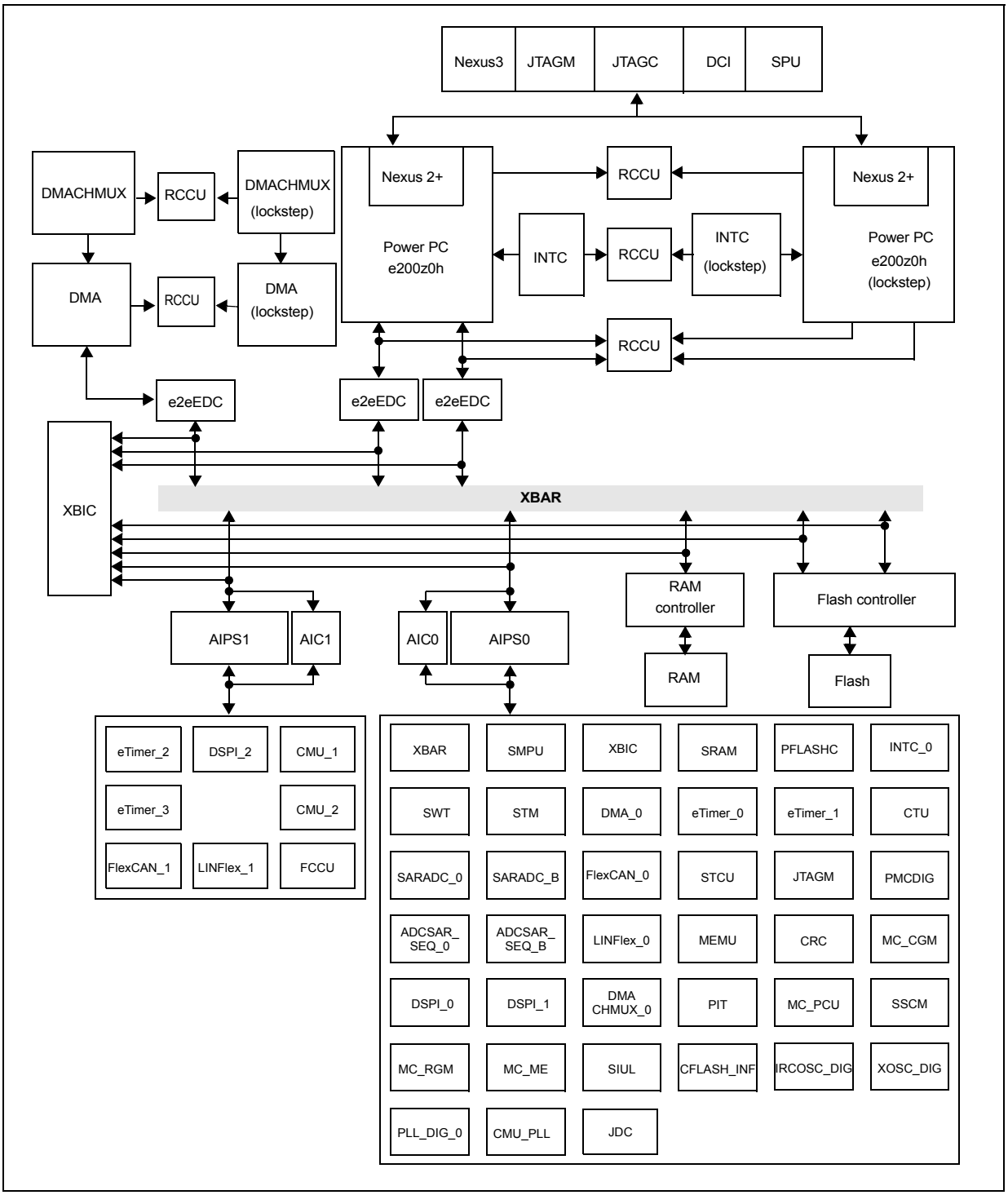


Table 3 summarizes the functions of all blocks present in the SPC570Sx series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. SPC570Sx series block summary

Block	Function
e200z0 CPU	Allows single clock instruction execution
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via 16 programmable channels.
DMACHMUX	Allows to route a defined number of DMA peripheral sources to the DMA channels
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
PLL0	Output independent of core clock frequency
Frequency-modulated phase-locked loop (PLL1)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
AIPS	System bus to peripheral bus interface
RAM controller	Acts as an interface between the system bus and the integrated system RAM
System RAM	Supports read/write accesses mapped to the SRAM memory from any master
Flash memory controller	Acts as an interface between the system bus and the Flash memory module
Flash memory	Up to 512 KB of programmable, non-volatile Flash memory for code and 32 KB for data
IRCOSC	Controls the internal 16 MHz RC oscillator system
XOSC	Controls the on-chip oscillator (XOSC) and provides the register interface for the programmable features
JTAG Master	Provides software the option to write data for driving JTAG
JTAG Data Communication Module	Provides the capability to move register data between the IPS and JTAG domains
PASS	Programs a set of Flash memory access protections, based on user programmable passwords
Sequence Processing Unit	Provides an on-device trigger functions similar to those found on a logic analyzer
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load

Table 3. SPC570Sx series block summary (continued)

Block	Function
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

4.3 Absolute maximum ratings

Table 6. Absolute maximum ratings (1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	T	Lifetime power cycles	—	—	1000k	—
V_{SS}	C	Ground voltage	—	—	—	—
V_{DD_LV}	C	1.2 V core supply voltage	—	-0.3	1.5	V
$V_{DD\_HV\_IO}$	C	I/O supply voltage(2)	—	-0.3	6.0	V
$V_{DD\_HV\_OSC\_PMC}$	C	Power management unit and OSC power supply	—	-0.3	6.0	V
$V_{DD\_HV\_ADC\_TSENS}$	C	ADC & TSENS power supply	—	-0.3	6.0	V
V_{REFH_ADC}	C	ADC reference supply	—	0	$V_{DD\_HV\_ADC\_TSENS}$	V
V_{IN}	C	I/O input voltage range(3)	—	-0.3	6.0	V
			Relative to V_{SS}	-0.3	—	
			Relative to $V_{DD\_HV\_IO}$	—	0.3	
I_{INJD}	T	Maximum DC injection current for digital pad during overload condition	Per pin, applies to all digital pins	-3	3	mA
I_{INJA}	T	Maximum DC injection current for analog pad during overload condition	Per pin, applies to all analog pins	-3	3	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	-7	8	mA
			Strong	-10	10	
			Very strong	-11	11	
I_{MAXSEG}	SR	Maximum current per power segment(4)	—	-90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	-55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range -40 °C to 85 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature(5) Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level(6)	—	—	3	—
t_{XRAY}	SR	X-ray screen time	At 80÷130 KV; 20÷50 µA; max 1 Gy dose	—	200	ms

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device. During overload conditions (V_{IN} > $V_{DD\_HV\_IO}$ or V_{IN} < V_{SS}), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

2. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C remaining time at or below 5.5 V.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
4. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
5. Solder profile per IPC/JEDEC J-STD-020D
6. Moisture sensitivity per JEDEC test method A112

4.4 Electromagnetic compatibility (EMC)

Table 7 describes the EMC characteristics of the device.

Table 7. Radiated emissions testing specification(1),(2)

Coupling structure	Test setup	Function	Functional configuration	BISS radiated emissions limit
Entire IC	(G) TEM	Reference test	C1-S3	18 dBµV
		Reference test with SSCG	C1-S3	18 dBµV
		Memory copy	C4-S2	18 dBµV
		Memory copy with SSCG	C4-S2	18 dBµV

1. Reference “BISS Generic IC EMC Test Specification”, version 1.2, section 9.3, “Emission test configuration for ICs with CPU”.
2. The EMC parameters are classified as "T", validated on testbench.

4.5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 8. ESD ratings(1),(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

4.9.2 I/O input DC characteristics

Table 13 provides input DC electrical characteristics as described in *Figure 4*.

Figure 4. I/O input DC electrical characteristics definition

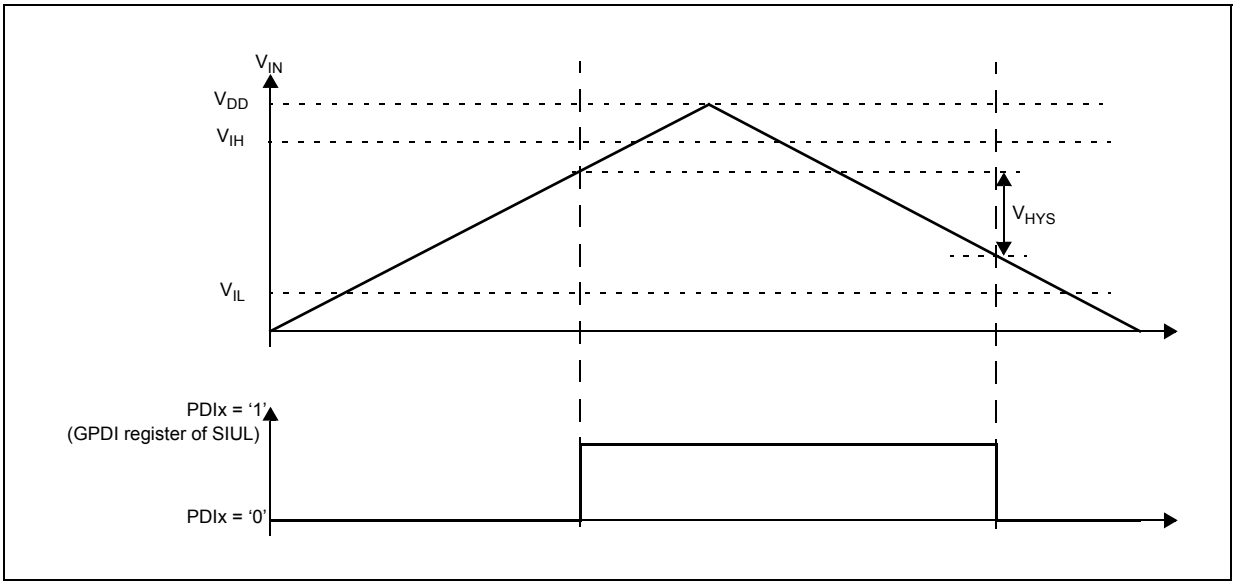


Table 13. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{IH}	SR	P	Input high level TTL	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.0	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL}	SR	P	Input low level TTL	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	0.8	
V_{HYST}	—	C	Input hysteresis TTL	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.3(1)	—	—	
CMOS								
V_{IHCMOS_H}(2)	SR	P	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IHCMOS}(2)	SR	P	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.6 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILCMOS_H}(2)	SR	P	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	0.35 * $V_{DD\_HV\_IO}$	V

Table 13. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ILCMOS}(2)	SR	P	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
$V_{HYSCMOS}$	—	C	Input hysteresis CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
Automotive								
V_{IH}(3)	SR	P	Input high level Automotive	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.75 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	
V_{IL}	SR	P	Input low level Automotive	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	2.2	V
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	-0.3	—	0.35 * $V_{DD\_HV\_IO}$	
V_{HYST}	—	C	Input hysteresis Automotive	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.5	—	—	V
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.11 * $V_{DD\_HV\_IO}$	—	—	
Input Characteristics								
I_{LKG}	CC	P	Digital input leakage	—	—	—	1	µA
C_{IN}	C	D	Digital input capacitance	—	—	—	10	pF

1. Minimum hysteresis at 4.0 V
2. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V.
3. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V.

Table 14 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up/down current absolute value(1)	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	23	—	—	µA
				V_{IN} = 0.49 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	82	
				V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	
	CC	T		V_{IN} = 0.75 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	10	—	—	
				V_{IN} = 0.35 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	70	
				V_{IN} > V_{IL} = 1.1 V (TTL) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	75	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	µA
				V_{IN} = 0.49 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	—	
				V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	16	—	—	
	CC	T		V_{IN} = 0.75 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	92	
				V_{IN} = 0.35 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	19	—	—	
				V_{IN} > V_{IL} = 1.1 V (TTL) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	16	—	—	

1. Weak pull-up/down is enabled within t_{WK_PU} = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.

4.9.3 I/O output DC characteristics

Table 15: Weak configuration I/O output characteristics, provide DC characteristics for bidirectional pads in the following configurations:

- Weak
- Medium
- Strong
- Very Strong

Table 19. I/O output characteristics for pads 4, 9, 11, 55, 56 (continued)

Functionality	Symbol	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Medium	R_{OH_M}	PMOS output impedance medium configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	—	—	405	Ω
	R_{OL_M}	NMOS output impedance medium configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	—	—	495	Ω
	f_{max_M}	Output frequency medium configuration	C_L = 25 pF	—	—	12	MHz
			C_L = 50 pF	—	—	6	
	t_{TR_M}	Transition time output pin medium configuration	C_L = 25 pF	—	—	34	ns
			C_L = 50 pF	—	—	62	
	t_{SKEW_M}	Difference between rise time and fall time	—	—	—	46	%

4.10 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

Note: $\overline{PORST}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 Kohm.

Figure 5. Start-up reset requirements

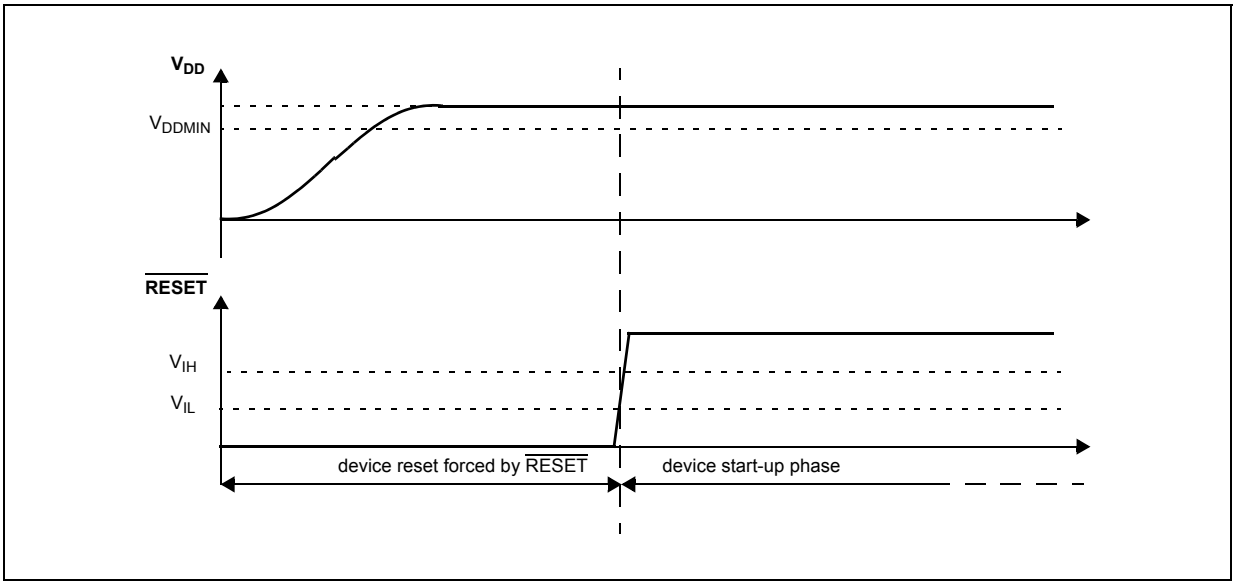


Table 24. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1]	Value									Unit
		Typ [2]	C	Initial max			Typical end of life[3]	Lifetime max[4]		C	
				25 °C [5]	All temp [6]	C		≤ 1 K cycles	≤ 100 K cycles		
t_{AIC0P}	Array Integrity Check (0.5 MB, proprietary)[11]	0.75	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (0.5 MB, sequential)	25	T	—	—	—	—	—	—	—	ms
$t_{MR128KS}$	Margin Read (128 KB, sequential)	6.26	T	—	—	—	—	—	—	—	ms
t_{AABT}	Array Integrity Check Abort Latency	—	—	—	—	—	—	10		—	µs
t_{MABT}	Margin Read Abort Latency	—	—	—	—	—	—	10		—	µs

1. Actual hardware programming times; this does not include software overhead.
2. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
3. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
4. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
5. Initial factory condition: < 100 program/erase cycles, 20 °C < T_J < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
6. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, -40 °C < T_J < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Rate computed based on 128K sectors.
8. Only code sectors, not including EEPROM.
9. Time between erase suspend resume and next erase suspend.
10. Timings guaranteed by design.
11. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at 80 MHz.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 25. Flash memory Life Specification

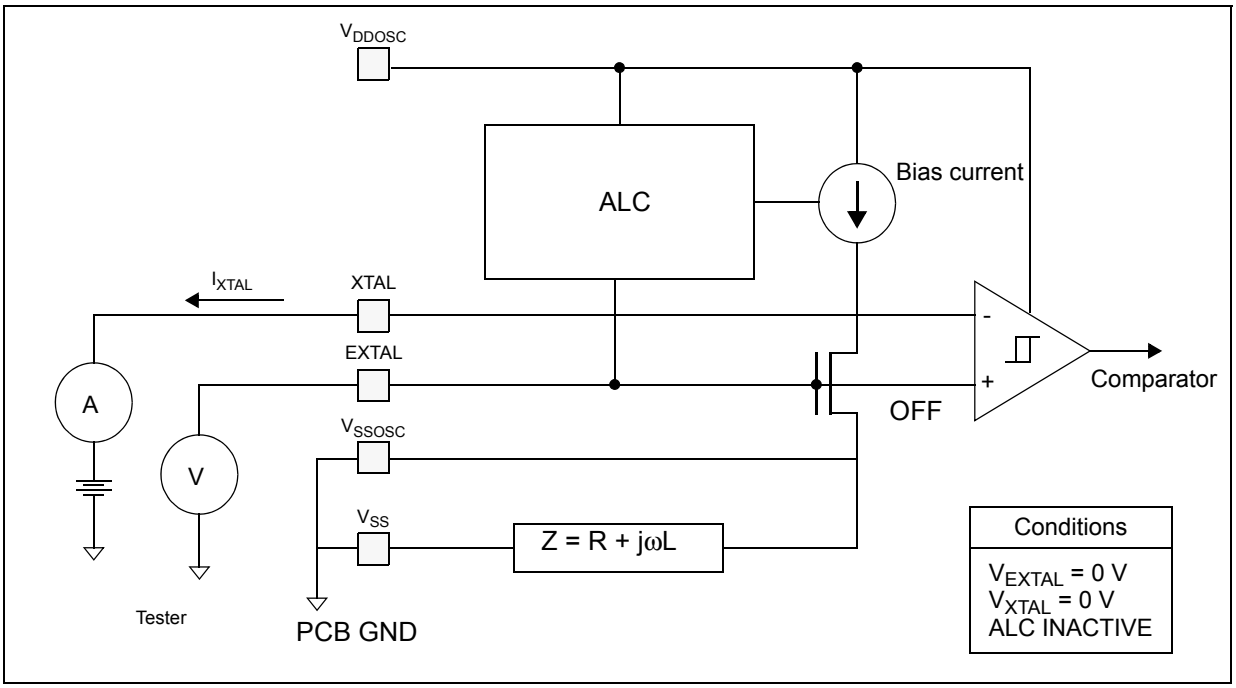
Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles

Table 29. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance offered on EXTAL/XTAL (Cx and Cy)(1) (pF)
00000	1.032
00001	1.976
00010	2.898
00011	3.823
00100	4.751
00101	5.679
00110	6.605
00111	7.536
01000	8.460
01001	9.390
01010	10.317
01011	11.245
01100	12.173
01101	13.101
01110	14.029
01111	14.957

1. Values are determined from simulation with a tolerance of ±15%.

Figure 9. Test circuit



4.17 Internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 30. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation across temperature and voltage	—	-6	—	+6	%
δf_{var_SW}	—	T	IRC software trimming accuracy	Trimming temperature	-0.5	—	+0.5	%
t_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs

4.18.2 ADC electrical characteristics

Table 31. ADC input leakage current

Symbol		Parameter	Conditions		Value		Unit
					Min	Max	
I_{LKG}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_j < 40 °C	No current injection on adjacent pin	—	70	nA
			T_j < 150 °C		—	220	

Table 32. ADC conversion characteristics

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{IN}	SR		ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO}$	$V_{SS\_HV\_ADR}$(1)	V_{REFH_ADC}	V
f_{ADCK}	SR	P	Clock frequency	—	7.5	12	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	—	83	—	ns
V_{PRECH}	SR	D	Precharge voltage	—	—	0.25	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * V_{REFH_ADC}, 2/3 * V_{REFH_ADC}, V_{REFH_ADC})	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time	SAR – 12-bit configuration	0.5	—	µs
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (12 clock cycles)	1.000	—	µs
		D		10-bit configuration (10 clock cycles)	0.833		
$I_{ADCREFH}$(2)	CC	C	ADC high reference current (average across all codes)	Run mode	—	15	µA
				Power Down mode	—	1	
I_{ADCVDD}	CC	P	$V_{DD\_HV\_ADC\_TSENS}$ power supply current	Run mode	—	4.0	mA
				Power Down mode	—	0.04	
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration	V_{REFH_ADC} > 3 V	-6	6	LSB (12b)
				3 V > V_{REFH_ADC} > 2 V	-9	9	

4.19 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 33. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Temperature monitoring range	—	-40	—	165	°C
T_{SENS}	CC	P	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	C	Accuracy	T_J < 150 °C	-3	—	3	°C
I_{TEMP_SENS}	CC	C	VDD_HV_ADC_TSENS power supply current	—	—	—	700	µA

4.20 JTAG interface timings

Table 34. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDC}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%-70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	5	—	ns
6	t_{DOV}	D	TCK low to TDO data valid	—	—	30	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	30	ns
9	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 11. JTAG test clock input timing

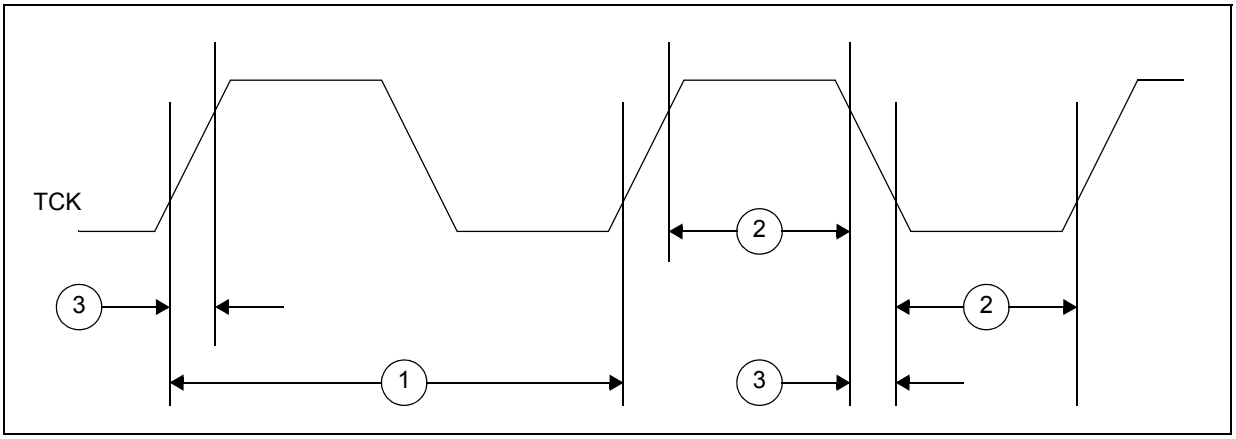


Figure 12. JTAG test access port timing

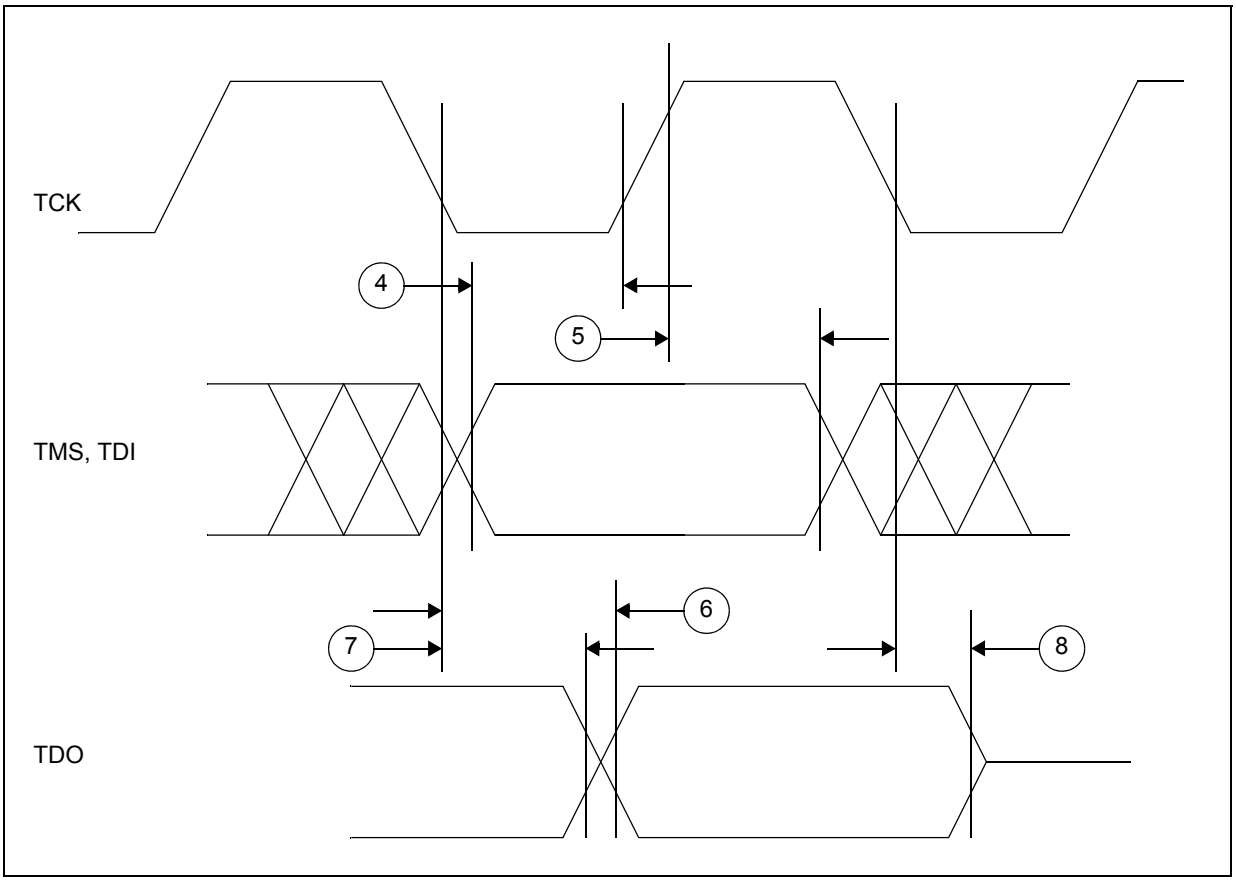


Figure 14. DSPI CMOS master mode – classic timing, CPHA = 0

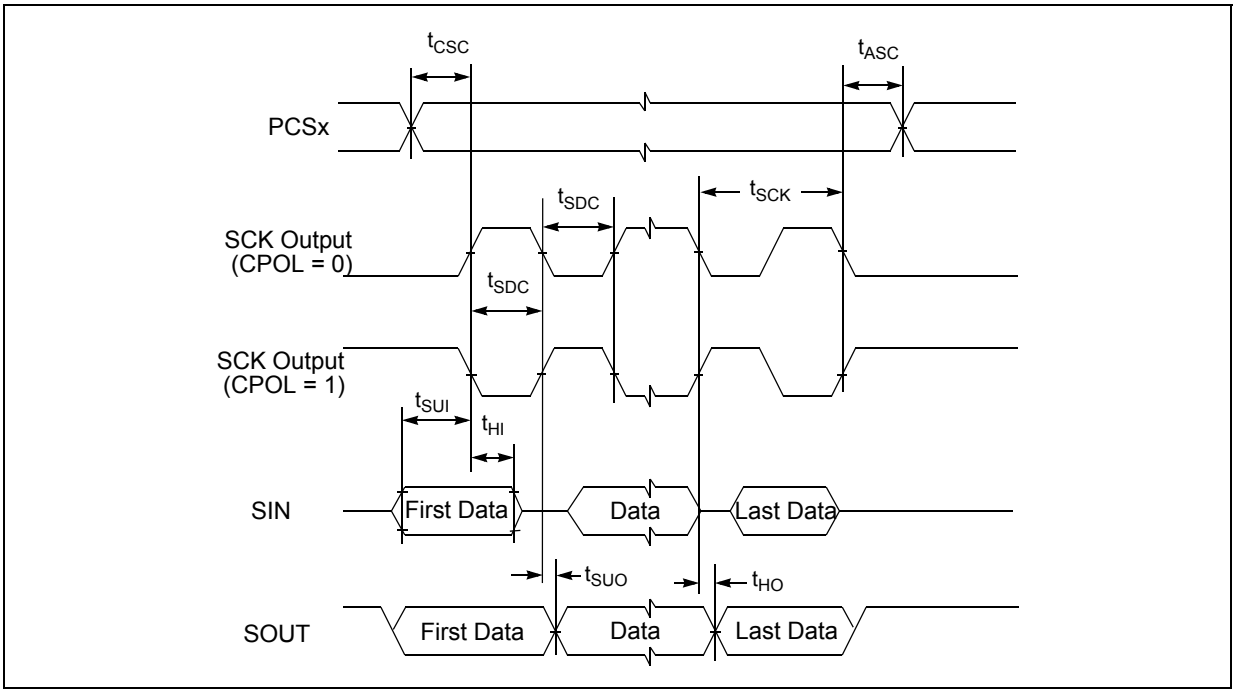


Figure 15. DSPI CMOS master mode – classic timing, CPHA = 1

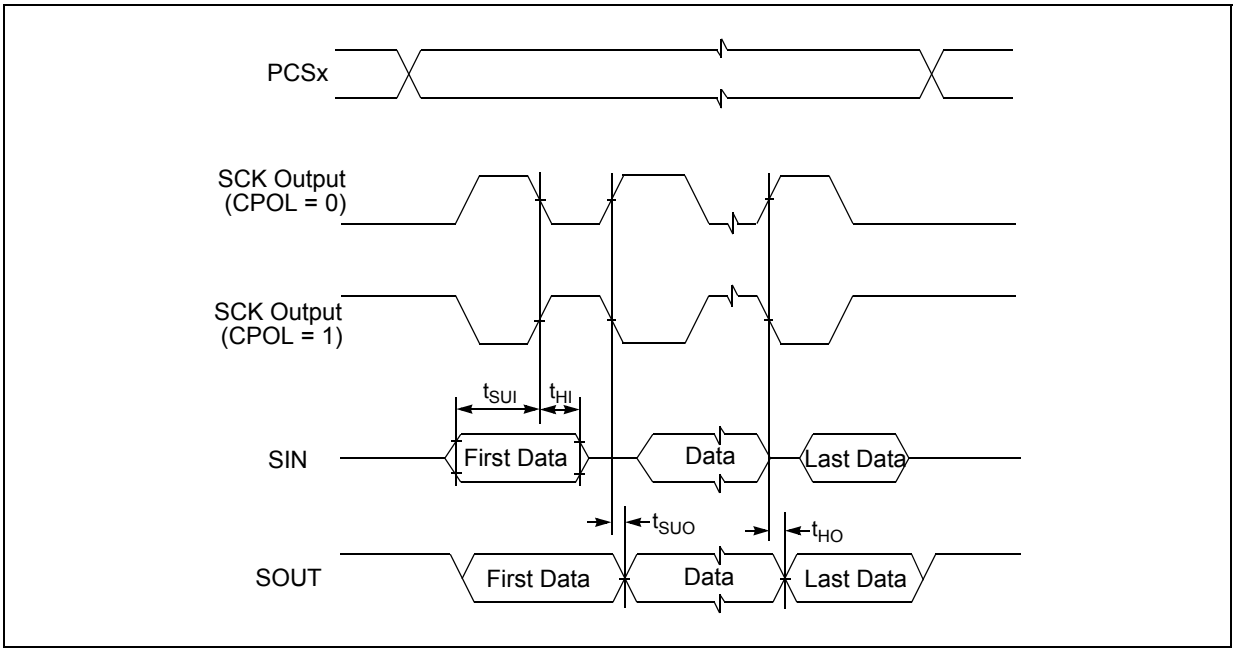


Table 38. eTQFP100 mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	—	—	1.20	—	—	0.0472
A1	—	0.05	0.15	—	0.0020	0.0059
A2	1.00	0.95	1.05	0.0394	0.0374	0.0413
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c	—	0.09	0.20	—	0.0035	0.0079
D	16.00	15.80	16.20	0.6299	0.6220	0.6378
D1	14.00	13.80	14.20	0.5512	0.5433	0.5591
D2	—	2.00	—	—	0.0787	—
D3	12.00	—	—	0.4724	—	—
E	16.00	15.80	16.20	0.6299	0.6220	0.6378
E1	14.00	13.80	14.20	0.5512	0.5433	0.5591
E2	—	2.00	—	—	0.0787	—
E3	12.00	—	—	0.4724	—	—
e	0.50	—	—	0.0197	—	—
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00	—	—	0.0394	—	—
k	3.5 °	0.0 °	7.0 °	3.5 °	0.0 °	7.0 °
ccc	—	—	0.08	—	—	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Note: TQFP stands for Thin Quad Flat Package.

Table 39. Document revision history (continued)

Date	Revision	Changes
26-Mar-2015	5	*Table 9: Device operating conditions*: – Added: $V_{DD\_HV\_OSC\_PMC}$, V_{REFH_ADC} - $V_{DD\_HV\_ADC\_TSENS}$, V_{IN}, I_{MAXSEG} – Changed values for: $V_{DD\_HV\_IO}$ – Updated parameter descriptions for: V_{REFH_ADC}, V_{REFH_ADC} - $V_{DD\_HV\_ADC\_TSENS}$ – Updated classification tags and footnotes for: $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_OSC\_PMC}$ – Removed: V_{DD_LV} *Table 13: I/O input DC electrical characteristics* – Added I_{LKG} – Changed conditions for: V_{IH}, V_{IL}, V_{HYST}, V_{IHCMOS_H}, $V_{IHCMOS}^{(2)}$, $V_{ILCMOS\_H}^{(2)}$, $V_{ILCMOS}^{(2)}$, $V_{HYSCMOS}$ – Changed values for: V_{IH}, V_{IL}, C_{IN} – Removed 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V conditions from the *Automotive* section Updated *Table 14: I/O pull-up/pull-down DC electrical characteristics* Removed “Min” values from tables: *15*, *16*, *17*, *19* Removed “Typ” values from tables: *15*, *16*, *17*, *18*, *19* Renamed *Table 19: I/O output characteristics for pads 4, 9, 11, 55, 56* to include the pad numbers *Table 20: Reset electrical characteristics* changed conditions and values for: I_{OL_R}, $\lvert I_{WPU}\rvert$, $\lvert I_{WPD}\rvert$ *Table 21: Voltage regulator electrical characteristics* – changed values and condition description for C_{DECBV} – removed $I_{MREGINT}$ *Table 24: Flash memory program and erase specifications* changed values for: t_{PSUS}, t_{ESUS} *Table 30: Internal RC oscillator electrical specifications* – Removed condition and changed values for df_{var_noT} – Changed values for df_{var_SW} *Table 32: ADC conversion characteristics* – Changed values for: $I_{ADCREFH}$, I_{ADCVDD}, *DNL* – Added footnotes for $V_{SS\_HV\_ADR}$ and $I_{ADCREFH}$
23-Sep-2015	6	*Table 6: Absolute maximum ratings*: – Updated t_{XRAY} *Table 11: Current consumption*: – Updated IDD information – Added classification tag, Min Typ and Max columns – Updated value of maximum consumption during boot time M/LBIST Tables *15*, *16*, *17*, *18*: – Added classification tag, Min Typ and Max columns *Table 22: Trimmed (PVT) values*: – Updated POR200 lower limit Removed “(pending silicon Qualification)” from the titles of *Table 24* and *Table 25* Corrected *Section 4.12.2: Power up/down sequencing* Reverted to using weak/medium/strong/very strong to describe pad strength