STMicroelectronics - SPC570S40E1CEFAY Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	-
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-eTQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc570s40e1cefay

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC570Sx is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC570Sx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of Chassis and Safety electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 80 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. SPC570Sx device feature summary (Family Superset Configuration)

Feature		Description
Process		55 nm
Main processor	Core	e200z0h
	Number of main cores	1
	Number of checker cores	1
	VLE	Yes
	Main processor frequency	80 MHz(1)
Interrupt controllers (including interrupt controller checker)		1
Software watchdog timer		1
System timers		1 AUTOSAR® STM 1 PIT with four 32-bit channels
DMA (including DMA checker)		1
DMA channels		16
SMPU		Yes (8 regions)(2)
System SRAM		48 KB
Code flash memory		512 KB
Data flash memory (suitable for EEPROM emulation)		32 KB

2 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. Block diagram

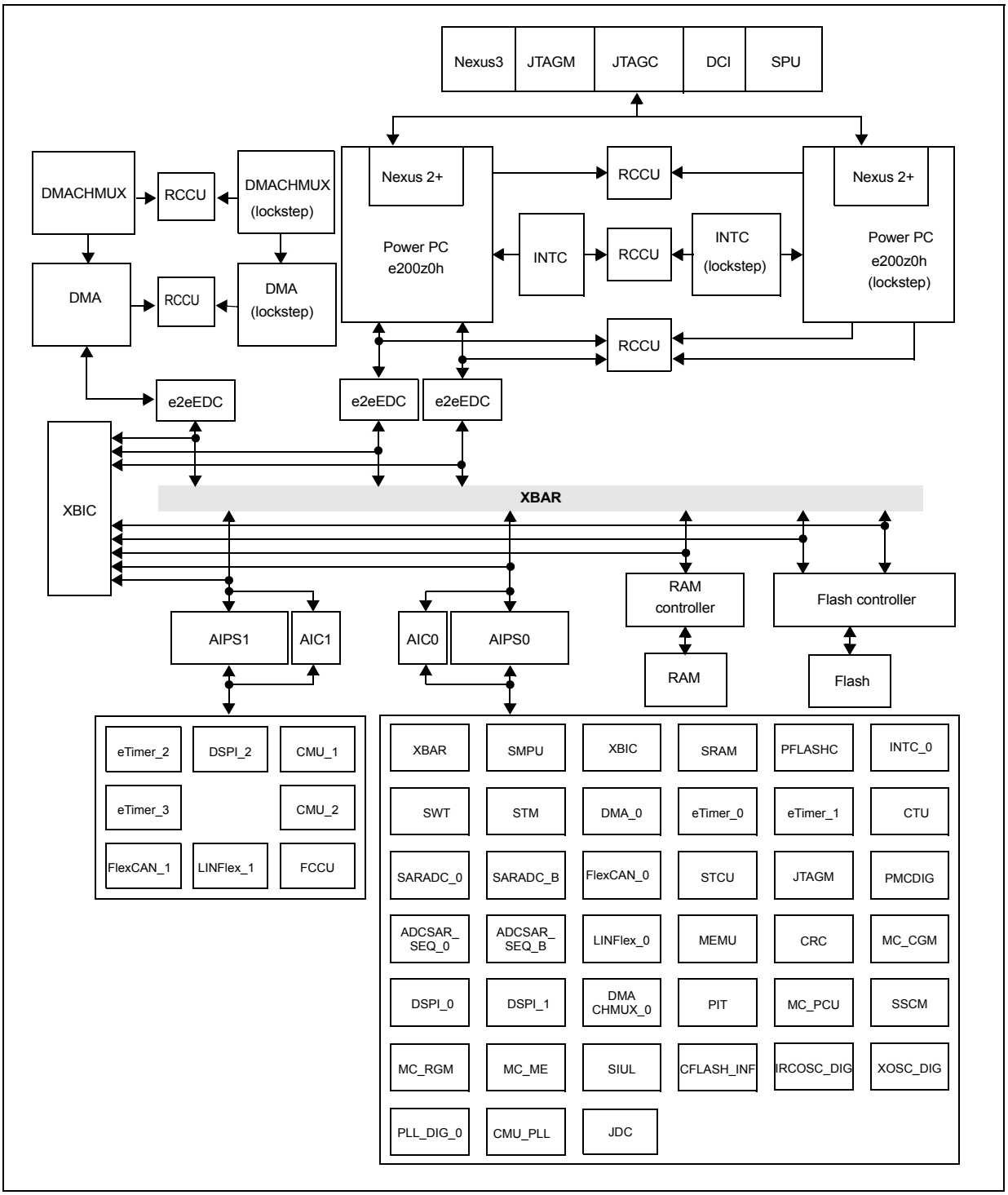


Table 3 summarizes the functions of all blocks present in the SPC570Sx series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

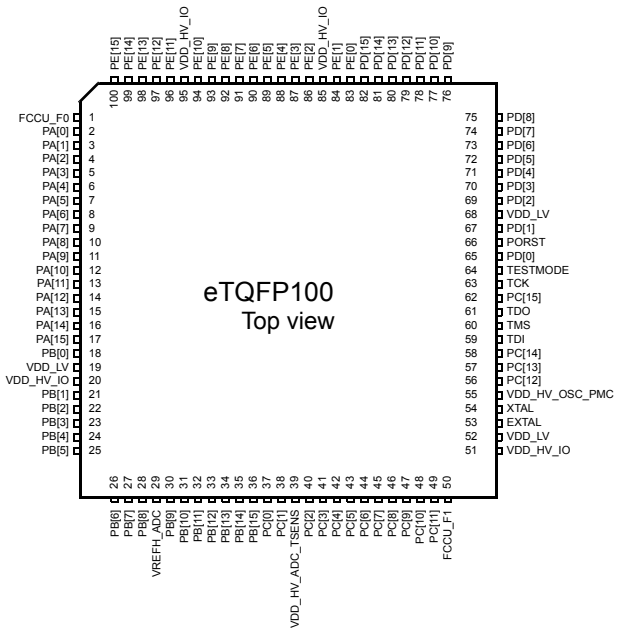
Table 3. SPC570Sx series block summary

Block	Function
e200z0 CPU	Allows single clock instruction execution
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via 16 programmable channels.
DMACHMUX	Allows to route a defined number of DMA peripheral sources to the DMA channels
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
PLL0	Output independent of core clock frequency
Frequency-modulated phase-locked loop (PLL1)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
AIPS	System bus to peripheral bus interface
RAM controller	Acts as an interface between the system bus and the integrated system RAM
System RAM	Supports read/write accesses mapped to the SRAM memory from any master
Flash memory controller	Acts as an interface between the system bus and the Flash memory module
Flash memory	Up to 512 KB of programmable, non-volatile Flash memory for code and 32 KB for data
IRCOSC	Controls the internal 16 MHz RC oscillator system
XOSC	Controls the on-chip oscillator (XOSC) and provides the register interface for the programmable features
JTAG Master	Provides software the option to write data for driving JTAG
JTAG Data Communication Module	Provides the capability to move register data between the IPS and JTAG domains
PASS	Programs a set of Flash memory access protections, based on user programmable passwords
Sequence Processing Unit	Provides an on-device trigger functions similar to those found on a logic analyzer
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load

Table 3. SPC570Sx series block summary (continued)

Block	Function
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
MC_PMC	Contains registers that enable/disable the various voltage monitors
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
eTimer	Has six 16-bit general purpose counter, where each counter can be used as input capture or output compare function
FCCU	Collects fault event notification from the rest of the system and translates them into internal and/or external system reactions
RCCU	Compares input signals and issues an alarm in the case of a mismatch
MEMU	Collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory
XBIC	Verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected
STCU2	Handles the BIST procedure
CRC	Controls the computation of CRC, off-loading this work from the CPU
RegProt	Protects several registers against accidental writing, locking their value till the next reset phase
Temperature sensor	Monitors the device temperature
Debug Control Interface	Provides debug features for the MCU
Nexus Port Controller	Monitor a variety of signals including addresses, data, control signals, status signals, etc.
Nexus Multimaster Trace Client	Monitors the system bus and provides real-time trace information to debug or development tools
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
System integration unit (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code

Figure 3. eTQFP 100-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PD[9]	PAD[57]	49	76	IO	FlexCAN 0 - RX	DSPI 2 - CS 1	FlexCAN 1 - RX	Timer 2 - ch. 2
PD[10]	PAD[58]	50	77	IO	FlexCAN 0 - TX	—	FlexCAN 1 - TX	Timer 2 - ch. 3
PD[11]	PAD[59]	51	78	IO	Timer 3 - ch. 2	DSPI 2 - CLK	DSPI 1 - CS 7	—
PD[12]	PAD[60]	—	79	IO	DSPI 2 - Serial Data	Timer 2 - ch. 3	DSPI 2 - CS 2	—
PD[13]	PAD[61]	—	80	IO	DSPI 2 - CLK	Timer 2 - ch. 4	DSPI 2 - CS 3	—
PD[14]	PAD[62]	52	81	IO	Timer 2 - ch. 3	DSPI 2 - Serial Data	Timer 3 - ch. 3	—
PD[15]	PAD[63]	53	82	IO	Timer 2 - ch. 4	DSPI 2 - Serial Data	Timer 3 - ch. 4	—
PE[0]	PAD[64]	—	83	IO	Timer 3 - ch. 3	Ext. INT 2	—	Timer 2 - ch. 4
PE[1]	PAD[65]	—	84	IO	Timer 3 - ch. 4	—	—	Timer 2 - ch. 5
—	VDD_HV_IO	54	85	PWB85	—			
PE[2]	PAD[66]	55	86	IO	Timer 2 - ch. 5	DSPI 2 - CS 0	DSPI 0 - CS 3	—
PE[3]	PAD[67]	56	87	IO	Nexus MSEO(2)	—	DSPI 0 - CS 4	DSPI 2 - CLK
PE[4]	PAD[68]	—	88	IO	Timer 3 - ch. 5	DSPI 2 - CS 2	Timer 2 - ch. 4	—
PE[5]	PAD[69]	57	89	IO	Nexus MDO 3(2)	—	CLOCKOUT	DSPI 2 - Serial Data
PE[6]	PAD[70]	58	90	IO	Nexus MDO 2(2)	—	DSPI 0 - CS 6	DSPI 2 - Serial Data
PE[7]	PAD[71]	59	91	IO	Nexus MDO 1(2)	—	DSPI 0 - CS 7	Timer 3 - ch. 4
PE[8]	PAD[72]	60	92	IO	Nexus MDO 0(2)	DSPI 0 - CS 0	Ext. INT 3	Timer 3 - ch. 5
PE[9]	PAD[73]	—	93	IO	—	Timer 3 - ch. 2	Ext. INT 4	DSPI 2 - CS 1
PE[10]	PAD[74]	—	94	IO	—	Timer 3 - ch. 3	DSPI 0 - CS 5	DSPI 2 - CS 2
—	VDD_HV_IO	61	95	PW	—			

4.6 Operating conditions

Table 9. Device operating conditions(1)

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Frequency							
f_{SYS}	SR		Device operating frequency(2)	-40 °C < T_J < 150 °C	—	—	80	MHz
Temperature							
T_J	SR	P	Operating temperature range - junction	—	-40.0	—	150.0	°C
T_A (T_L to T_H)	SR	P	Ambient operating temperature range	—	-40.0	—	125.0	°C
Voltage							
$V_{DD\_HV\_IO}$	SR	P	I/O supply voltage	LVD290/HVD400 enabled	2.97	—	3.63	V
		C		LVD290 enabled HVD400 disabled (3),(4)	2.97	—	5.5	
$V_{DD\_HV\_OSC\_PMC}$	SR	P	PMC and OSC supply voltage	LVD290/HVD400 enabled	2.97	—	3.63	V
		C		LVD290 enabled HVD400 disabled	2.97	—	5.5	
$V_{DD\_HV\_ADC\_TSENS}$	SR	D	SAR ADC supply voltage	LVD400 enabled	4.5	—	5.5	V
		C		LVD400 disabled(3),(5)	3.0	—	3.6	
V_{REFH_ADC}	SR	P	SAR ADC reference voltage	—	2.0	—	$V_{DD\_HV\_ADC\_TSENS}$	V
V_{REFH_ADC} - $V_{DD\_HV\_ADC\_TSENS}$	SR	D	SAR ADC reference differential voltage	—	—	—	25	mV
V_{RAMP}	SR	D	Slew rate on power supply pins	—	—	—	0.5	V/µs
V_{IN}	SR	C	I/O input voltage range	—	0	—	5.5	V
Injection current								
I_{IC}	SR	T	DC injection current (per pin)(6),(7),(8)	Digital pins and analog pins	-3	—	3	mA
I_{MAXSEG}	SR	D	Maximum current per power segment(9)	—	-80	—	80	mA

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2: $T_J = T_B + (R_{qJB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

R_{qJB} = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Table 13. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ILCMOS}(2)	SR	P	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
$V_{HYSCMOS}$	—	C	Input hysteresis CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
Automotive								
V_{IH}(3)	SR	P	Input high level Automotive	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.75 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	
V_{IL}	SR	P	Input low level Automotive	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	2.2	V
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	-0.3	—	0.35 * $V_{DD\_HV\_IO}$	
V_{HYST}	—	C	Input hysteresis Automotive	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.5	—	—	V
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.11 * $V_{DD\_HV\_IO}$	—	—	
Input Characteristics								
I_{LKG}	CC	P	Digital input leakage	—	—	—	1	µA
C_{IN}	C	D	Digital input capacitance	—	—	—	10	pF

1. Minimum hysteresis at 4.0 V
2. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V.
3. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V.

Table 14 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 14. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up/down current absolute value(1)	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	23	—	—	µA
				V_{IN} = 0.49 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	82	
				V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	
	CC	T		V_{IN} = 0.75 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	10	—	—	
				V_{IN} = 0.35 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	70	
				V_{IN} > V_{IL} = 1.1 V (TTL) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	75	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	µA
				V_{IN} = 0.49 * $V_{DD\_HV\_IO}$ 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	—	
				V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	16	—	—	
	CC	T		V_{IN} = 0.75 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	92	
				V_{IN} = 0.35 * $V_{DD\_HV\_IO}$ 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	19	—	—	
				V_{IN} > V_{IL} = 1.1 V (TTL) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	16	—	—	

1. Weak pull-up/down is enabled within t_{WK_PU} = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.

4.9.3 I/O output DC characteristics

Table 15: Weak configuration I/O output characteristics, provide DC characteristics for bidirectional pads in the following configurations:

- Weak
- Medium
- Strong
- Very Strong

Table 17. Strong configuration I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{TR_S}	CC	D	Transition time output pin strong configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 25 pF	—	—	11	ns
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 50 pF	—	—	22	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 25 pF	—	—	8	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 50 pF	—	—	13	
t_{SKEW_S}	CC	T	Difference between rise time and fall time	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	40	%
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	28	

Table 18. Very Strong configuration I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
R_{OH_V}	CC	P	PMOS output impedance very strong configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, I_{OH} < 7 mA	—	—	85	Ω
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	—	—	65	
R_{OL_V}	CC	P	NMOS output impedance very strong configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, I_{OL} < 7 mA	—	—	85	Ω
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	—	—	65	
f_{max_V}	CC	T	Output frequency very strong configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 15 pF	—	—	50	MHz
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 25 pF	—	—	30	
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V T_d = 0.6 ns, load = 10 pF	—	—	25	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 25 pF	—	—	50	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 50 pF	—	—	25	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V T_d = 1 ns, load = 10 pF	—	—	25	

Figure 6 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ does not go low enough: it is filtered by input buffer hysteresis. The device remains in the current state.
2. $\overline{\text{PORST}}$ goes low enough, but not for long enough: it is filtered by a low pass filter. The device remains in the current state.
3. The $\overline{\text{PORST}}$ generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown. It may either be reset or remains in current state depending on extra conditions (PVT — process, voltage, temperature).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. The device is under hardware reset.

Figure 6. Noise filtering on reset signal

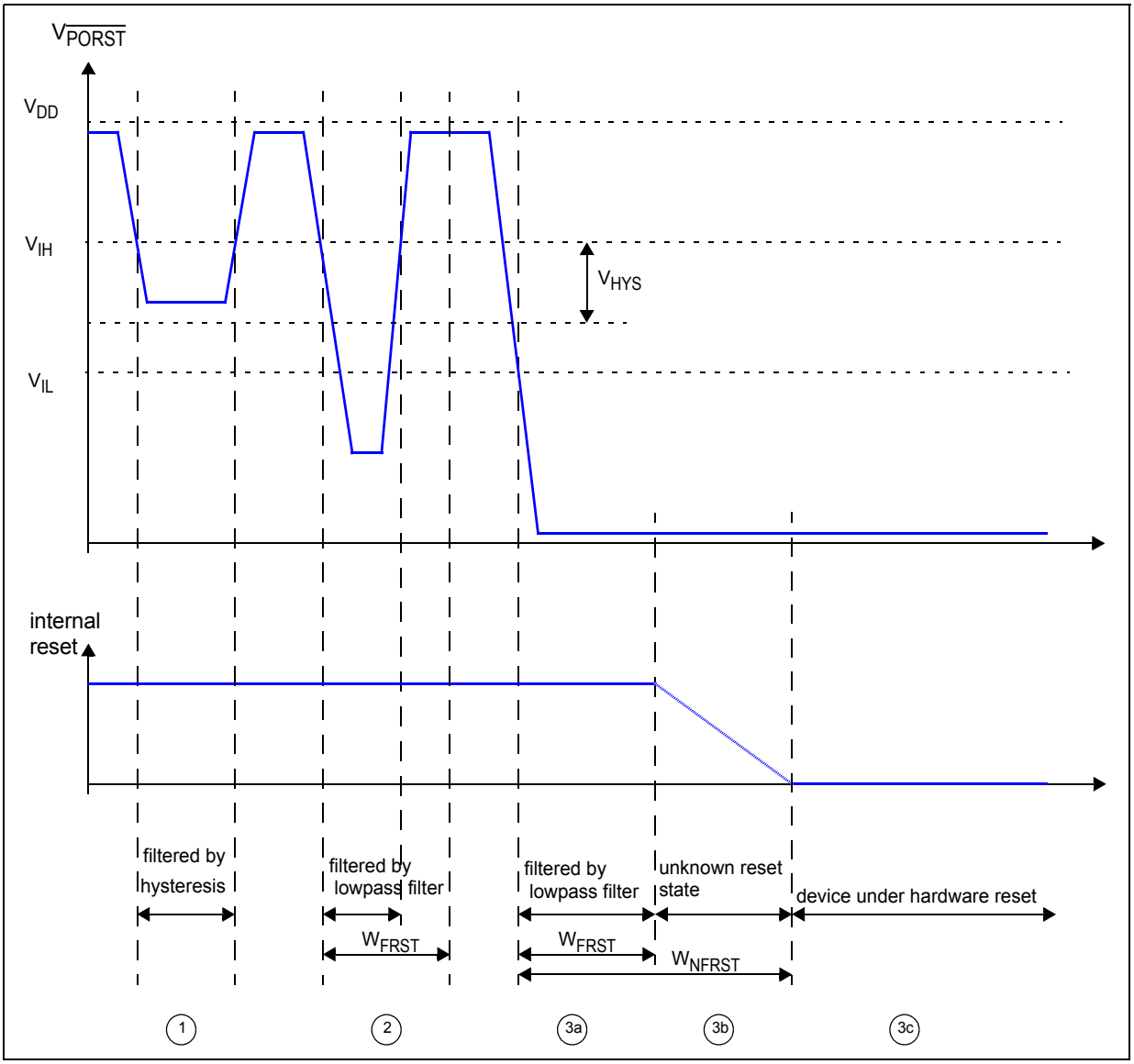


Table 24. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1]	Value									Unit
		Typ [2]	C	Initial max			Typical end of life[3]	Lifetime max[4]		C	
				25 °C [5]	All temp [6]	C		≤ 1 K cycles	≤ 100 K cycles		
t_{AIC0P}	Array Integrity Check (0.5 MB, proprietary)[11]	0.75	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (0.5 MB, sequential)	25	T	—	—	—	—	—	—	—	ms
$t_{MR128KS}$	Margin Read (128 KB, sequential)	6.26	T	—	—	—	—	—	—	—	ms
t_{AABT}	Array Integrity Check Abort Latency	—	—	—	—	—	—	10		—	µs
t_{MABT}	Margin Read Abort Latency	—	—	—	—	—	—	10		—	µs

1. Actual hardware programming times; this does not include software overhead.
2. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
3. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
4. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
5. Initial factory condition: < 100 program/erase cycles, 20 °C < T_J < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
6. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, -40 °C < T_J < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Rate computed based on 128K sectors.
8. Only code sectors, not including EEPROM.
9. Time between erase suspend resume and next erase suspend.
10. Timings guaranteed by design.
11. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at 80 MHz.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 25. Flash memory Life Specification

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles

Table 25. Flash memory Life Specification (continued)

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
$N_{CER128K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
N_{DER16K}	16 KB EEPROM Flash endurance	100	—		—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—		—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	15	—		—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—		—	Years

1. Program and erase cycles supported across specified temperature specs.

4.15 PLL0/PLL1 electrical characteristics

The device provides a phase-locked loop (PLL0) as well as a frequency-modulated phase-locked loop (PLL1) module to generate a fast system clock from the main oscillator driver.

Table 26. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL1 reference clock[2]	—	37.5	—	78.125	MHz
Δ_{PLLIN}	SR	—	PLL1 reference clock duty cycle[2]	—	35	—	65	%
f_{PLLOUT}	CC	D	PLL1 output clock frequency	—	4.762	—	625	MHz
f_{VCO}[3]	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL1 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	110	µs
Δt_{STJIT}	CC	T	PLL1 short term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	—	—	1.8	ns
I_{PLL}	CC	C	PLL1 consumption	T_A = 25 °C	—	—	6	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ±2%.

Table 27. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL0 reference clock[2]	—	8	—	56	MHz
Δ_{PLLIN}	SR	—	PLL0 reference clock duty cycle[2]	—	30	—	70	%
f_{PLLOUT}	CC	D	PLL0 output clock frequency	—	4.762	—	625	MHz
f_{VCO}	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL0 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	110	µs
Δt_{STJIT}	CC	T	PLL0 short term jitter	f_{sys} maximum	—	—	300	ps
Δt_{LTJIT}	CC	T	PLL0 long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	-1	—	1	ns
I_{PLL}	CC	C	PLL0 consumption	T_A = 25 °C	—	—	5.5	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, TA = -40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

4.16 External oscillator (XOSC) electrical characteristics

Table 28. External Oscillator electrical specifications[1]

Symbol		C	Parameter	Conditions		Value		Unit
						Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range[2]	—		4	8	MHz
				—		>8	20	
				—		>20	40	
t_{cst}	CC	T	[Covers: ADD12.017]Crystal start-up time [3],[4]	T_J = 150 °C		—	5	ms
trec	CC	—	Crystal recovery time[5]	—		—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO}$		V_{REF} + 0.6	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage[6],[7]	V_{REF} = 0.28 * $V_{DD\_HV\_IO}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	CC	T	Total on-chip stray capacitance on EXTAL pin[8]	QFP		6.0	8.0	pF
C_{S_XTAL}	CC	T	Total on-chip stray capacitance on XTAL pin[8]	QFP		6.0	8.0	pF
g_m	CC	P	Oscillator Transconductance (5 V)	T_J = -40 °C to 150 °C	$f_{XTAL} \leq 8$ MHz	2.6	11.0	mA/V
		C			$f_{XTAL} \leq 20$ MHz	7.9	26.0	
		C			$f_{XTAL} \leq 40$ MHz	10.4	34.0	

4.18 ADC electrical characteristics

4.18.1 Introduction

The device provides a 12-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 10. ADC characteristic and error definitions

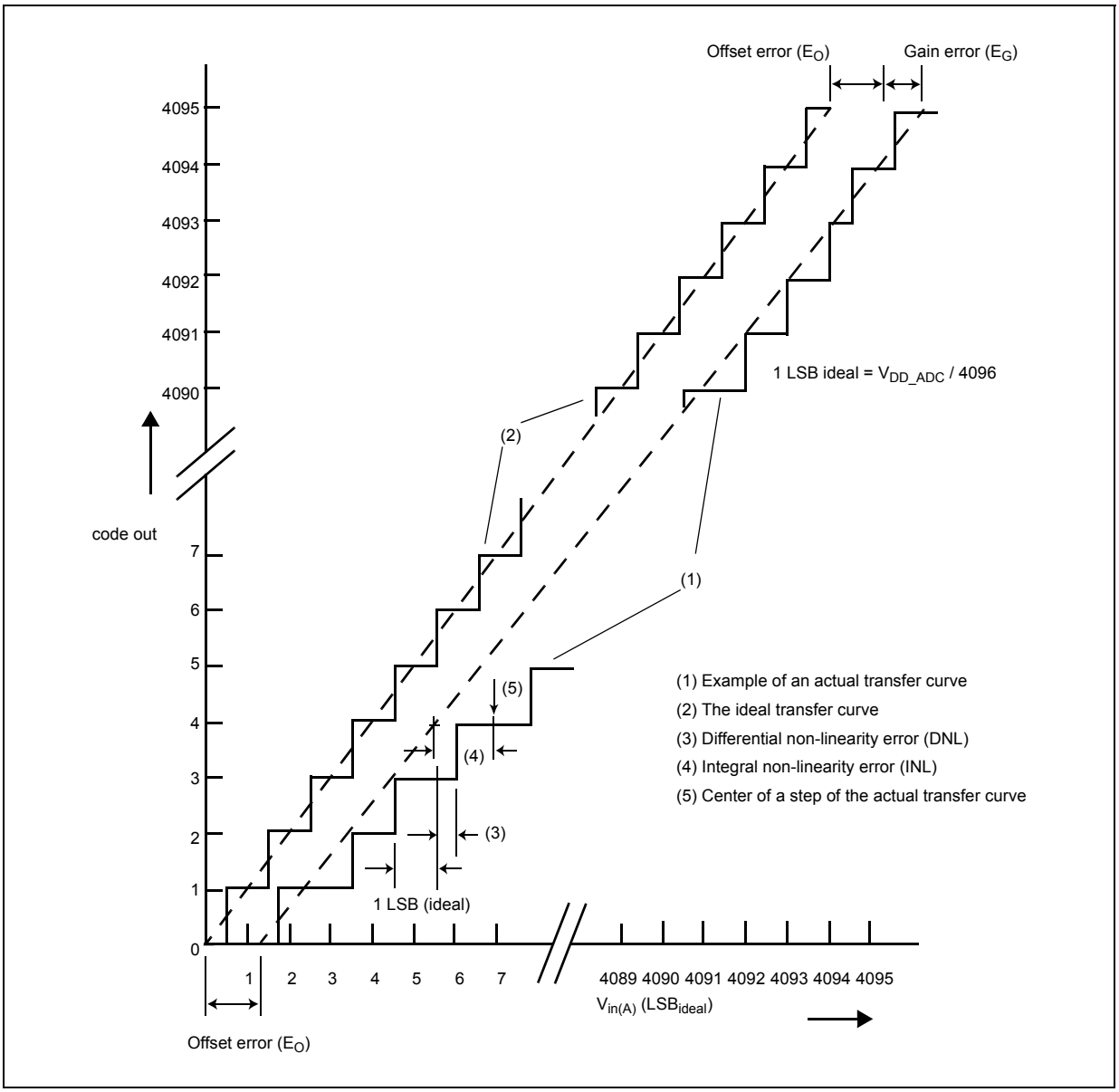


Table 35. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	53	—	ns
4	t_{SDC}	CC	D	SCK duty cycle[4]	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[5]	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[5]	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK[6]	SCK drive strength				
					Very strong	25 pF	32	—	ns
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK[6]	SCK drive strength				
					Very strong	0 pF	0	—	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK[7]	SOUT and SCK drive strength				
					Very strong	25 pF	—	5	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK[7]	SOUT and SCK drive strength				
					Very strong	25 pF	2	—	ns

1. Protocol clock is 40 MHz and all pads are configured as very strong.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. PCSx and PCSS using same pad configuration.
6. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 18. DSPI CMOS master mode – modified timing, CPHA = 1

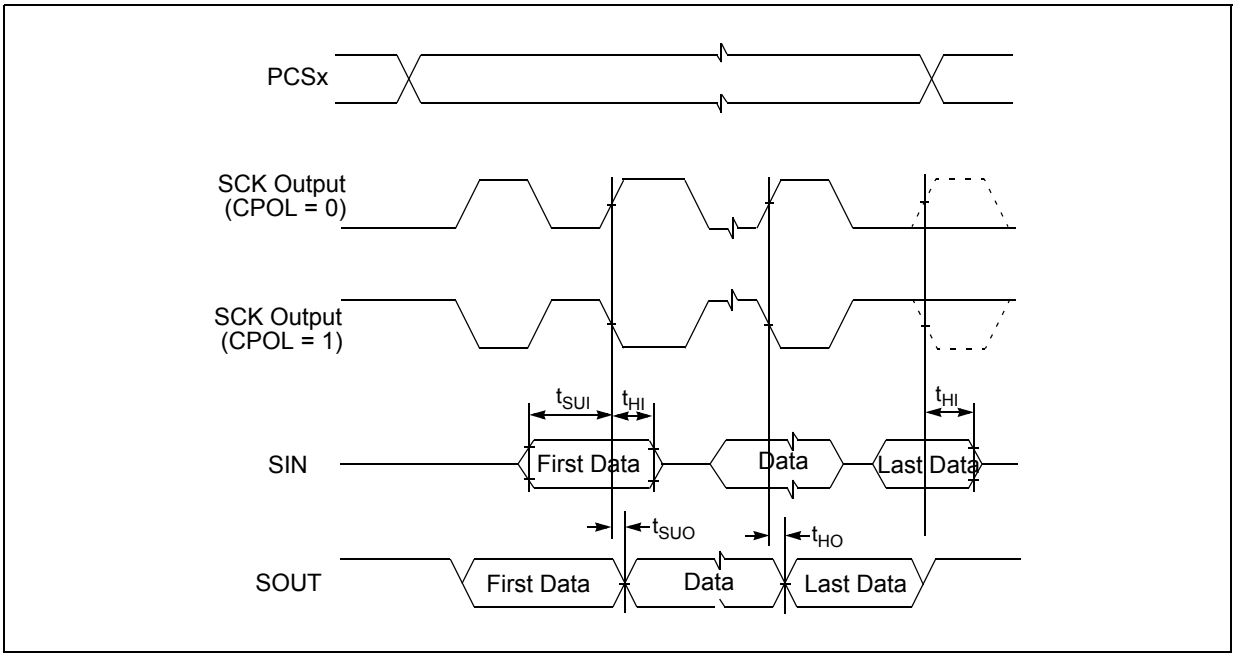


Figure 19. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)