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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z0h |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, LINbus, SPI, UART/USART |
| Peripherals | DMA, POR, WDT |
| Number of I/O | - |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 125°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP Exposed Pad |
| Supplier Device Package | 64-eTQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/spc570s50e1cefar |

# Contents

# 1 Introduction

## 1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

## 1.2 Description

The SPC570Sx is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC570Sx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of Chassis and Safety electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 80 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

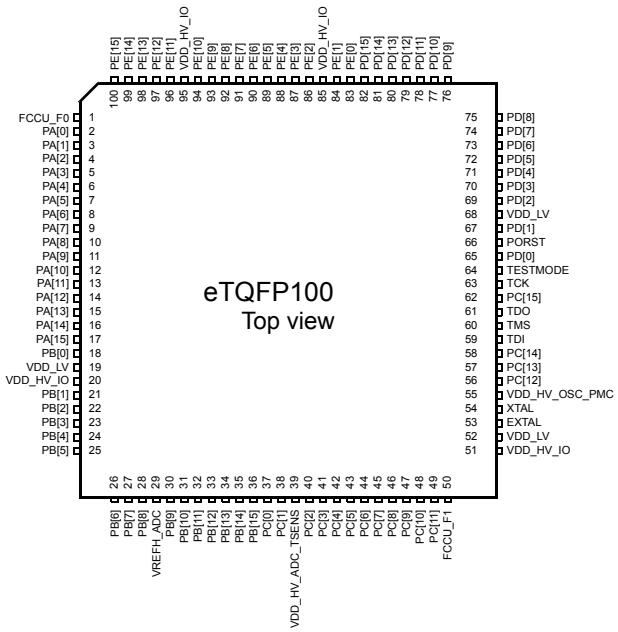
**Table 1. SPC570Sx device feature summary (Family Superset Configuration)**

| Feature | | Description |
|---|---|---|
| Process | | 55 nm |
| Main processor | Core | e200z0h |
| | Number of main cores | 1 |
| | Number of checker cores | 1 |
| | VLE | Yes |
| | Main processor frequency | 80 MHz(1) |
| Interrupt controllers (including interrupt controller checker) | | 1 |
| Software watchdog timer | | 1 |
| System timers | | 1 AUTOSAR® STM<br>1 PIT with four 32-bit channels |
| DMA (including DMA checker) | | 1 |
| DMA channels | | 16 |
| SMPU | | Yes (8 regions)(2) |
| System SRAM | | 48 KB |
| Code flash memory | | 512 KB |
| Data flash memory (suitable for EEPROM emulation) | | 32 KB |

**Table 3. SPC570Sx series block summary (continued)**

| Block | Function |
|---|---|
| Clock generation module (MC_CGM) | Provides logic and control required for the generation of system and peripheral clocks |
| Mode entry module (MC_ME) | Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications |
| MC_PMC | Contains registers that enable/disable the various voltage monitors |
| Reset generation module (MC_RGM) | Centralizes reset sources and manages the device reset sequence of the device |
| Memory protection unit (MPU) | Provides hardware access control for all memory references generated in a device |
| eTimer | Has six 16-bit general purpose counter, where each counter can be used as input capture or output compare function |
| FCCU | Collects fault event notification from the rest of the system and translates them into internal and/or external system reactions |
| RCCU | Compares input signals and issues an alarm in the case of a mismatch |
| MEMU | Collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory |
| XBIC | Verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected |
| STCU2 | Handles the BIST procedure |
| CRC | Controls the computation of CRC, off-loading this work from the CPU |
| RegProt | Protects several registers against accidental writing, locking their value till the next reset phase |
| Temperature sensor | Monitors the device temperature |
| Debug Control Interface | Provides debug features for the MCU |
| Nexus Port Controller | Monitor a variety of signals including addresses, data, control signals, status signals, etc. |
| Nexus Multimaster Trace Client | Monitors the system bus and provides real-time trace information to debug or development tools |
| Periodic interrupt timer (PIT) | Produces periodic interrupts and triggers |
| System integration unit (SIUL) | Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration |
| System status configuration module (SSCM) | Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable |
| System timer module (STM) | Provides a set of output compare events to support AUTOSAR and operating system tasks |
| System watchdog timer (SWT) | Provides protection from runaway code |

**Figure 3. eTQFP 100-pin configuration**




Note:
Availability of port pin alternate functions depends on product selection.

**Table 4. eTQFP64 and eTQFP100 pinout (continued)**

| Port pin | Pad | Pin No. | | Type | Alternate functions | | | |
|---|---|---|---|---|---|---|---|---|
| | | eTQFP64 | eTQFP100 | | AF1 | AF2 | AF3 | AF4 |
| PE[11] | PAD[75] | 62 | 96 | IO | Nexus MCK0(2) | DSPI 0 - CLK | DSPI 0 - CS 1 | DSPI 1 - CS 3 |
| PE[12] | PAD[76] | — | 97 | IO | — | Timer 3 - ch. 4 | DSPI 2 - CS 0 | DSPI 1 - CS 2 |
| PE[13] | PAD[77] | — | 98 | IO | — | Timer 3 - ch. 5 | DSPI 2 - CS 1 | DSPI 1 - CS 1 |
| PE[14] | PAD[78] | 63 | 99 | IO | Nexus EVTO (2) | DSPI 0 - Serial Data | DSPI 0 - CS 2 | DSPI 2 - CS 3 |
| PE[15] | PAD[79] | 64 | 100 | IO | Nexus EVTI(2) | DSPI 0 - Serial Data | DSPI 1 - CS 3 | — |

1. Cannot be changed
2. Can be enabled via JTAG during the reset phase

2. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, $T_J$ = 150 °C remaining time at or below 5.5 V.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
4. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
5. Solder profile per IPC/JEDEC J-STD-020D
6. Moisture sensitivity per JEDEC test method A112

## 4.4 Electromagnetic compatibility (EMC)

*Table 7* describes the EMC characteristics of the device.

**Table 7. Radiated emissions testing specification(1),(2)**

| Coupling structure | Test setup | Function | Functional configuration | BISS radiated emissions limit |
|---|---|---|---|---|
| Entire IC | (G) TEM | Reference test | C1-S3 | 18 dBµV |
| | | Reference test with SSCG | C1-S3 | 18 dBµV |
| | | Memory copy | C4-S2 | 18 dBµV |
| | | Memory copy with SSCG | C4-S2 | 18 dBµV |

1. Reference “BISS Generic IC EMC Test Specification”, version 1.2, section 9.3, “Emission test configuration for ICs with CPU”.
2. The EMC parameters are classified as "T", validated on testbench.

## 4.5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

**Table 8. ESD ratings(1),(2)**

| Parameter | C | Conditions | Value | Unit |
|---|---|---|---|---|
| ESD for Human Body Model (HBM)(3) | T | All pins | 2000 | V |
| ESD for field induced Charged Device Model (CDM)(4) | T | All pins | 500 | V |

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

## 4.6 Operating conditions

**Table 9. Device operating conditions(1)**

| Symbol | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Frequency | | | | | | | |
| $f_{SYS}$ | SR | | Device operating frequency(2) | -40 °C < $T_J$ < 150 °C | — | — | 80 | MHz |
| Temperature | | | | | | | |
| $T_J$ | SR | P | Operating temperature range - junction | — | -40.0 | — | 150.0 | °C |
| $T_A$ ($T_L$ to $T_H$) | SR | P | Ambient operating temperature range | — | -40.0 | — | 125.0 | °C |
| Voltage | | | | | | | |
| $V_{DD\_HV\_IO}$ | SR | P | I/O supply voltage | LVD290/HVD400 enabled | 2.97 | — | 3.63 | V |
| | | C | | LVD290 enabled HVD400 disabled (3),(4) | 2.97 | — | 5.5 | |
| $V_{DD\_HV\_OSC\_PMC}$ | SR | P | PMC and OSC supply voltage | LVD290/HVD400 enabled | 2.97 | — | 3.63 | V |
| | | C | | LVD290 enabled HVD400 disabled | 2.97 | — | 5.5 | |
| $V_{DD\_HV\_ADC\_TSENS}$ | SR | D | SAR ADC supply voltage | LVD400 enabled | 4.5 | — | 5.5 | V |
| | | C | | LVD400 disabled(3),(5) | 3.0 | — | 3.6 | |
| $V_{REFH\_ADC}$ | SR | P | SAR ADC reference voltage | — | 2.0 | — | $V_{DD\_HV\_ADC\_TSENS}$ | V |
| $V_{REFH\_ADC}$ - $V_{DD\_HV\_ADC\_TSENS}$ | SR | D | SAR ADC reference differential voltage | — | — | — | 25 | mV |
| $V_{RAMP}$ | SR | D | Slew rate on power supply pins | — | — | — | 0.5 | V/µs |
| $V_{IN}$ | SR | C | I/O input voltage range | — | 0 | — | 5.5 | V |
| Injection current | | | | | | | | |
| $I_{IC}$ | SR | T | DC injection current (per pin)(6),(7),(8) | Digital pins and analog pins | -3 | — | 3 | mA |
| $I_{MAXSEG}$ | SR | D | Maximum current per power segment(9) | — | -80 | — | 80 | mA |

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *SPC570Sx Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. Maximum voltage is not permitted for entire product life. See *Absolute maximum ratings*.
4. Reduced output/input capabilities below 4.2 V. See performance derating values in *I/O pad electrical characteristics*
5. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
6. Full device lifetime without performance degradation
7. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Table 6: Absolute maximum ratings* for maximum input current for reliability requirements.
8. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature. For more information, see the device characterization report.
9. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

# 4.7 Thermal characteristics

## 4.7.1 Package thermal characteristics

**Table 10. Thermal characteristics for eTQFP64**

| Symbol | | C | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | D | Junction to ambient, natural convection(1) | Four layer board - 2s2p board | 32.3 | °C/W |
| $R_{\theta JMA}$ | CC | D | Junction to ambient in forced air @ 200 ft/min (1 m/s)(1) | Four layer board - 2s2p board | 26.5 | °C/W |
| $R_{\theta JB}$ | CC | D | Junction to board(2) | — | 12.1 | °C/W |
| $R_{\theta JCtop}$ | CC | D | Junction to top case(3) | — | 19.0 | °C/W |
| $R_{\theta JCbotttom}$ | CC | D | Junction to bottom case thermal resistance(4) | — | 1.9 | °C/W |
| $\Psi_{JT}$ | CC | D | Junction to package top, natural convection(5) | — | 0.6 | °C/W |

1. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
2. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1021.1).
4. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

## 4.7.2 Power considerations

An estimation of the chip junction temperature, $T_J$ can be obtained from the equation:

**Equation 1: $T_J = T_A + (R_{\theta JA} * P_D)$**

where:

$T_B$ = thermocouple temperature on bottom of the package (°C)

$\Psi_{JPB}$ = thermal characterization parameter (°C/W)

$P_D$ = power dissipation in the package (W)

## 4.8 Current consumption

The following table describes the consumption figures.

**Table 11. Current consumption**

| Symbol | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| IDD | P | Operating current all supply rails | $F_{max}$(1) | — | — | 110(1) | mA |
| | T | | $T_j$ = 150 °C(1) | — | — | 0.75 * $f_{CPU}$(2) + 50 | mA |
| Stop | P | Stop mode consumption | Device working on RC clock | — | — | 40(3) | mA |

1. Values are based on typical application code executing from Flash memory, where the DMA is running in continuous mode, the ADC is in continuous conversion, the timers are running to maximum counter values and communication IPs are in loopback or transmitting mode. IOs are unloaded.
The maximum consumption can reach 110 mA during boot time M/LBIST (before reset).
2. $f_{CPU}$ is measured in MHz
3. ADC and XOSC disabled, Includes regulator consumption for VDD_LV generation. Includes static I/O current with no pins toggling.

## 4.9 I/O pad electrical characteristics

### 4.9.1 I/O pad types

*Table 12* describes the different pad type configurations.

**Table 12. I/O pad specification descriptions**

| Pad type | Description |
|---|---|
| Weak configuration | Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω |
| Medium configuration | Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω |
| Strong configuration | Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω |
| Very strong configuration | Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interfaces requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω |
| Input only pads | These pads are associated to ADC channels and the external 8-40 MHz crystal oscillator (XOSC) providing low input leakage |

**Table 16. Medium configuration I/O output characteristics(1),(2) (continued)**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{TR\_M}$ | CC | D | Transition time output pin medium configuration | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V $C_L$ = 25 pF | — | — | 37 | ns |
| | | | | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V $C_L$ = 50 pF | — | — | 72 | |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V $C_L$ = 25 pF | — | — | 25 | |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V $C_L$ = 50 pF | — | — | 50 | |
| $t_{SKEW\_M}$ | CC | T | Difference between rise time and fall time | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V | — | — | 40 | % |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V | — | — | 28 | |

1. The above mentioned values are different for M/W (Medium/Weak) pads.
2. Please refer to *Table 19: I/O output characteristics for pads 4, 9, 11, 55, 56*

**Table 17. Strong configuration I/O output characteristics**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $R_{OH\_S}$ | CC | P | PMOS output impedance strong configuration | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, $I_{OH}$< 6 mA | — | — | 90 | Ω |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, $I_{OH}$ < 8 mA | — | — | 75 | |
| $R_{OL\_S}$ | CC | P | NMOS output impedance strong configuration | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, $I_{OL}$< 6 mA | — | — | 90 | Ω |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, $I_{OL}$ < 8 mA | — | — | 75 | |
| $f_{max\_S}$ | CC | T | Output frequency strong configuration | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V $C_L$ = 25 pF | — | — | 25 | MHz |
| | | | | 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V $C_L$ = 50 pF | — | — | 12.5 | |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V $C_L$ = 25 pF | — | — | 50 | |
| | | | | 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V $C_L$ = 50 pF | — | — | 25 | |

**Table 21. Voltage regulator electrical characteristics (continued)**

| Symbol | | Parameter | Conditions[1] | Value[2] | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $C_{V1V2}$ | SR | EMC cap to be placed on every 1.2V pin | $V_{DD\_LV}/V_{SS}$ pair | 50 | 100 | 135 | nF |
| $C_{DECBV}$ | SR | Decoupling capacitance ballast | $V_{DD\_HV\_IO}/V_{SS\_LV}$ pair | 1.1 | 2.2[4] | 3 | µF |

1. $V_{DD}$ = 5.0 V ± 10%, $T_A$ = -40 / 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Recommended X7R or X5R ceramic -43% / +35% variation, 20% tolerance and 12.5% temperature.
4. Recommended X7R or X5R ceramic -43% / +35% variation, 20% tolerance and 12.5% temperature.

## 4.12 PMU monitor specifications

### 4.12.1 Nomenclature

- **POR** stands for Power On Reset. The POR circuit manages the reset from very low voltage up to its threshold. Cannot be disabled.
- **MVD** stands for Minimum Voltage Detector. It cannot be disabled by the user and generate a destructive Reset.
- **LVD** stands for Low Voltage Detector. It can be disabled by the user.
- **HVD** stands for High Voltage Detector. It can be disabled by the user.
- **UVD** stands for Upper Voltage Detector. It cannot be disabled by the user and generate a destructive reset.

**Table 22. Trimmed (PVT) values**

| Domain monitor | Voltage | Name | Segment | Lower limit | Upper limit |
|---|---|---|---|---|---|
| 1.2 V | Power On Reset | POR041 | Core | 0.39 V | 0.95 V |
| | Low | MVD098 | Core | 1.005 V | 1.055 V |
| | | | Flash | 1.005 V | 1.055 V |
| | | LVD108 | Core | 1.085 V | 1.137 V |
| | High | HVD140 | Core | 1.340 V | 1.400 V |
| | | UVD145 | Core | 1.379 V | 1.441 V |
| | | | Flash | 1.379 V | 1.441 V |
| 3.3 V | Power On Reset | POR200 | Core | 1.750 V | 2.400 V |
| | Low | MVD270 | Core | 2.694 V | 2.826 V |
| | | | Flash | 2.694 V | 2.826 V |
| | | LVD290 | Core | 2.881 V | 2.999 V |
| | | | Flash | 2.881 V | 2.999 V |
| | | | ADC | 2.881 V | 2.999 V |
| | High | HVD400 | Core | 3.660 V | 3.840 V |

**Table 22. Trimmed (PVT) values (continued)**

| Domain monitor | Voltage | Name | Segment | Lower limit | Upper limit |
|---|---|---|---|---|---|
| 5 V | Low | LVD400 | ADC | 4.128 V | 4.332 V |
| | High | UVD600 | Core | 5.684 V | 5.920 V |

### 4.12.2 Power up/down sequencing

For proper device functioning please adhere to following power sequence:

$V_{DD\_HV\_OSC\_PMC}$ supply should always be greater than or equal to $V_{DD\_HV\_IO}$ supply (even during ramping up).

$V_{DD\_HV\_ADC\_TSENS}$ supply should always be greater than or equal to $V_{REFH\_ADC}$ supply.

## 4.13 Platform Flash controller electrical characteristics

**Table 23. RWSC settings(1)**

| Max Flash operating Frequency (MHz)(2) | RWSC |
|---|---|
| 20 | 0b000 |
| 40 | 0b001 |
| 64 | 0b010 |
| 80 | 0b011 |

1. RWSC is a field in the Flash memory of PFCR register used to specify the wait states for address pipelining and read/write accesses.
2. Maximum frequencies (FM modulation up to 2% could be enabled additionally).

## 4.14 Flash memory electrical characteristics

*Table 24* shows the program and erase characteristics.

**Table 24. Flash memory program and erase specifications**

| Symbol | Characteristics(1) | Value | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ (2) | C | Initial max | | | Typical end of life(3) | Lifetime max(4) | | C | |
| | | | | 25 °C (5) | All temp (6) | C | | ≤ 1 K cycles | ≤ 100 K cycles | | |
| $t_{dwprogram}$ | Double Word (64 bits) program time [Packaged part] | 38 | C | 150 | — | — | 94 | 500 | | C | µs |
| $t_{pprogram}$ | Page (256 bits) program time | 78 | C | 300 | — | — | 214 | 1000 | | C | µs |
| $t_{pprogrameep}$ | Page (256 bits) program time EEPROM (partition 1) [Packaged part] | 90 | C | 330 | — | — | 250 | 1000 | | C | µs |

**Table 24. Flash memory program and erase specifications (continued)**

| Symbol | Characteristics[1] | Value | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ [2] | C | Initial max | | | Typical end of life[3] | Lifetime max[4] | | C | |
| | | | | 25 °C [5] | All temp [6] | C | | ≤ 1 K cycles | ≤ 100 K cycles | | |
| $t_{AIC0P}$ | Array Integrity Check (0.5 MB, proprietary)[11] | 0.75 | T | — | — | — | — | — | — | — | s |
| $t_{MR0S}$ | Margin Read (0.5 MB, sequential) | 25 | T | — | — | — | — | — | — | — | ms |
| $t_{MR128KS}$ | Margin Read (128 KB, sequential) | 6.26 | T | — | — | — | — | — | — | — | ms |
| $t_{AABT}$ | Array Integrity Check Abort Latency | — | — | — | — | — | — | 10 | | — | µs |
| $t_{MABT}$ | Margin Read Abort Latency | — | — | — | — | — | — | 10 | | — | µs |

1. Actual hardware programming times; this does not include software overhead.
2. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
3. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
4. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
5. Initial factory condition: < 100 program/erase cycles, 20 °C < $T_J$ < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
6. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, -40 °C < $T_J$ < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Rate computed based on 128K sectors.
8. Only code sectors, not including EEPROM.
9. Time between erase suspend resume and next erase suspend.
10. Timings guaranteed by design.
11. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at 80 MHz.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

**Table 25. Flash memory Life Specification**

| Symbol | Characteristics[1] | Value | | | | Unit |
|---|---|---|---|---|---|---|
| | | Min | C | Typ | C | |
| $N_{CER16K}$ | 16 KB CODE Flash endurance | 10 | — | 100 | — | Kcycles |
| $N_{CER32K}$ | 32 KB CODE Flash endurance | 10 | — | 100 | — | Kcycles |
| $N_{CER64K}$ | 64 KB CODE Flash endurance | 10 | — | 100 | — | Kcycles |

Figure 11. JTAG test clock input timing

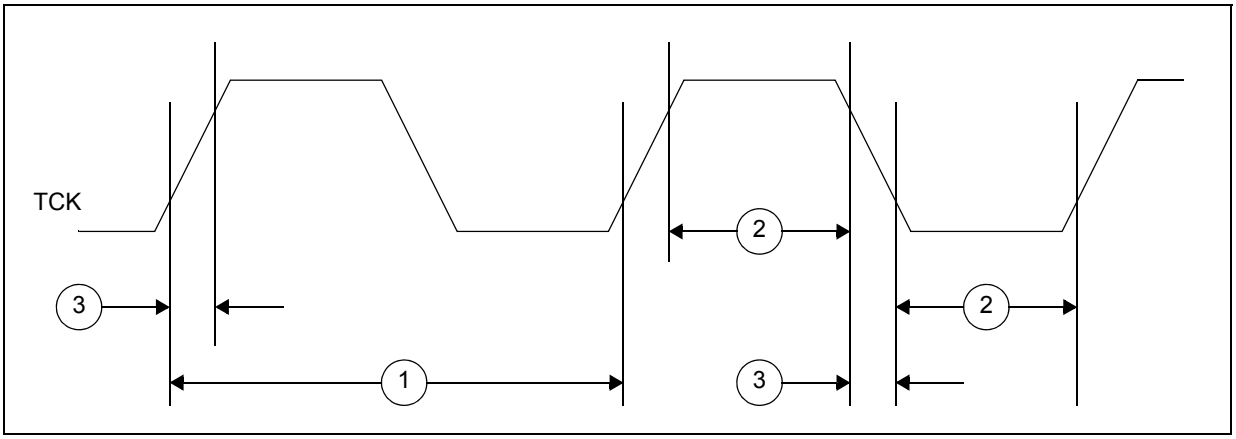



Figure 12. JTAG test access port timing

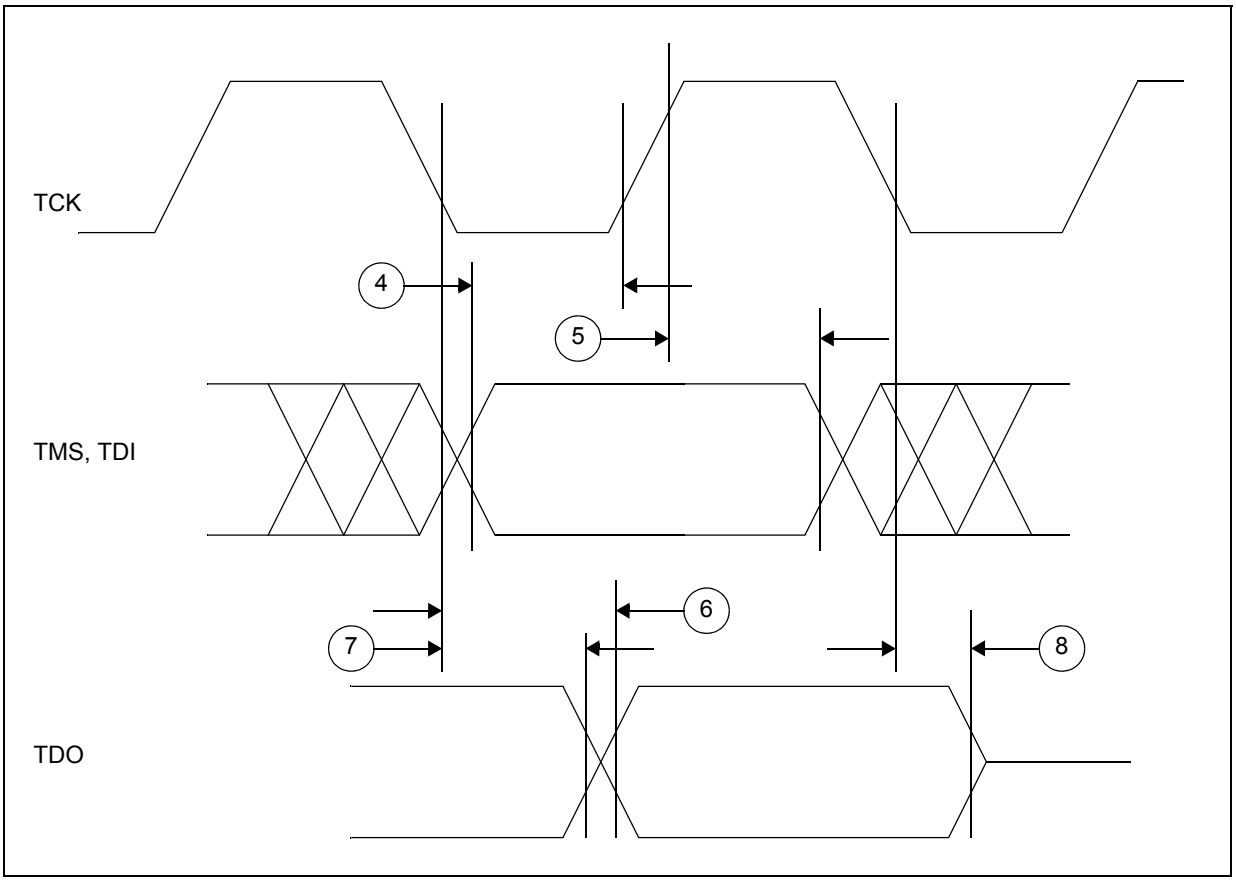
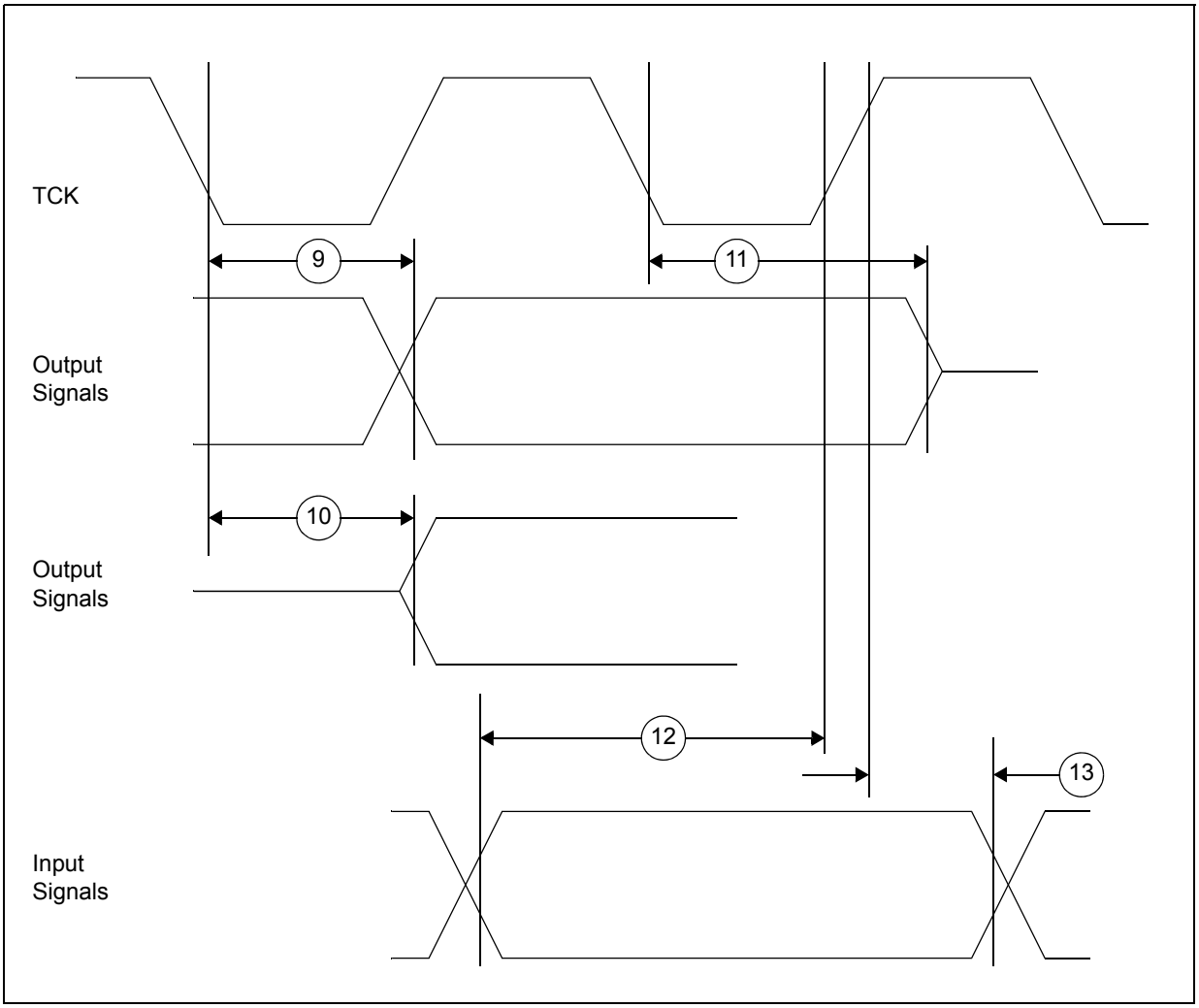


Figure 13. JTAG boundary scan timing




## 4.21 DSPI CMOS master mode timing

### 4.21.1 Classic timing

Table 35. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0[1]

| # | Symbol | | C | Characteristic | Condition | | Value[2] | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Pad drive[3] | Load ($C_L$) | Min | Max | |
| 1 | $t_{SCK}$ | CC | D | SCK cycle time | SCK drive strength | | | | |
| | | | | | Very strong | 25 pF | 75 | — | ns |
| 2 | $t_{CSC}$ | CC | D | PCS to SCK delay | SCK and PCS drive strength | | | | |
| | | | | | Very strong | 25 pF | 50 | — | ns |

**Figure 14. DSPI CMOS master mode – classic timing, CPHA = 0**

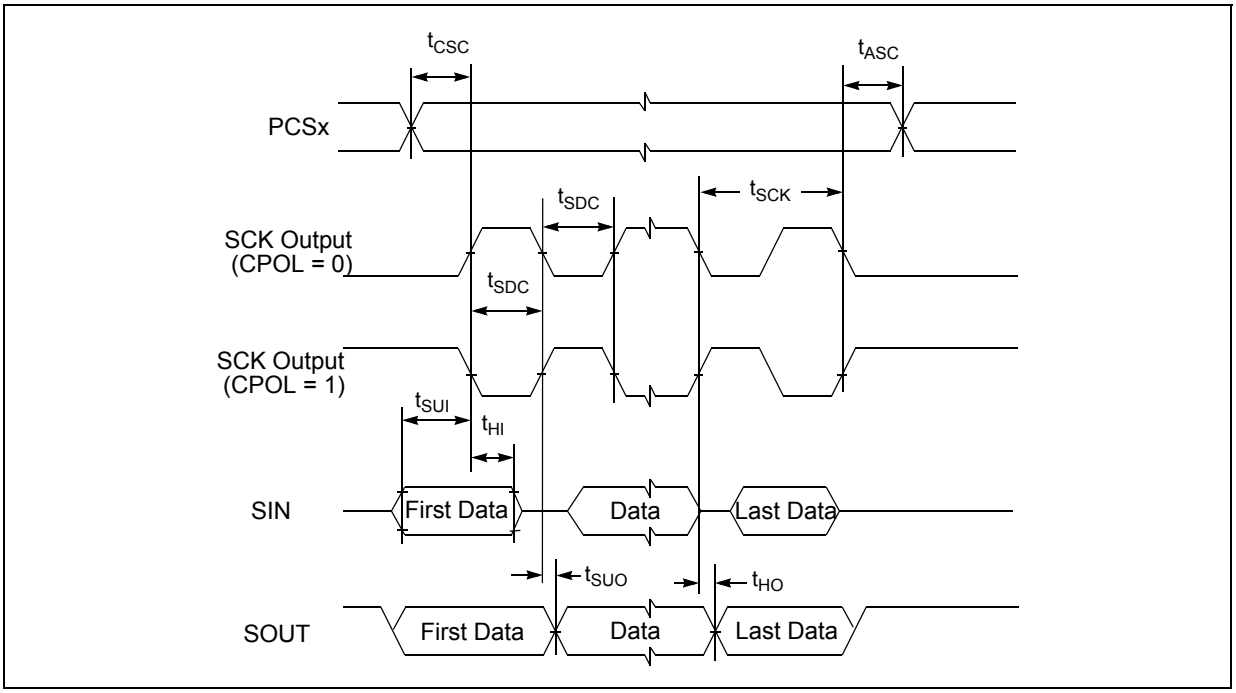



**Figure 15. DSPI CMOS master mode – classic timing, CPHA = 1**

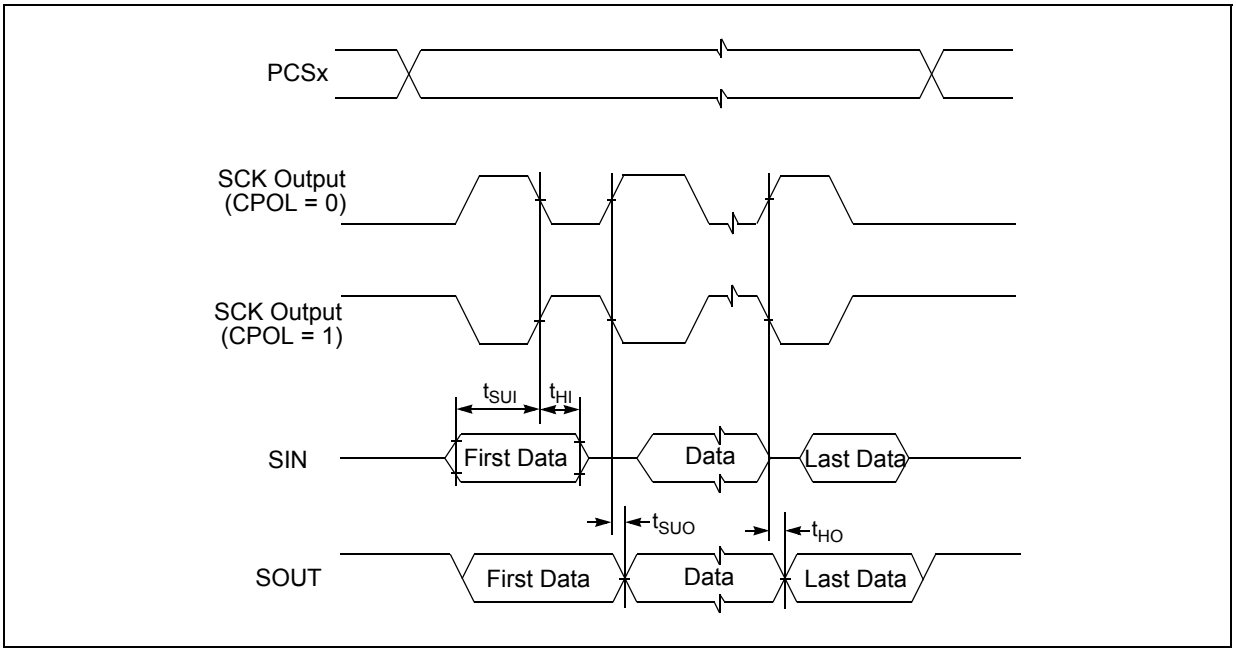


**Figure 18. DSPI CMOS master mode – modified timing, CPHA = 1**

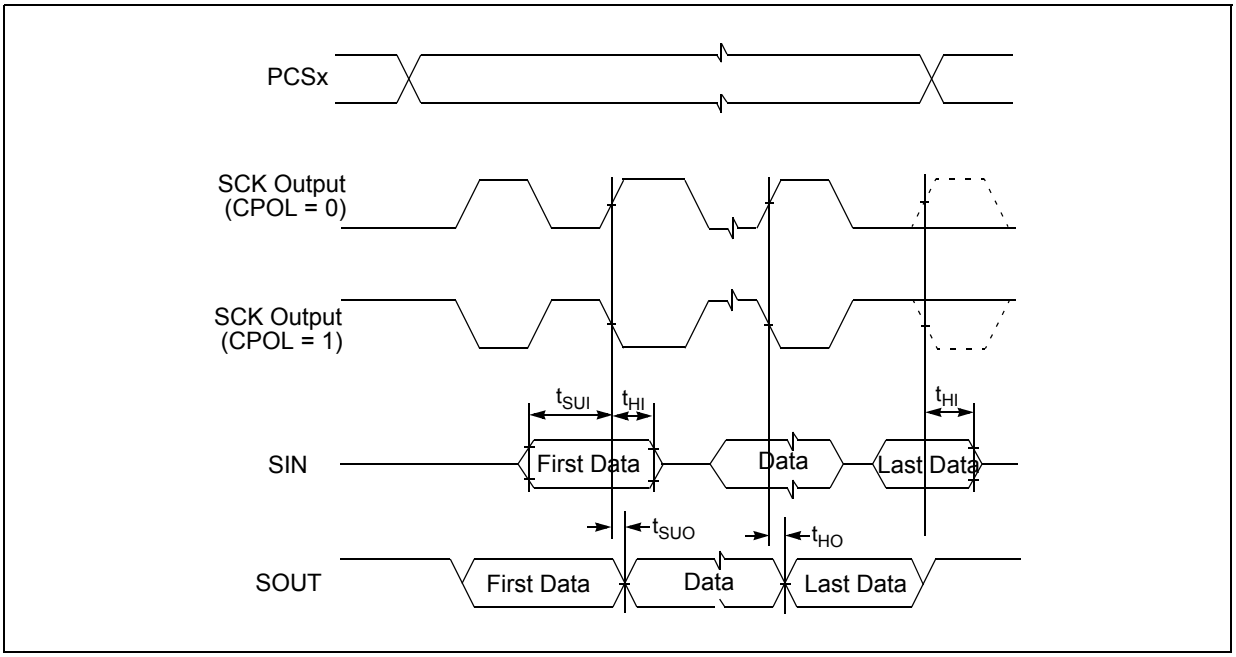



**Figure 19. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)**

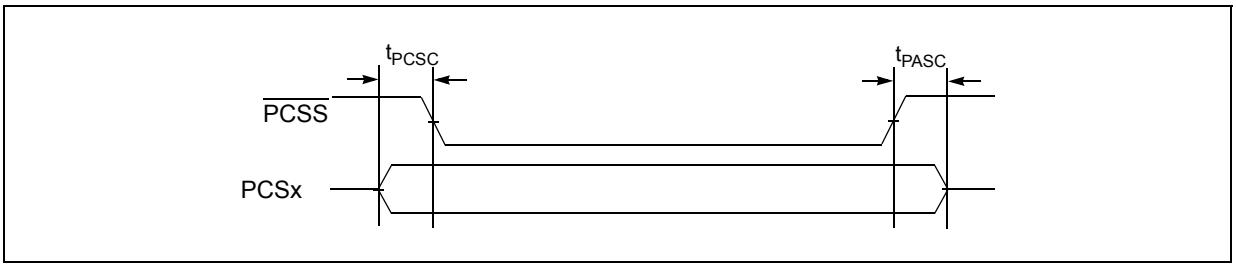


**Table 37. eTQFP64 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches[1] | | |
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | — | — | 1.20 | — | — | 0.0472 |
| A1 | — | 0.05 | 0.15 | — | 0.0020 | 0.0059 |
| A2 | 1.00 | 0.95 | 1.05 | 0.0394 | 0.0374 | 0.0413 |
| b | 0.22 | 0.17 | 0.27 | 0.0087 | 0.0067 | 0.0106 |
| c | — | 0.09 | 0.20 | — | 0.0035 | 0.0079 |
| D | 12.00 | 11.80 | 12.20 | 0.4724 | 0.4646 | 0.4803 |
| D1 | 10.00 | 9.80 | 10.20 | 0.3937 | 0.3858 | 0.4016 |
| D2 | 4.50 | 4.35 | 4.65 | 0.1772 | 0.1713 | 0.1831 |
| D3 | 7.50 | — | — | 0.2953 | — | — |
| E | 12.00 | 11.80 | 12.20 | 0.4724 | 0.4646 | 0.4803 |
| E1 | 10.00 | 9.80 | 10.20 | 0.3937 | 0.3858 | 0.4016 |
| E2 | 4.5 | 4.35 | 4.65 | 0.1772 | 0.1713 | 0.1831 |
| E3 | 7.50 | — | — | 0.2953 | — | — |
| e | 0.50 | — | — | 0.0197 | — | — |
| L | 0.60 | 0.45 | 0.75 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.00 | — | — | 0.0394 | — | — |
| k | 3.5° | 0° | 7° | 3.5° | 0° | 7° |
| ccc | — | — | 0.08 | — | — | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

*Note: TQFP stands for Thin Quad Flat Package.*

## 5.2 eTQFP100 package information

**Figure 21. eTQFP100 package outline**