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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-eTQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc570s50e1cefay

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Table 2. SPC570S40Ex, SPC570S50Ex device configuration differences

	SPC570S40 (full option configuration)	SPC570S50 (full option configuration)
Flash	256 KB(1)	512 KB
RAM	32 KB(2)	48 KB
CAN	1(3)	2
Others	aligned to the *SPC570Sx device feature summary (Family Superset Configuration)* described in *Table 1*	

1. Flash blocks excluded on SPC570S40:
   128K Block 0 [0x0100_0000 … 0x0101_FFFF]
   128K Block 1 [0x0102_0000 … 0x0103_FFFF]
2. SRAM area excluded on SPC570S40
   [0x4000_8000…0x4000_BFFF]
3. FlexCAN1 excluded on SPC570S40

Table 3. SPC570Sx series block summary (continued)

Block	Function
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
MC_PMC	Contains registers that enable/disable the various voltage monitors
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
eTimer	Has six 16-bit general purpose counter, where each counter can be used as input capture or output compare function
FCCU	Collects fault event notification from the rest of the system and translates them into internal and/or external system reactions
RCCU	Compares input signals and issues an alarm in the case of a mismatch
MEMU	Collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory
XBIC	Verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected
STCU2	Handles the BIST procedure
CRC	Controls the computation of CRC, off-loading this work from the CPU
RegProt	Protects several registers against accidental writing, locking their value till the next reset phase
Temperature sensor	Monitors the device temperature
Debug Control Interface	Provides debug features for the MCU
Nexus Port Controller	Monitor a variety of signals including addresses, data, control signals, status signals, etc.
Nexus Multimaster Trace Client	Monitors the system bus and provides real-time trace information to debug or development tools
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
System integration unit (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PB[12]	PAD[28]	—	33	IN/ANA	Timer 2 - ch. 4	ADC ch. 12	Timer 1 - ch. 5	LINFlex 1 - RX
PB[13]	PAD[29]	—	34	IN/ANA	Timer 2 - ch. 5	ADC ch. 11	Timer 3 - ch. 0	NMI
PB[14]	PAD[30]	22	35	IN/ANA	Timer 2 - ch. 0	ADC ch. 2	Timer 3 - ch. 1	Timer 2 - ch. 1
PB[15]	PAD[31]	23	36	IN/ANA	Timer 2 - ch. 1	ADC ch. 1	Timer 3 - ch. 2	Timer 2 - ch. 2
PC[0]	PAD[32]	—	37	IN/ANA	Timer 1 - ch. 0	ADC ch. 10	Timer 3 - ch. 3	Ext. INT 0
PC[1]	PAD[33]	24	38	IN/ANA	Timer 2 - ch. 2	ADC ch. 0	Timer 3 - ch. 4	Timer 2 - ch. 4
—	VDD_HV_ADC_TSENS	25	39	PW	—			
PC[2]	PAD[34]	26	40	IO	Timer 0 - ch. 5	DSPI 2 - CS 1	FlexCAN 1 - RX	FlexCAN 0 - RX
PC[3]	PAD[35]	27	41	IO	Timer 1 - ch. 0	DSPI 2 - CS 2	FlexCAN 1 - TX	FlexCAN 0 - TX
PC[4]	PAD[36]	28	42	IO	Timer 1 - ch. 1	DSPI 1 - CS 0	Ext. INT 1	FlexCAN 1 - RX
PC[5]	PAD[37]	—	43	IO	DSPI 1 - CS 0	Timer 1 - ch. 2	Nexus RDY	FlexCAN 1 - TX
PC[6]	PAD[38]	—	44	IO	DSPI 1 - Serial Data	Timer 1 - ch. 3	DSPI 2 - CS 4	DSPI 0 - Serial Data
PC[7]	PAD[39]	29	45	IO	Timer 1 - ch. 2	DSPI 1 - Serial Data	DSPI 2 - CS 5	DSPI 0 - CS 0
PC[8]	PAD[40]	30	46	IO	Timer 1 - ch. 3	DSPI 1 - Serial Data	DSPI 2 - CS 6	DSPI 0 - CS 1
PC[9]	PAD[41]	—	47	IO	DSPI 1 - Serial Data	Timer 1 - ch. 4	DSPI 2 - CS 7	DSPI 0 - Serial Data
PC[10]	PAD[42]	—	48	IO	DSPI 1 - CLK	Timer 1 - ch. 5	—	DSPI 0 - CLK
PC[11]	PAD[43]	31	49	IO	Timer 1 - ch. 4	DSPI 1 - CLK	—	DSPI 0 - CS 2
—	FCCU_F1	32	50	IO	FCCU_F1			
—	VDD_HV_IO	33	51	PWB51	—			
—	VDD_LV	34	52	PW	—			
—	EXTAL	35	53	ANA	—			

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
—	XTAL	36	54	ANA	—			
—	VDD_HV_OSC_PMC	37	55	PW	—			
PC[12]	PAD[44]	—	56	IO	Timer 0 - ch. 0	DSPI 1 - CS 3	—	LINFlex 0 - RX
PC[13]	PAD[45]	—	57	IO	Timer 0 - ch. 1	DSPI 1 - CS 4	—	LINFlex 0 - TX
PC[14]	PAD[46]	—	58	IO	Timer 0 - ch. 2	DSPI 1 - CS 5	—	DSPI 0 - CS 3
—	TDI	38	59	IO	—			
—	TMS	39	60	IO	—			
—	TDO	40	61	IO	—			
PC[15]	PAD[47]	41	62	IO	NMI	DSPI 1 - CS 2	Ext. INT 4	Timer 2 - ch. 0
—	TCK	42	63	IO	—			
—	TESTMODE	43	64	IO	—			
PD[0]	PAD[48]	—	65	IO	DSPI 1 - CS 6	Ext. INT 0	—	Timer 2 - ch. 1
—	PORST	44	66	IO	—			
PD[1]	PAD[49]	—	67	IO	Timer 0 - ch. 3	DSPI 1 - CS 7	—	DSPI 0 - CS 4
—	VDD_LV	45	68	PW	—			
PD[2]	PAD[50]	—	69	IO	Timer 2 - ch. 0	DSPI 2 - CS 1	DSPI 1 - CS 6	Timer 3 - ch. 0
PD[3]	PAD[51]	—	70	IO	Timer 2 - ch. 1	DSPI 2 - CS 2	DSPI 1 - CS 4	Timer 3 - ch. 1
PD[4]	PAD[52]	—	71	IO	Timer 2 - ch. 2	DSPI 2 - CS 3	DSPI 1 - CS 7	Timer 3 - ch. 2
—	VDD_HV_IO	46	—	PWB51	—			
PD[5]	PAD[53]	—	72	IO	DSPI 2 - CS 0	Timer 2 - ch. 1	DSPI 1 - CS 6	Timer 3 - ch. 3
PD[6]	PAD[54]	—	73	IO	DSPI 2 - Serial Data	Timer 2 - ch. 2	DSPI 1 - CS 5	DSPI 0 - CS 5
PD[7]	PAD[55]	47	74	IO	Timer 3 - ch. 0	CTU trg_inp	DSPI 1 - CS 2	LINFlex 1 - RX
PD[8]	PAD[56]	48	75	IO	Timer 3 - ch. 1	CTU trg_outp	DSPI 1 - CS 6	LINFlex 1 - TX

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 5* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C remaining time at or below 5.5 V.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
4. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
5. Solder profile per IPC/JEDEC J-STD-020D
6. Moisture sensitivity per JEDEC test method A112

4.4 Electromagnetic compatibility (EMC)

Table 7 describes the EMC characteristics of the device.

Table 7. Radiated emissions testing specification(1),(2)

Coupling structure	Test setup	Function	Functional configuration	BISS radiated emissions limit
Entire IC	(G) TEM	Reference test	C1-S3	18 dBµV
		Reference test with SSCG	C1-S3	18 dBµV
		Memory copy	C4-S2	18 dBµV
		Memory copy with SSCG	C4-S2	18 dBµV

1. Reference “BISS Generic IC EMC Test Specification”, version 1.2, section 9.3, “Emission test configuration for ICs with CPU”.
2. The EMC parameters are classified as "T", validated on testbench.

4.5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 8. ESD ratings(1),(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

4.9.2 I/O input DC characteristics

Table 13 provides input DC electrical characteristics as described in *Figure 4*.

Figure 4. I/O input DC electrical characteristics definition

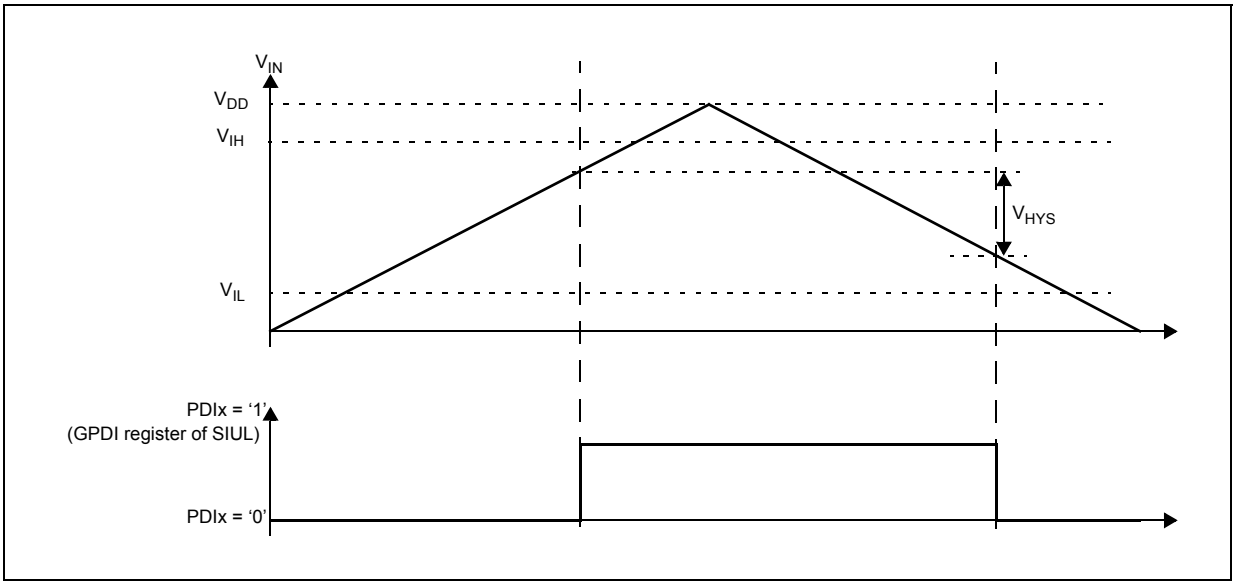


Table 13. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{IH}	SR	P	Input high level TTL	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	2.0	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IL}	SR	P	Input low level TTL	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	0.8	
V_{HYST}	—	C	Input hysteresis TTL	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.3(1)	—	—	
CMOS								
V_{IHCMOS_H}(2)	SR	P	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.65 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{IHCMOS}(2)	SR	P	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.6 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILCMOS_H}(2)	SR	P	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	-0.3	—	0.35 * $V_{DD\_HV\_IO}$	V

Table 18. Very Strong configuration I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{TR_V}	CC	D	Transition time output pin very strong configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 15 pF	—	—	4.5	ns
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 25 pF	—	—	5	
				3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V T_d = 0.6 ns, load = 10 pF	—	—	(4.5 * T_r) + T_f < 9	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 25 pF	—	—	4	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 50 pF	—	—	8	
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V T_d = 1 ns, load = 10 pF	—	—	(4.5 * T_r) + T_f < 9	
$t_{PHL-PLH\_V}$	CC	T	Difference between delay of rising and falling edges	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V C_L = 15 pF	0	—	1.2	ns
				4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V C_L = 25 pF	0	—	1.2	

For W/M (Weak/Medium) pads the following values hold true.

Table 19. I/O output characteristics for pads 4, 9, 11, 55, 56

Functionality	Symbol	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Weak	R_{OH_S}	PMOS output impedance weak configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	—	—	1600	Ω
	R_{OL_S}	NMOS output impedance weak configuration	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	—	—	1896	Ω
	f_{max_S}	Output frequency weak configuration	C_L = 25 pF	—	—	2	MHz
			C_L = 50 pF	—	—	1	
	t_{TR_S}	Transition time output pin weak configuration	C_L = 25 pF	—	—	127	ns
			C_L = 50 pF	—	—	2443	
	t_{SKEW_S}	Difference between rise time and fall time	—	—	—	50	%

Table 24. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1]	Value									Unit
		Typ [2]	C	Initial max			Typical end of life[3]	Lifetime max[4]		C	
				25 °C [5]	All temp [6]	C		≤ 1 K cycles	≤ 100 K cycles		
t_{AIC0P}	Array Integrity Check (0.5 MB, proprietary)[11]	0.75	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (0.5 MB, sequential)	25	T	—	—	—	—	—	—	—	ms
$t_{MR128KS}$	Margin Read (128 KB, sequential)	6.26	T	—	—	—	—	—	—	—	ms
t_{AABT}	Array Integrity Check Abort Latency	—	—	—	—	—	—	10		—	µs
t_{MABT}	Margin Read Abort Latency	—	—	—	—	—	—	10		—	µs

1. Actual hardware programming times; this does not include software overhead.
2. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
3. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
4. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
5. Initial factory condition: < 100 program/erase cycles, 20 °C < T_J < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
6. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, -40 °C < T_J < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Rate computed based on 128K sectors.
8. Only code sectors, not including EEPROM.
9. Time between erase suspend resume and next erase suspend.
10. Timings guaranteed by design.
11. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at 80 MHz.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 25. Flash memory Life Specification

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles

Table 25. Flash memory Life Specification (continued)

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
$N_{CER128K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
N_{DER16K}	16 KB EEPROM Flash endurance	100	—		—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—		—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	15	—		—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—		—	Years

1. Program and erase cycles supported across specified temperature specs.

4.15 PLL0/PLL1 electrical characteristics

The device provides a phase-locked loop (PLL0) as well as a frequency-modulated phase-locked loop (PLL1) module to generate a fast system clock from the main oscillator driver.

Table 26. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL1 reference clock[2]	—	37.5	—	78.125	MHz
Δ_{PLLIN}	SR	—	PLL1 reference clock duty cycle[2]	—	35	—	65	%
f_{PLLOUT}	CC	D	PLL1 output clock frequency	—	4.762	—	625	MHz
f_{VCO}[3]	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL1 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	110	µs
Δt_{STJIT}	CC	T	PLL1 short term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	—	—	1.8	ns
I_{PLL}	CC	C	PLL1 consumption	T_A = 25 °C	—	—	6	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ±2%.

Figure 14. DSPI CMOS master mode – classic timing, CPHA = 0

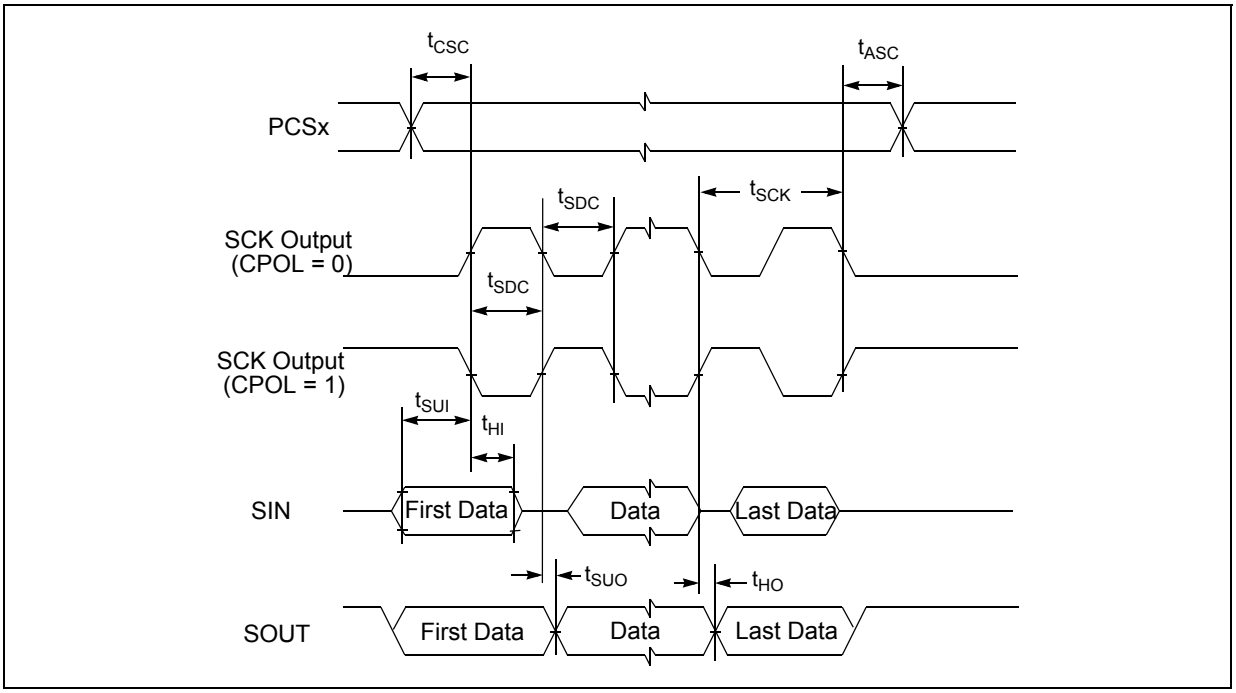


Figure 15. DSPI CMOS master mode – classic timing, CPHA = 1

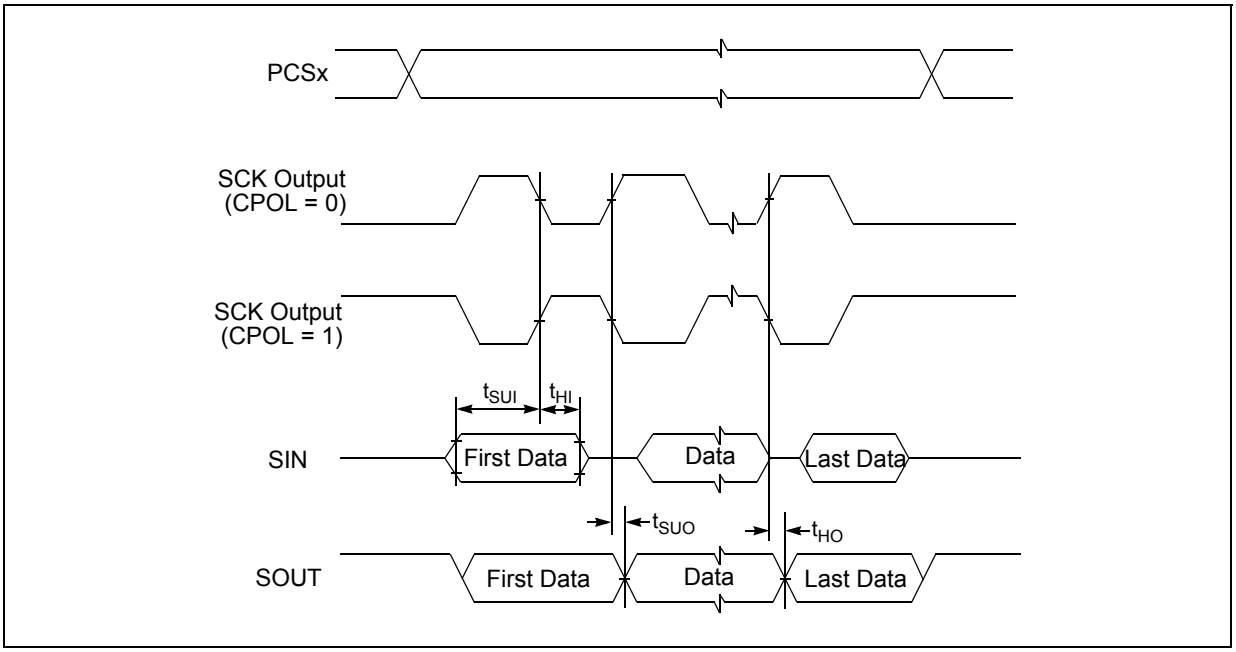


Table 36. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1(1)

#	Symbol	C	Characteristic	Condition		Value(2)		Unit
				Pad drive(3)	Load (C_L)	Min	Max	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK	SOUT and SCK drive strength			
					Very strong	25 pF	2	—	ns

1. Protocol clock is 40 MHz and all pads are configured as very strong.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. PCSx and PCSS using same pad configuration.

Figure 17. DSPI CMOS master mode – modified timing, CPHA = 0

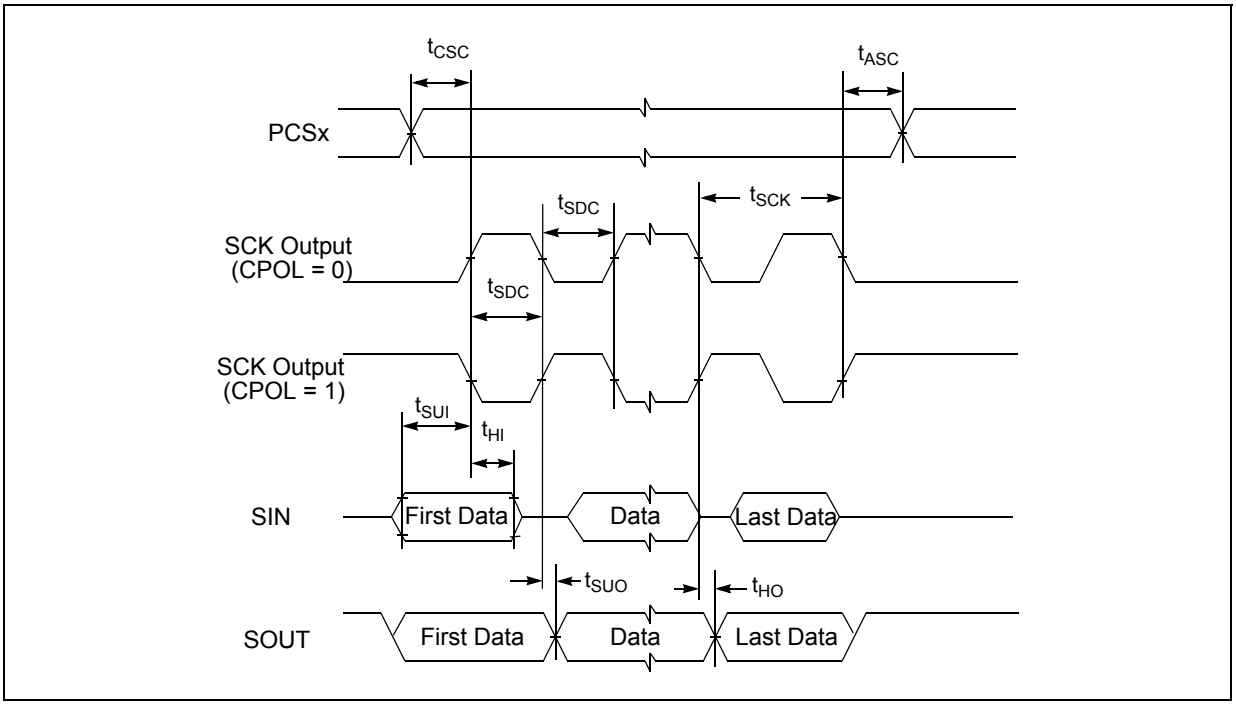


Figure 18. DSPI CMOS master mode – modified timing, CPHA = 1

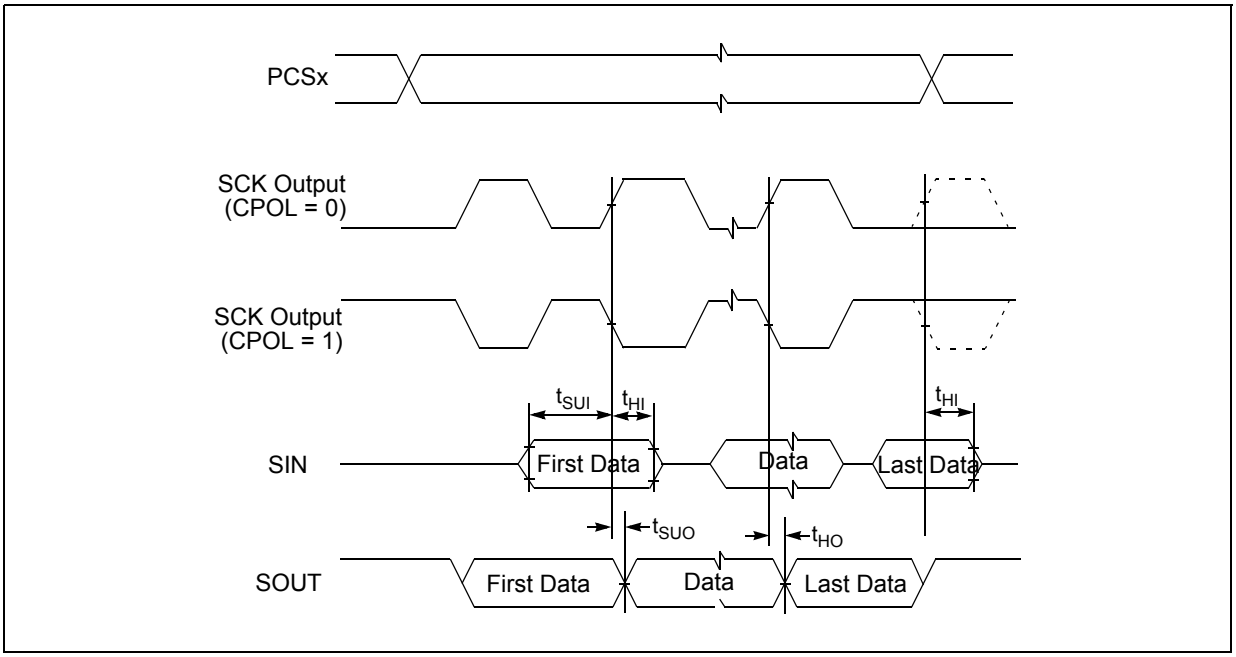
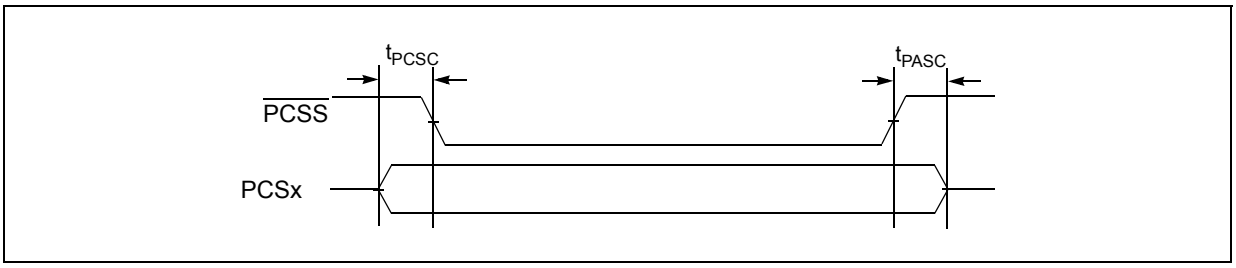
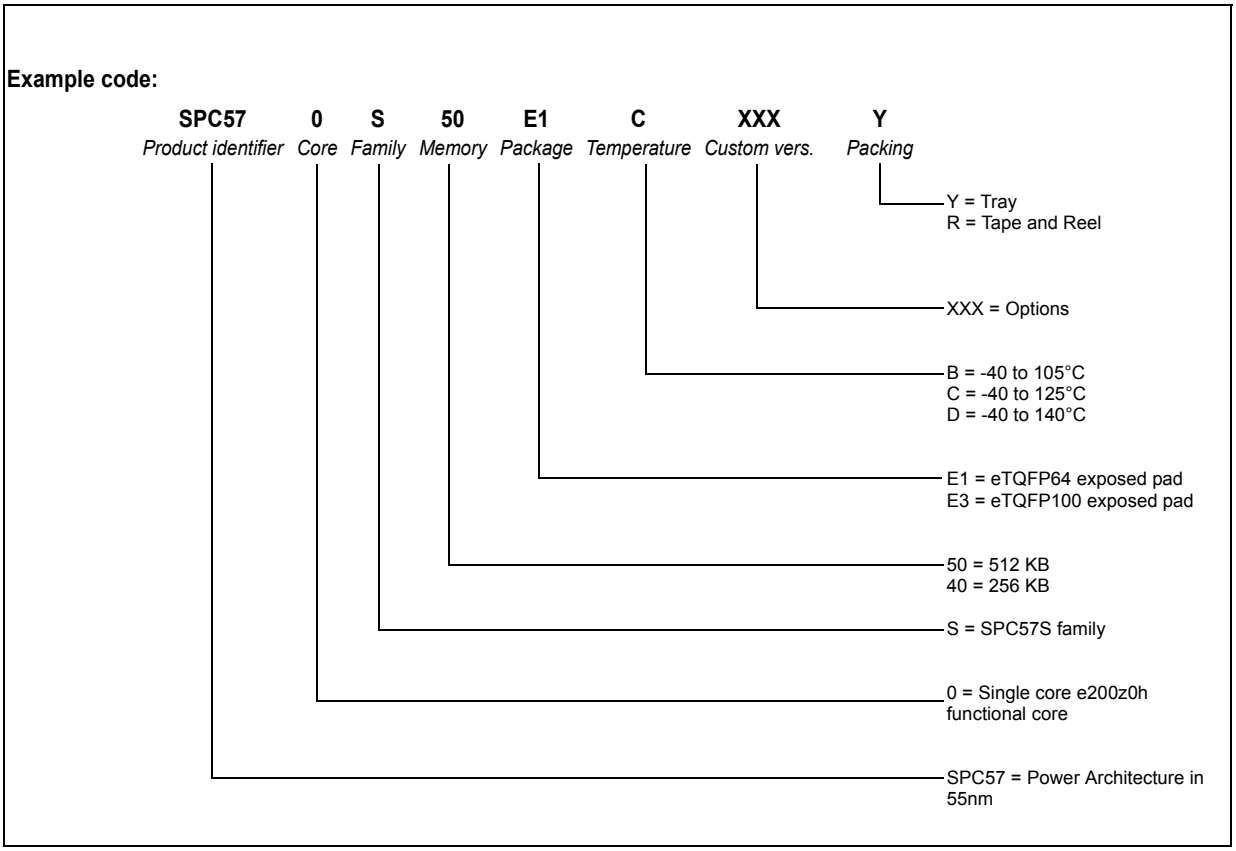


Figure 19. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)



6 Ordering information

Figure 22. Ordering information scheme



7 Revision history

Table 39. Document revision history

Date	Revision	Changes
08-Apr-2013	1	Initial release
21-Sep-2013	2	Updated Disclaimer.
03-Jun-2014	3	Updated the tables in Section 3.2.4: Pin multiplexing, *Section 3.3: Package pads/pins* and *Section 4.9.3: I/O output DC characteristics* Updated *Table 5: Parameter classifications* Updated *Table 24: Flash memory program and erase specifications*
12-Jun-2014	4	Changed timing values in *Table 24: Flash memory program and erase specifications* Added *Table 25: Flash memory Life Specification*
26-Mar-2015	5	Throughout the document: – Editorial and formatting updates – Changed device name from SPC570S40Ex to SPC570S – Used slow/medium/fast/veryfast to describe pad strength – Replaced all occurrences of PLL by PLL0 and FMPLL by PLL1 – Renamed $V_{DD\_HV\_OSC}$ as $V_{DD\_HV\_OSC\_PMC}$ – Renamed $V_{DD\_HV\_ADV}$ and $V_{DD\_ADC\_TSENS}$ as $V_{DD\_HV\_ADC\_TSENS}$ – Renamed $V_{DD\_HV\_ADR}$ as V_{REFH_ADC} – Renamed $V_{DD\_HV\_IO\_MAIN}$ and $V_{DD\_HV\_IO\_JTAG}$ as $V_{DD\_HV\_IO}$ – Renamed $V_{SS\_HV\_IO}$ as V_{SS} Clarified descriptions of *Figure 6: Noise filtering on reset signal* Removed subsections of *Section 3.2: Pin descriptions* with referral to the "Signal description" chapter in the devices' reference manual Added *Section 4.4: Electromagnetic compatibility (EMC)* Added *Section 4.5: Electrostatic discharge (ESD)* Added *Section 4.8: Current consumption* Updated *Section 4.11: Power management electrical characteristics* Added *Section 4.12: PMU monitor specifications* Added *Section 4.16: External oscillator (XOSC) electrical characteristics* Added *Section 4.19: Temperature sensor* Added *Section 4.20: JTAG interface timings* Added *Section 4.21: DSPI CMOS master mode timing* Added *Table 2: SPC570S40Ex, SPC570S50Ex device configuration differences* *Table 6: Absolute maximum ratings* – Added: $V_{DD\_HV\_OSC\_PMC}$, $V_{DD\_HV\_ADC\_TSENS}$, V_{REFH_ADC}, I_{MAXSEG} – Changed values for: *Cycle*, V_{IN}, I_{MAXD} – Added condition for t_{XRAY} – Removed T_J – Updated footnote *1.* and parameter descriptions for I_{INJD} and I_{INJA}

Table 39. Document revision history (continued)

Date	Revision	Changes
26-Mar-2015	5	*Table 9: Device operating conditions*: – Added: $V_{DD\_HV\_OSC\_PMC}$, V_{REFH_ADC} - $V_{DD\_HV\_ADC\_TSENS}$, V_{IN}, I_{MAXSEG} – Changed values for: $V_{DD\_HV\_IO}$ – Updated parameter descriptions for: V_{REFH_ADC}, V_{REFH_ADC} - $V_{DD\_HV\_ADC\_TSENS}$ – Updated classification tags and footnotes for: $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_OSC\_PMC}$ – Removed: V_{DD_LV} *Table 13: I/O input DC electrical characteristics* – Added I_{LKG} – Changed conditions for: V_{IH}, V_{IL}, V_{HYST}, V_{IHCMOS_H}, $V_{IHCMOS}^{(2)}$, $V_{ILCMOS\_H}^{(2)}$, $V_{ILCMOS}^{(2)}$, $V_{HYSCMOS}$ – Changed values for: V_{IH}, V_{IL}, C_{IN} – Removed 4.0 V < $V_{DD\_HV\_IO}$ < 4.5 V conditions from the *Automotive* section Updated *Table 14: I/O pull-up/pull-down DC electrical characteristics* Removed “Min” values from tables: *15*, *16*, *17*, *19* Removed “Typ” values from tables: *15*, *16*, *17*, *18*, *19* Renamed *Table 19: I/O output characteristics for pads 4, 9, 11, 55, 56* to include the pad numbers *Table 20: Reset electrical characteristics* changed conditions and values for: I_{OL_R}, $\lvert I_{WPU}\rvert$, $\lvert I_{WPD}\rvert$ *Table 21: Voltage regulator electrical characteristics* – changed values and condition description for C_{DECBV} – removed $I_{MREGINT}$ *Table 24: Flash memory program and erase specifications* changed values for: t_{PSUS}, t_{ESUS} *Table 30: Internal RC oscillator electrical specifications* – Removed condition and changed values for df_{var_noT} – Changed values for df_{var_SW} *Table 32: ADC conversion characteristics* – Changed values for: $I_{ADCREFH}$, I_{ADCVDD}, *DNL* – Added footnotes for $V_{SS\_HV\_ADR}$ and $I_{ADCREFH}$
23-Sep-2015	6	*Table 6: Absolute maximum ratings*: – Updated t_{XRAY} *Table 11: Current consumption*: – Updated IDD information – Added classification tag, Min Typ and Max columns – Updated value of maximum consumption during boot time M/LBIST Tables *15*, *16*, *17*, *18*: – Added classification tag, Min Typ and Max columns *Table 22: Trimmed (PVT) values*: – Updated POR200 lower limit Removed “(pending silicon Qualification)” from the titles of *Table 24* and *Table 25* Corrected *Section 4.12.2: Power up/down sequencing* Reverted to using weak/medium/strong/very strong to describe pad strength