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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

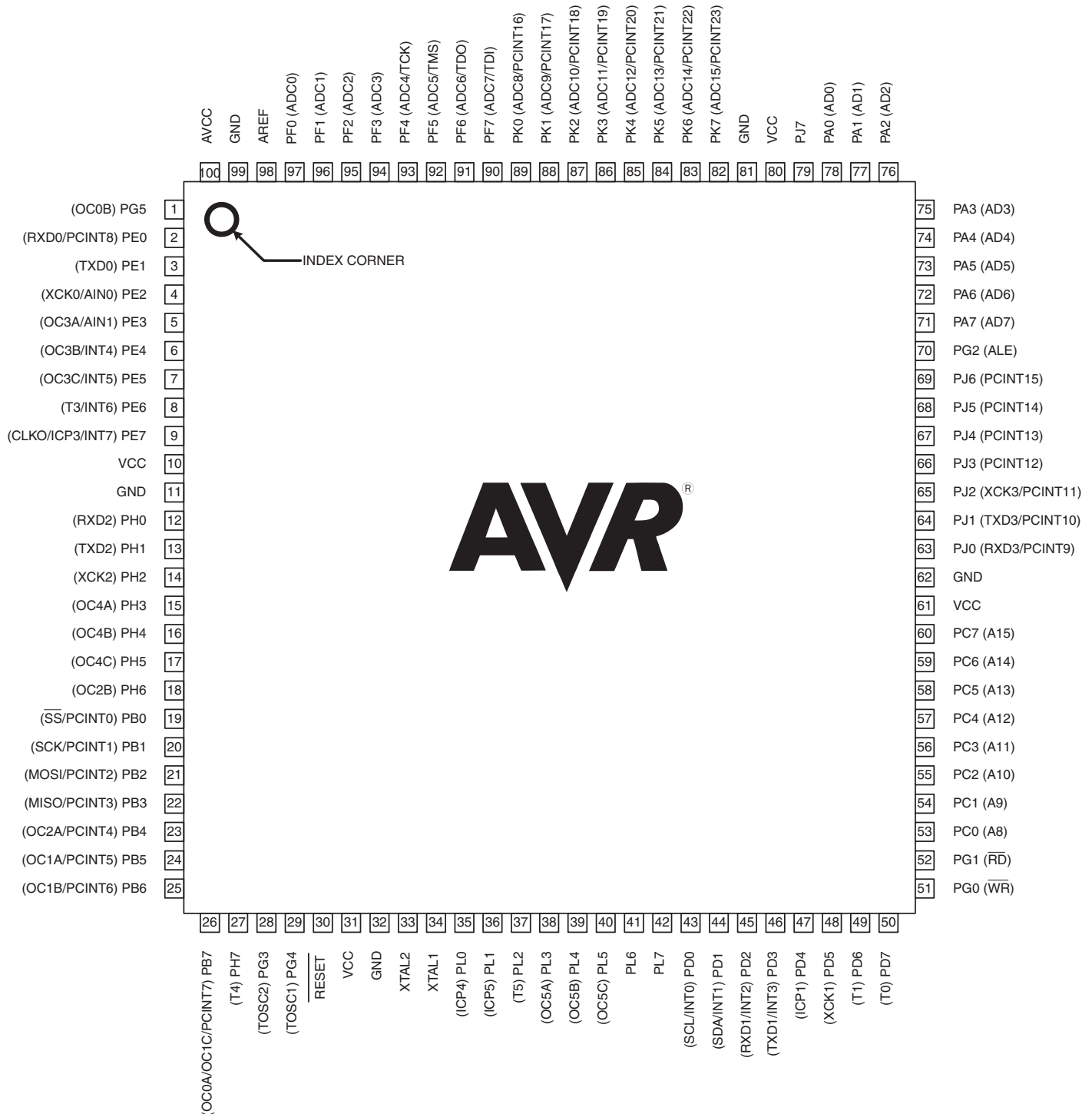
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

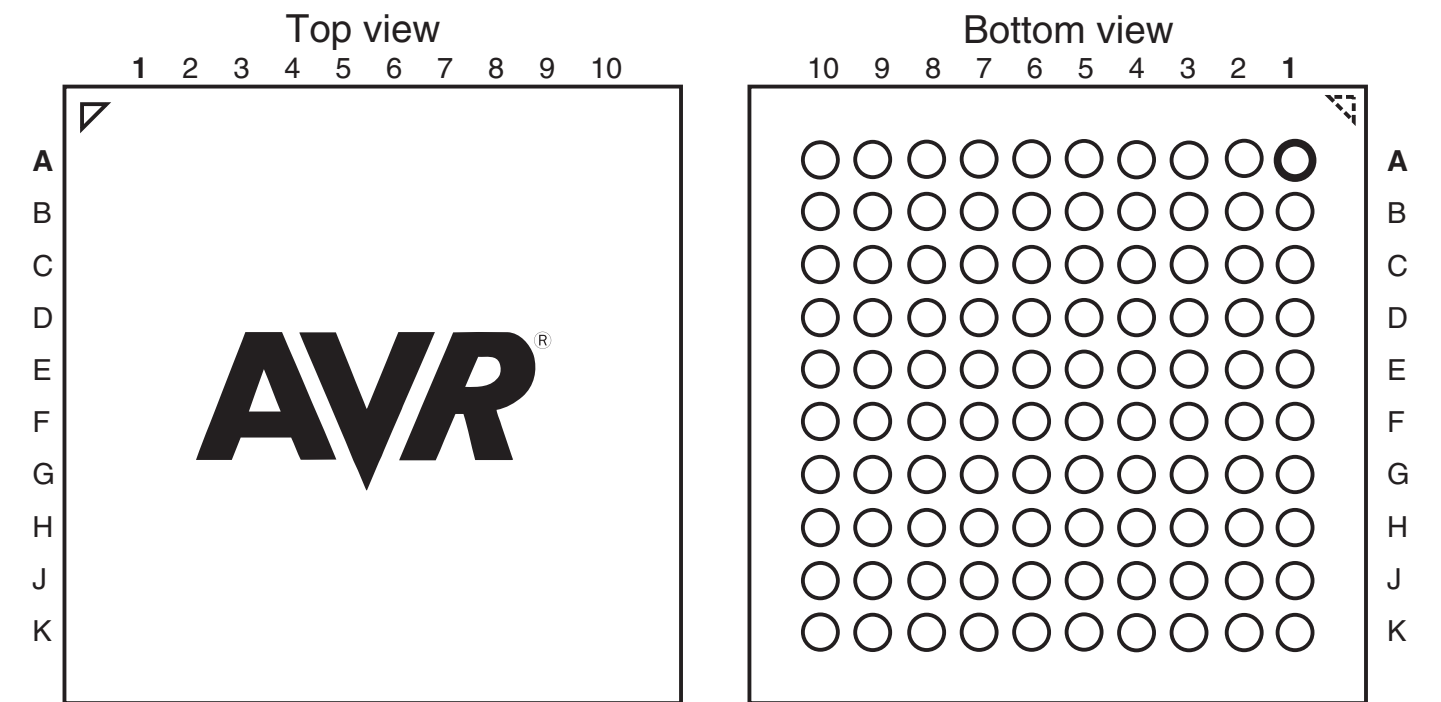
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atmega1280-16aur">https://www.e-xfl.com/product-detail/microchip-technology/atmega1280-16aur</a>

# 1. Pin Configurations

Figure 1-1. TQFP-pinout ATmega640/1280/2560



**Figure 1-2.** CBGA-pinout ATmega640/1280/2560

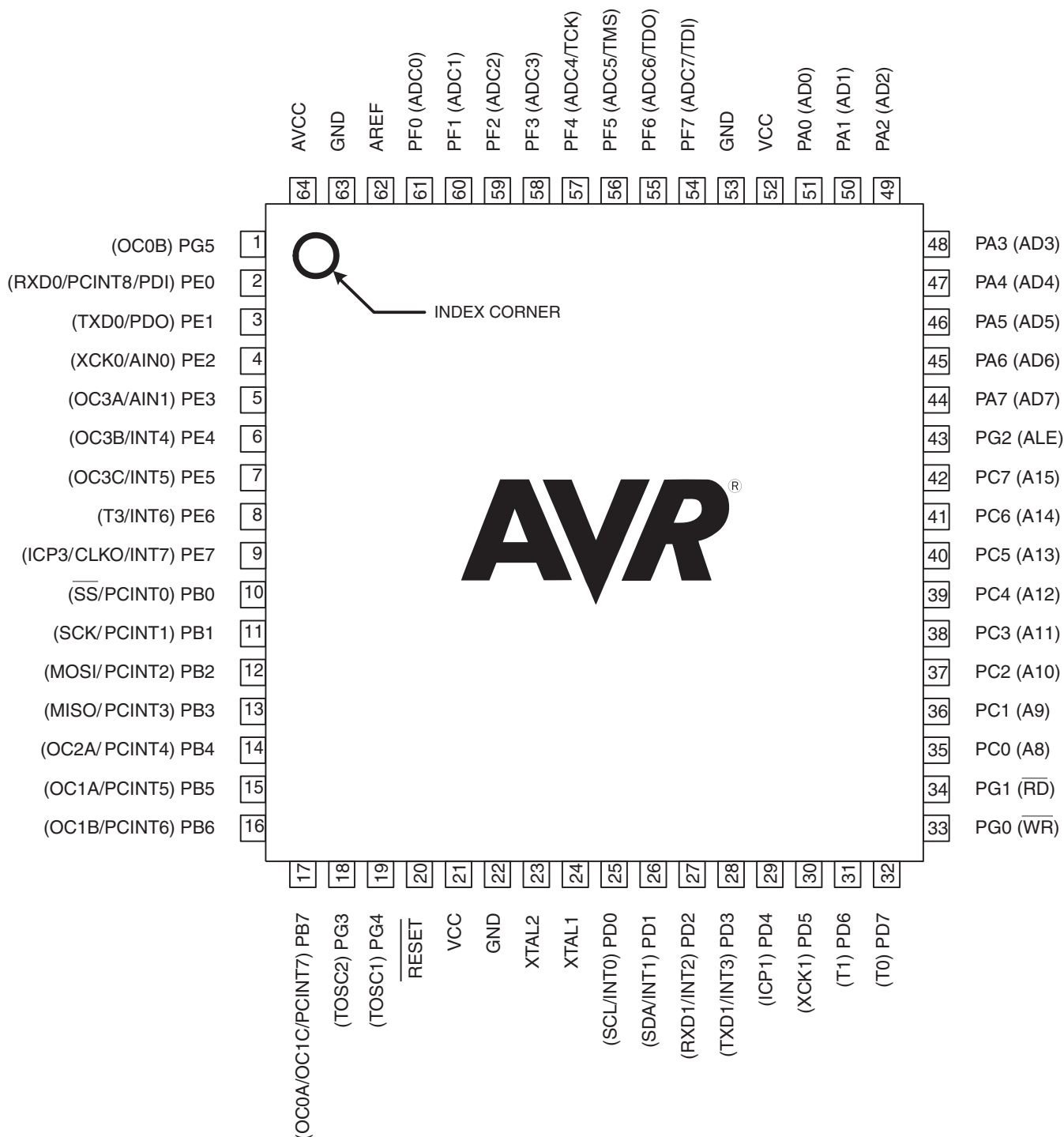


**Table 1-1.** CBGA-pinout ATmega640/1280/2560

	1	2	3	4	5	6	7	8	9	10
A	GND	AREF	PF0	PF2	PF5	PK0	PK3	PK6	GND	VCC
B	AVCC	PG5	PF1	PF3	PF6	PK1	PK4	PK7	PA0	PA2
C	PE2	PE0	PE1	PF4	PF7	PK2	PK5	PJ7	PA1	PA3
D	PE3	PE4	PE5	PE6	PH2	PA4	PA5	PA6	PA7	PG2
E	PE7	PH0	PH1	PH3	PH5	PJ6	PJ5	PJ4	PJ3	PJ2
F	VCC	PH4	PH6	PB0	PL4	PD1	PJ1	PJ0	PC7	GND
G	GND	PB1	PB2	PB5	PL2	PD0	PD5	PC5	PC6	VCC
H	PB3	PB4	RESET	PL1	PL3	PL7	PD4	PC4	PC3	PC2
J	PH7	PG3	PB6	PL0	XTAL2	PL6	PD3	PC1	PC0	PG1
K	PB7	PG4	VCC	GND	XTAL1	PL5	PD2	PD6	PD7	PG0

Note: The functions for each pin is the same as for the 100 pin packages shown in [Figure 1-1 on page 2](#).

**Figure 1-3.** Pinout ATmega1281/2561



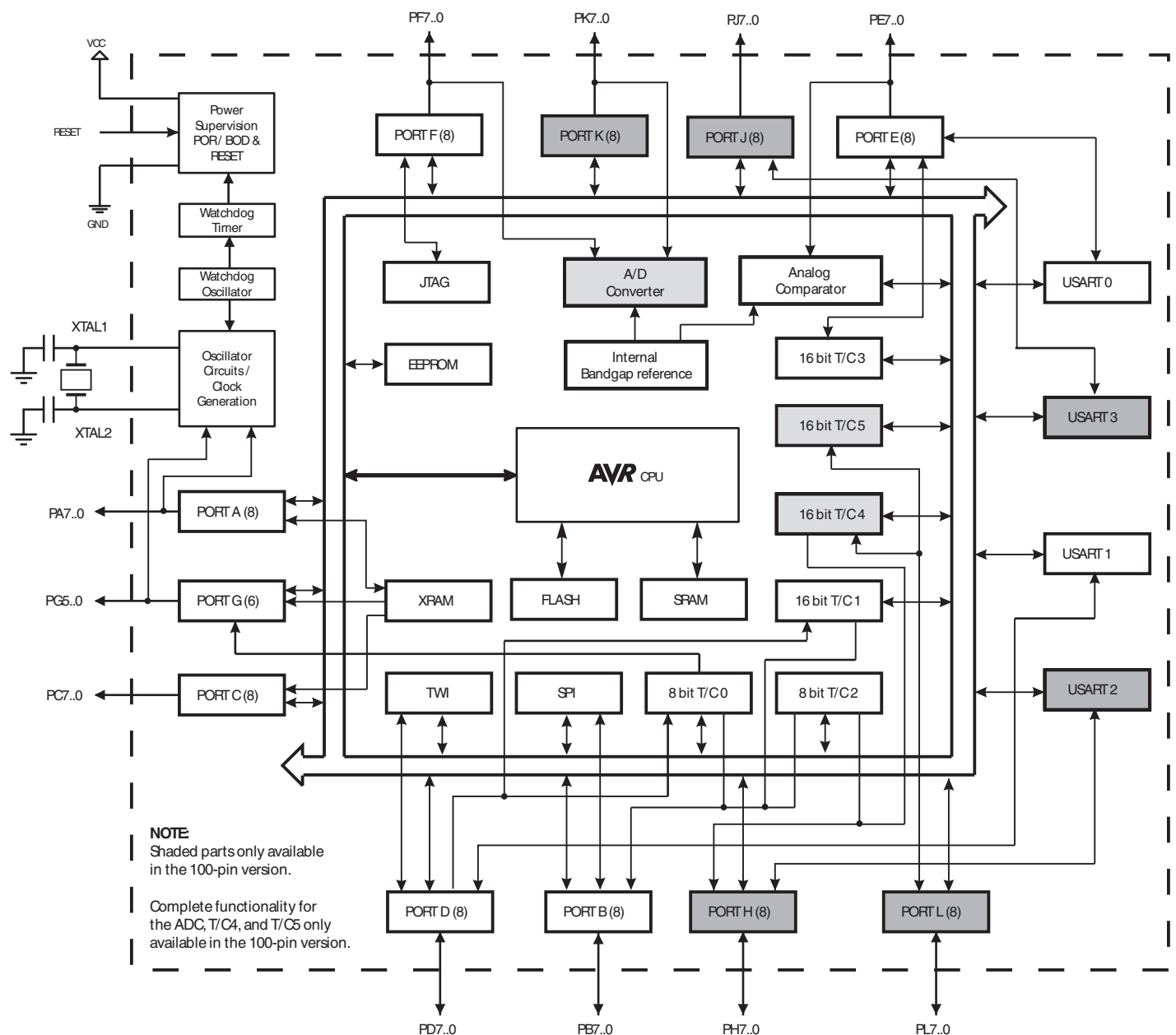
**Note:** The large center pad underneath the QFN/MLF package is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

## 2. Overview

The ATmega640/1280/1281/2560/2561 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega640/1280/1281/2560/2561 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### 2.1 Block Diagram

Figure 2-1. Block Diagram



The Atmel® AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega640/1280/1281/2560/2561 provides the following features: 64K/128K/256K bytes of In-System Programmable Flash with Read-While-Write capabilities, 4Kbytes EEPROM, 8Kbytes SRAM, 54/86 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), six flexible Timer/Counters with compare modes and PWM, four USARTs, a byte oriented 2-wire Serial Interface, a 16-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE® std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using the Atmel high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega640/1280/1281/2560/2561 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega640/1280/1281/2560/2561 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

### 2.3.6 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega640/1280/1281/2560/2561 as listed on [page 80](#).

### 2.3.7 Port E (PE7..PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega640/1280/1281/2560/2561 as listed on [page 82](#).

### 2.3.8 Port F (PF7..PF0)

Port F serves as analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

### 2.3.9 Port G (PG5..PG0)

Port G is a 6-bit I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega640/1280/1281/2560/2561 as listed on [page 86](#).

### 2.3.10 Port H (PH7..PH0)

Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port H also serves the functions of various special features of the ATmega640/1280/2560 as listed on [page 88](#).

### 2.3.11 Port J (PJ7..PJ0)

Port J is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port J also serves the functions of various special features of the ATmega640/1280/2560 as listed on [page 90](#).

### 3. Resources

A comprehensive set of development tools and application notes, and datasheets are available for download on <http://www.atmel.com/avr>.

### 4. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBR", "SBRC", "SBR", and "CBR".

### 5. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 ppm over 20 years at 85°C or 100 years at 25°C.

### 6. Capacitive touch sensing

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: [www.atmel.com/qtouchlibrary](http://www.atmel.com/qtouchlibrary). For implementation details and other information, refer to the [Atmel QTouch Library User Guide](#) - also available for download from the Atmel website.



## 7. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page	
(0x1FF)	Reserved	-	-	-	-	-	-	-	-		
...	Reserved	-	-	-	-	-	-	-	-		
(0x13F)	Reserved										
(0x13E)	Reserved										
(0x13D)	Reserved										
(0x13C)	Reserved										
(0x13B)	Reserved										
(0x13A)	Reserved										
(0x139)	Reserved										
(0x138)	Reserved										
(0x137)	Reserved										
(0x136)	UDR3	USART3 I/O Data Register								<a href="#">page 218</a>	
(0x135)	UBRR3H	-	-	-	-	USART3 Baud Rate Register High Byte					<a href="#">page 222</a>
(0x134)	UBRR3L	USART3 Baud Rate Register Low Byte								<a href="#">page 222</a>	
(0x133)	Reserved	-	-	-	-	-	-	-	-		
(0x132)	UCSR3C	UMSEL31	UMSEL30	UPM31	UPM30	USBS3	UCSZ31	UCSZ30	UCPOL3	<a href="#">page 235</a>	
(0x131)	UCSR3B	RXCIE3	TXCIE3	UDRIE3	RXEN3	TXEN3	UCSZ32	RXB83	TXB83	<a href="#">page 234</a>	
(0x130)	UCSR3A	RXC3	TXC3	UDRE3	FE3	DOR3	UPE3	U2X3	MPCM3	<a href="#">page 233</a>	
(0x12F)	Reserved	-	-	-	-	-	-	-	-		
(0x12E)	Reserved	-	-	-	-	-	-	-	-		
(0x12D)	OCR5CH	Timer/Counter5 - Output Compare Register C High Byte								<a href="#">page 160</a>	
(0x12C)	OCR5CL	Timer/Counter5 - Output Compare Register C Low Byte								<a href="#">page 160</a>	
(0x12B)	OCR5BH	Timer/Counter5 - Output Compare Register B High Byte								<a href="#">page 160</a>	
(0x12A)	OCR5BL	Timer/Counter5 - Output Compare Register B Low Byte								<a href="#">page 160</a>	
(0x129)	OCR5AH	Timer/Counter5 - Output Compare Register A High Byte								<a href="#">page 160</a>	
(0x128)	OCR5AL	Timer/Counter5 - Output Compare Register A Low Byte								<a href="#">page 160</a>	
(0x127)	ICR5H	Timer/Counter5 - Input Capture Register High Byte								<a href="#">page 161</a>	
(0x126)	ICR5L	Timer/Counter5 - Input Capture Register Low Byte								<a href="#">page 161</a>	
(0x125)	TCNT5H	Timer/Counter5 - Counter Register High Byte								<a href="#">page 158</a>	
(0x124)	TCNT5L	Timer/Counter5 - Counter Register Low Byte								<a href="#">page 158</a>	
(0x123)	Reserved	-	-	-	-	-	-	-	-		
(0x122)	TCCR5C	FOC5A	FOC5B	FOC5C	-	-	-	-	-	<a href="#">page 157</a>	
(0x121)	TCCR5B	ICNC5	ICES5	-	WGM53	WGM52	CS52	CS51	CS50	<a href="#">page 156</a>	
(0x120)	TCCR5A	COM5A1	COM5A0	COM5B1	COM5B0	COM5C1	COM5C0	WGM51	WGM50	<a href="#">page 154</a>	
(0x11F)	Reserved	-	-	-	-	-	-	-	-		
(0x11E)	Reserved	-	-	-	-	-	-	-	-		
(0x11D)	Reserved	-	-	-	-	-	-	-	-		
(0x11C)	Reserved	-	-	-	-	-	-	-	-		
(0x11B)	Reserved	-	-	-	-	-	-	-	-		
(0x11A)	Reserved	-	-	-	-	-	-	-	-		
(0x119)	Reserved	-	-	-	-	-	-	-	-		
(0x118)	Reserved	-	-	-	-	-	-	-	-		
(0x117)	Reserved	-	-	-	-	-	-	-	-		
(0x116)	Reserved	-	-	-	-	-	-	-	-		
(0x115)	Reserved	-	-	-	-	-	-	-	-		
(0x114)	Reserved	-	-	-	-	-	-	-	-		
(0x113)	Reserved	-	-	-	-	-	-	-	-		
(0x112)	Reserved	-	-	-	-	-	-	-	-		
(0x111)	Reserved	-	-	-	-	-	-	-	-		
(0x110)	Reserved	-	-	-	-	-	-	-	-		
(0x10F)	Reserved	-	-	-	-	-	-	-	-		
(0x10E)	Reserved	-	-	-	-	-	-	-	-		
(0x10D)	Reserved	-	-	-	-	-	-	-	-		
(0x10C)	Reserved	-	-	-	-	-	-	-	-		
(0x10B)	PORTL	PORTL7	PORTL6	PORTL5	PORTL4	PORTL3	PORTL2	PORTL1	PORTL0	<a href="#">page 100</a>	
(0x10A)	DDRL	DDL7	DDL6	DDL5	DDL4	DDL3	DDL2	DDL1	DDL0	<a href="#">page 100</a>	
(0x109)	PINL	PINL7	PINL6	PINL5	PINL4	PINL3	PINL2	PINL1	PINL0	<a href="#">page 100</a>	
(0x108)	PORTK	PORTK7	PORTK6	PORTK5	PORTK4	PORTK3	PORTK2	PORTK1	PORTK0	<a href="#">page 99</a>	
(0x107)	DDRK	DDK7	DDK6	DDK5	DDK4	DDK3	DDK2	DDK1	DDK0	<a href="#">page 99</a>	
(0x106)	PINK	PINK7	PINK6	PINK5	PINK4	PINK3	PINK2	PINK1	PINK0	<a href="#">page 99</a>	
(0x105)	PORTJ	PORTJ7	PORTJ6	PORTJ5	PORTJ4	PORTJ3	PORTJ2	PORTJ1	PORTJ0	<a href="#">page 99</a>	
(0x104)	DDRJ	DDJ7	DDJ6	DDJ5	DDJ4	DDJ3	DDJ2	DDJ1	DDJ0	<a href="#">page 99</a>	
(0x103)	PINJ	PINJ7	PINJ6	PINJ5	PINJ4	PINJ3	PINJ2	PINJ1	PINJ0	<a href="#">page 99</a>	
(0x102)	PORTH	PORTH7	PORTH6	PORTH5	PORTH4	PORTH3	PORTH2	PORTH1	PORTH0	<a href="#">page 98</a>	
(0x101)	DDRH	DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0	<a href="#">page 99</a>	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x100)	PINH	PINH7	PINH6	PINH5	PINH4	PINH3	PINH2	PINH1	PINH0	<a href="#">page 99</a>
(0xFF)	Reserved	-	-	-	-	-	-	-	-	
(0xFE)	Reserved	-	-	-	-	-	-	-	-	
(0xFD)	Reserved	-	-	-	-	-	-	-	-	
(0xFC)	Reserved	-	-	-	-	-	-	-	-	
(0xFB)	Reserved	-	-	-	-	-	-	-	-	
(0xFA)	Reserved	-	-	-	-	-	-	-	-	
(0xF9)	Reserved	-	-	-	-	-	-	-	-	
(0xF8)	Reserved	-	-	-	-	-	-	-	-	
(0xF7)	Reserved	-	-	-	-	-	-	-	-	
(0xF6)	Reserved	-	-	-	-	-	-	-	-	
(0xF5)	Reserved	-	-	-	-	-	-	-	-	
(0xF4)	Reserved	-	-	-	-	-	-	-	-	
(0xF3)	Reserved	-	-	-	-	-	-	-	-	
(0xF2)	Reserved	-	-	-	-	-	-	-	-	
(0xF1)	Reserved	-	-	-	-	-	-	-	-	
(0xF0)	Reserved	-	-	-	-	-	-	-	-	
(0xEF)	Reserved	-	-	-	-	-	-	-	-	
(0xEE)	Reserved	-	-	-	-	-	-	-	-	
(0xED)	Reserved	-	-	-	-	-	-	-	-	
(0xEC)	Reserved	-	-	-	-	-	-	-	-	
(0xEB)	Reserved	-	-	-	-	-	-	-	-	
(0xEA)	Reserved	-	-	-	-	-	-	-	-	
(0xE9)	Reserved	-	-	-	-	-	-	-	-	
(0xE8)	Reserved	-	-	-	-	-	-	-	-	
(0xE7)	Reserved	-	-	-	-	-	-	-	-	
(0xE6)	Reserved	-	-	-	-	-	-	-	-	
(0xE5)	Reserved	-	-	-	-	-	-	-	-	
(0xE4)	Reserved	-	-	-	-	-	-	-	-	
(0xE3)	Reserved	-	-	-	-	-	-	-	-	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	-	-	-	-	-	-	-	-	
(0xE0)	Reserved	-	-	-	-	-	-	-	-	
(0xDF)	Reserved	-	-	-	-	-	-	-	-	
(0xDE)	Reserved	-	-	-	-	-	-	-	-	
(0xDD)	Reserved	-	-	-	-	-	-	-	-	
(0xDC)	Reserved	-	-	-	-	-	-	-	-	
(0xDB)	Reserved	-	-	-	-	-	-	-	-	
(0xDA)	Reserved	-	-	-	-	-	-	-	-	
(0xD9)	Reserved	-	-	-	-	-	-	-	-	
(0xD8)	Reserved	-	-	-	-	-	-	-	-	
(0xD7)	Reserved	-	-	-	-	-	-	-	-	
(0xD6)	UDR2	USART2 I/O Data Register								<a href="#">page 218</a>
(0xD5)	UBRR2H	-	-	-	-	USART2 Baud Rate Register High Byte				<a href="#">page 222</a>
(0xD4)	UBRR2L	USART2 Baud Rate Register Low Byte								<a href="#">page 222</a>
(0xD3)	Reserved	-	-	-	-	-	-	-	-	
(0xD2)	UCSR2C	UMSEL21	UMSEL20	UPM21	UPM20	USBS2	UCSZ21	UCSZ20	UCPOL2	<a href="#">page 235</a>
(0xD1)	UCSR2B	RXCIE2	TXCIE2	UDRIE2	RXEN2	TXEN2	UCSZ22	RXB82	TXB82	<a href="#">page 234</a>
(0xD0)	UCSR2A	RXC2	TXC2	UDRE2	FE2	DOR2	UPE2	U2X2	MPCM2	<a href="#">page 233</a>
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	UDR1	USART1 I/O Data Register								<a href="#">page 218</a>
(0xCD)	UBRR1H	-	-	-	-	USART1 Baud Rate Register High Byte				<a href="#">page 222</a>
(0xCC)	UBRR1L	USART1 Baud Rate Register Low Byte								<a href="#">page 222</a>
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	UCSR1C	UMSEL11	UMSEL10	UPM11	UPM10	USBS1	UCSZ11	UCSZ10	UCPOL1	<a href="#">page 235</a>
(0xC9)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	UCSZ12	RXB81	TXB81	<a href="#">page 234</a>
(0xC8)	UCSR1A	RXC1	TXC1	UDRE1	FE1	DOR1	UPE1	U2X1	MPCM1	<a href="#">page 233</a>
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	UDR0	USART0 I/O Data Register								<a href="#">page 218</a>
(0xC5)	UBRR0H	-	-	-	-	USART0 Baud Rate Register High Byte				<a href="#">page 222</a>
(0xC4)	UBRR0L	USART0 Baud Rate Register Low Byte								<a href="#">page 222</a>
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	UCSR0C	UMSEL01	UMSEL00	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	<a href="#">page 235</a>
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	<a href="#">page 234</a>
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	<a href="#">page 234</a>
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	-	<a href="#">page 264</a>

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x78)	ADCL	ADC Data Register Low byte								<a href="#">page 286</a>
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	XMCRB	XMBK	-	-	-	-	XMM2	XMM1	XMM0	<a href="#">page 38</a>
(0x74)	XMCRA	SRE	SRL2	SRL1	SRL0	SRW11	SRW10	SRW01	SRW00	<a href="#">page 36</a>
(0x73)	TIMSK5	-	-	ICIE5	-	OCIE5C	OCIE5B	OCIE5A	TOIE5	<a href="#">page 162</a>
(0x72)	TIMSK4	-	-	ICIE4	-	OCIE4C	OCIE4B	OCIE4A	TOIE4	<a href="#">page 161</a>
(0x71)	TIMSK3	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3	<a href="#">page 161</a>
(0x70)	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2	<a href="#">page 188</a>
(0x6F)	TIMSK1	-	-	ICIE1	-	OCIE1C	OCIE1B	OCIE1A	TOIE1	<a href="#">page 161</a>
(0x6E)	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0	<a href="#">page 131</a>
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	<a href="#">page 113</a>
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	<a href="#">page 113</a>
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	<a href="#">page 114</a>
(0x6A)	EICRB	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40	<a href="#">page 110</a>
(0x69)	EICRA	ISC31	ISC30	ISC21	ISC20	ISC11	ISC10	ISC01	ISC00	<a href="#">page 110</a>
(0x68)	PCICR	-	-	-	-	-	PCIE2	PCIE1	PCIE0	<a href="#">page 112</a>
(0x67)	Reserved	-	-	-	-	-	-	-	-	
(0x66)	OSCCAL	Oscillator Calibration Register								<a href="#">page 48</a>
(0x65)	PRR1	-	-	PRTIM5	PRTIM4	PRTIM3	PRUSART3	PRUSART2	PRUSART1	<a href="#">page 56</a>
(0x64)	PRR0	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	PRUSART0	PRADC	<a href="#">page 55</a>
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	<a href="#">page 48</a>
(0x60)	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	<a href="#">page 65</a>
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	<a href="#">page 13</a>
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	<a href="#">page 15</a>
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	<a href="#">page 15</a>
0x3C (0x5C)	EIND	-	-	-	-	-	-	-	EIND0	<a href="#">page 16</a>
0x3B (0x5B)	RAMPZ	-	-	-	-	-	-	RAMPZ1	RAMPZ0	<a href="#">page 16</a>
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	<a href="#">page 323</a>
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-	
0x35 (0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	IVCE	<a href="#">page 64, 108, 96, 301</a>
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF	<a href="#">page 301</a>
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	<a href="#">page 50</a>
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
0x31 (0x51)	OCDR	OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	<a href="#">page 294</a>
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	<a href="#">page 266</a>
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR	SPI Data Register								<a href="#">page 199</a>
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	<a href="#">page 198</a>
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	<a href="#">page 197</a>
0x2B (0x4B)	GPIOR2	General Purpose I/O Register 2								<a href="#">page 36</a>
0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1								<a href="#">page 36</a>
0x29 (0x49)	Reserved	-	-	-	-	-	-	-	-	
0x28 (0x48)	OCR0B	Timer/Counter0 Output Compare Register B								<a href="#">page 130</a>
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								<a href="#">page 130</a>
0x26 (0x46)	TCNT0	Timer/Counter0 (8 Bit)								<a href="#">page 130</a>
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00	<a href="#">page 129</a>
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	<a href="#">page 126</a>
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC	<a href="#">page 166, 189</a>
0x22 (0x42)	EEARH	-	-	-	-	EEPROM Address Register High Byte				<a href="#">page 34</a>
0x21 (0x41)	EEARL	EEPROM Address Register Low Byte								<a href="#">page 34</a>
0x20 (0x40)	EEDR	EEPROM Data Register								<a href="#">page 34</a>
0x1F (0x3F)	EECR	-	-	EEP1	EEP0	EERIE	EEMPE	EEPE	EERE	<a href="#">page 34</a>
0x1E (0x3E)	GPIOR0	General Purpose I/O Register 0								<a href="#">page 36</a>
0x1D (0x3D)	EIMSK	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0	<a href="#">page 111</a>
0x1C (0x3C)	EIFR	INTF7	INTF6	INTF5	INTF4	INTF3	INTF2	INTF1	INTF0	<a href="#">page 112</a>
0x1B (0x3B)	PCIFR	-	-	-	-	-	PCIF2	PCIF1	PCIF0	<a href="#">page 113</a>
0x1A (0x3A)	TIFR5	-	-	ICF5	-	OCF5C	OCF5B	OCF5A	TOV5	<a href="#">page 162</a>
0x19 (0x39)	TIFR4	-	-	ICF4	-	OCF4C	OCF4B	OCF4A	TOV4	<a href="#">page 162</a>
0x18 (0x38)	TIFR3	-	-	ICF3	-	OCF3C	OCF3B	OCF3A	TOV3	<a href="#">page 162</a>
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	<a href="#">page 188</a>
0x16 (0x36)	TIFR1	-	-	ICF1	-	OCF1C	OCF1B	OCF1A	TOV1	<a href="#">page 162</a>
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	<a href="#">page 131</a>

Mnemonics	Operands	Description	Operation	Flags	#Clocks
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
<b>MCU CONTROL INSTRUCTIONS</b>					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

Note: EICALL and EIJMP do not exist in ATmega640/1280/1281.  
ELPM does not exist in ATmega640.

## 9. Ordering Information

### 9.1 ATmega640

Speed [MHz] <sup>(2)</sup>	Power Supply	Ordering Code	Package <sup>(1)(3)</sup>	Operation Range
8	1.8 - 5.5V	ATmega640V-8AU ATmega640V-8AUR <sup>(4)</sup> ATmega640V-8CU ATmega640V-8CUR <sup>(4)</sup>	100A 100A 100C1 100C1	Industrial (-40°C to 85°C)
16	2.7 - 5.5V	ATmega640-16AU ATmega640-16AUR <sup>(4)</sup> ATmega640-16CU ATmega640-16CUR <sup>(4)</sup>	100A 100A 100C1 100C1	

- Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. See [“Speed Grades” on page 357](#).
  3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  4. Tape & Reel.

Package Type	
<b>100A</b>	100-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>100C1</b>	100-ball, Chip Ball Grid Array (CBGA)

### 9.3 ATmega1281

Speed [MHz] <sup>(2)</sup>	Power Supply	Ordering Code	Package <sup>(1)(3)</sup>	Operation Range
8	1.8 - 5.5V	ATmega1281V-8AU ATmega1281V-8AUR <sup>(4)</sup> ATmega1281V-8MU ATmega1281V-8MUR <sup>(4)</sup>	64A 64A 64M2 64M2	Industrial (-40°C to 85°C)
16	2.7 - 5.5V	ATmega1281-16AU ATmega1281-16AUR <sup>(4)</sup> ATmega1281-16MU ATmega1281-16MUR <sup>(4)</sup>	64A 64A 64M2 64M2	

- Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. See [“Speed Grades” on page 357](#).
  3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  4. Tape & Reel.

Package Type	
<b>64A</b>	64-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>64M2</b>	64-pad, 9mm × 9mm × 1.0mm Body, Quad Flat No-lead/Micro Lead Frame Package (QFN/MLF)

## 9.4 ATmega2560

Speed [MHz] <sup>(2)</sup>	Power Supply	Ordering Code	Package <sup>(1)(3)</sup>	Operation Range
8	1.8V - 5.5V	ATmega2560V-8AU	100A	Industrial (-40°C to 85°C)
		ATmega2560V-8AUR <sup>(4)</sup>	100A	
		ATmega2560V-8CU	100C1	
		ATmega2560V-8CUR <sup>(4)</sup>	100C1	
16	4.5V - 5.5V	ATmega2560-16AU	100A	
		ATmega2560-16AUR <sup>(4)</sup>	100A	
		ATmega2560-16CU	100C1	
		ATmega2560-16CUR <sup>(4)</sup>	100C1	

- Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. See [“Speed Grades” on page 357](#).
  3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  4. Tape & Reel.

Package Type	
<b>100A</b>	100-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>100C1</b>	100-ball, Chip Ball Grid Array (CBGA)

## 9.5 ATmega2561

Speed [MHz] <sup>(2)</sup>	Power Supply	Ordering Code	Package <sup>(1)(3)</sup>	Operation Range
8	1.8V - 5.5V	ATmega2561V-8AU ATmega2561V-8AUR <sup>(4)</sup> ATmega2561V-8MU ATmega2561V-8MUR <sup>(4)</sup>	64A 64A 64M2 64M2	Industrial (-40°C to 85°C)
16	4.5V - 5.5V	ATmega2561-16AU ATmega2561-16AUR <sup>(4)</sup> ATmega2561-16MU ATmega2561-16MUR <sup>(4)</sup>	64A 64A 64M2 64M2	

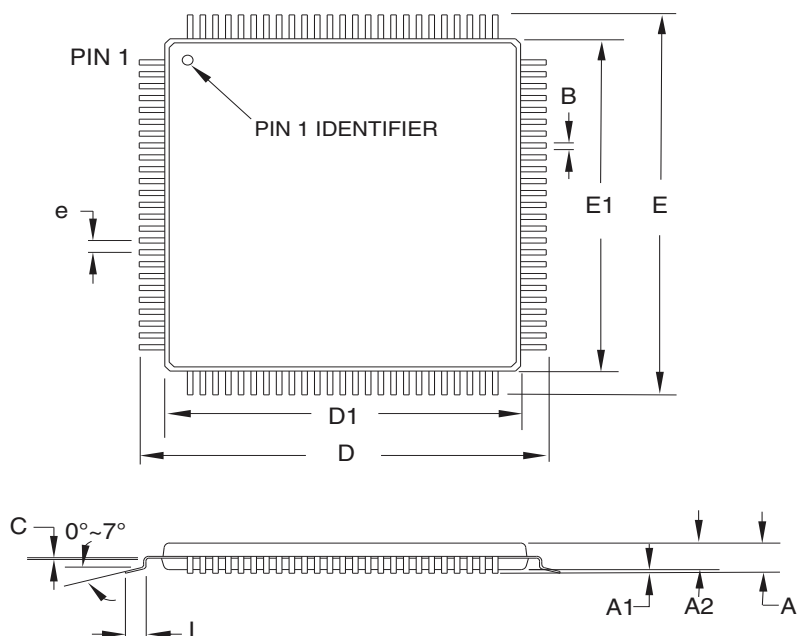
- Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. See [“Speed Grades” on page 357](#).
  3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  4. Tape & Reel.

Package Type	
<b>64A</b>	64-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>64M2</b>	64-pad, 9mm × 9mm × 1.0mm Body, Quad Flat No-lead/Micro Lead Frame Package (QFN/MLF)



## 10. Packaging Information

### 10.1 100A



#### COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	—	0.27	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.50 TYP			

#### Notes:

1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

2010-10-20

<b>Atmel</b> Package Drawing Contact: <a href="mailto:packagedrawings@atmel.com">packagedrawings@atmel.com</a>	TITLE	DRAWING NO.	REV.
	<b>100A</b> , 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	D

## 11. Errata

### 11.1 ATmega640 rev. B

- Inaccurate ADC conversion in differential mode with 200× gain
- High current consumption in sleep mode

#### 1. Inaccurate ADC conversion in differential mode with 200× gain

With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

##### Problem Fix/Workaround

None.

#### 2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

##### Problem Fix/Workaround

Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

### 11.2 ATmega640 rev. A

- Inaccurate ADC conversion in differential mode with 200× gain
- High current consumption in sleep mode

#### 1. Inaccurate ADC conversion in differential mode with 200× gain

With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

##### Problem Fix/Workaround

None.

#### 2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

##### Problem Fix/Workaround

Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

### 11.3 ATmega1280 rev. B

- High current consumption in sleep mode

#### 1. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

##### Problem Fix/Workaround

Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

### 11.4 ATmega1280 rev. A

- Inaccurate ADC conversion in differential mode with 200× gain
- High current consumption in sleep mode

#### 1. Inaccurate ADC conversion in differential mode with 200× gain

With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

## 11.10 ATmega2560 rev. C

- High current consumption in sleep mode

### 1. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

#### Problem Fix/Workaround

Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

## 11.11 ATmega2560 rev. B

Not sampled.

## 11.12 ATmega2560 rev. A

- Non-Read-While-Write area of flash not functional
- Part does not work under 2.4 volts
- Incorrect ADC reading in differential mode
- Internal ADC reference has too low value
- IN/OUT instructions may be executed twice when Stack is in external RAM
- EEPROM read from application code does not work in Lock Bit Mode 3

### 1. Non-Read-While-Write area of flash not functional

The Non-Read-While-Write area of the flash is not working as expected. The problem is related to the speed of the part when reading the flash of this area.

#### Problem Fix/Workaround

- Only use the first 248K of the flash.

- If boot functionality is needed, run the code in the Non-Read-While-Write area at maximum 1/4th of the maximum frequency of the device at any given voltage. This is done by writing the CLKPR register before entering the boot section of the code.

### 2. Part does not work under 2.4 volts

The part does not execute code correctly below 2.4 volts.

#### Problem Fix/Workaround

Do not use the part at voltages below 2.4 volts.

### 3. Incorrect ADC reading in differential mode

The ADC has high noise in differential mode. It can give up to 7 LSB error.

#### Problem Fix/Workaround

Use only the 7 MSB of the result when using the ADC in differential mode.

### 4. Internal ADC reference has too low value

The internal ADC reference has a value lower than specified.

#### Problem Fix/Workaround

- Use AVCC or external reference.

- The actual value of the reference can be measured by applying a known voltage to the ADC when using the internal reference. The result when doing later conversions can then be calibrated.

## 5. IN/OUT instructions may be executed twice when Stack is in external RAM

If either an IN or an OUT instruction is executed directly before an interrupt occurs and the stack pointer is located in external ram, the instruction will be executed twice. In some cases this will cause a problem, for example:

- If reading SREG it will appear that the I-flag is cleared.
- If writing to the PIN registers, the port will toggle twice.
- If reading registers with interrupt flags, the flags will appear to be cleared.

### Problem Fix/Workaround

There are two application workarounds, where selecting one of them, will be omitting the issue:

- Replace IN and OUT with LD/LDS/LDD and ST/STS/STD instructions.
- Use internal RAM for stack pointer.

## 6. EEPROM read from application code does not work in Lock Bit Mode 3

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

### Problem Fix/Workaround

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

## 11.13 ATmega2561 rev. F

- ADC differential input amplification by 46dB (200x) not functional

### 1. ADC differential input amplification by 46dB (200x) not functional

#### Problem Fix/Workaround

None.

## 11.14 ATmega2561 rev. E

No known errata.

## 11.15 ATmega2561 rev. D

Not sampled.

## 11.16 ATmega2561 rev. C

- High current consumption in sleep mode.

### 1. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

#### Problem Fix/Workaround

Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

## 11.17 ATmega2561 rev. B

Not sampled.

## 11.18 ATmega2561 rev. A

- **Non-Read-While-Write area of flash not functional**
- **Part does not work under 2.4 Volts**
- **Incorrect ADC reading in differential mode**
- **Internal ADC reference has too low value**
- **IN/OUT instructions may be executed twice when Stack is in external RAM**
- **EEPROM read from application code does not work in Lock Bit Mode 3**

### 1. **Non-Read-While-Write area of flash not functional**

The Non-Read-While-Write area of the flash is not working as expected. The problem is related to the speed of the part when reading the flash of this area.

#### **Problem Fix/Workaround**

- Only use the first 248K of the flash.

- If boot functionality is needed, run the code in the Non-Read-While-Write area at maximum 1/4th of the maximum frequency of the device at any given voltage. This is done by writing the CLKPR register before entering the boot section of the code.

### 2. **Part does not work under 2.4 volts**

The part does not execute code correctly below 2.4 volts.

#### **Problem Fix/Workaround**

Do not use the part at voltages below 2.4 volts.

### 3. **Incorrect ADC reading in differential mode**

The ADC has high noise in differential mode. It can give up to 7 LSB error.

#### **Problem Fix/Workaround**

Use only the 7 MSB of the result when using the ADC in differential mode.

### 4. **Internal ADC reference has too low value**

The internal ADC reference has a value lower than specified.

#### **Problem Fix/Workaround**

- Use AVCC or external reference.

- The actual value of the reference can be measured by applying a known voltage to the ADC when using the internal reference. The result when doing later conversions can then be calibrated.

### 5. **IN/OUT instructions may be executed twice when Stack is in external RAM**

If either an IN or an OUT instruction is executed directly before an interrupt occurs and the stack pointer is located in external ram, the instruction will be executed twice. In some cases this will cause a problem, for example:

- If reading SREG it will appear that the I-flag is cleared.

- If writing to the PIN registers, the port will toggle twice.

- If reading registers with interrupt flags, the flags will appear to be cleared.

#### **Problem Fix/Workaround**

There are two application workarounds, where selecting one of them, will be omitting the issue:

- Replace IN and OUT with LD/LDS/LDD and ST/STS/STD instructions.