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What is "Embedded - Microcontrollers"?

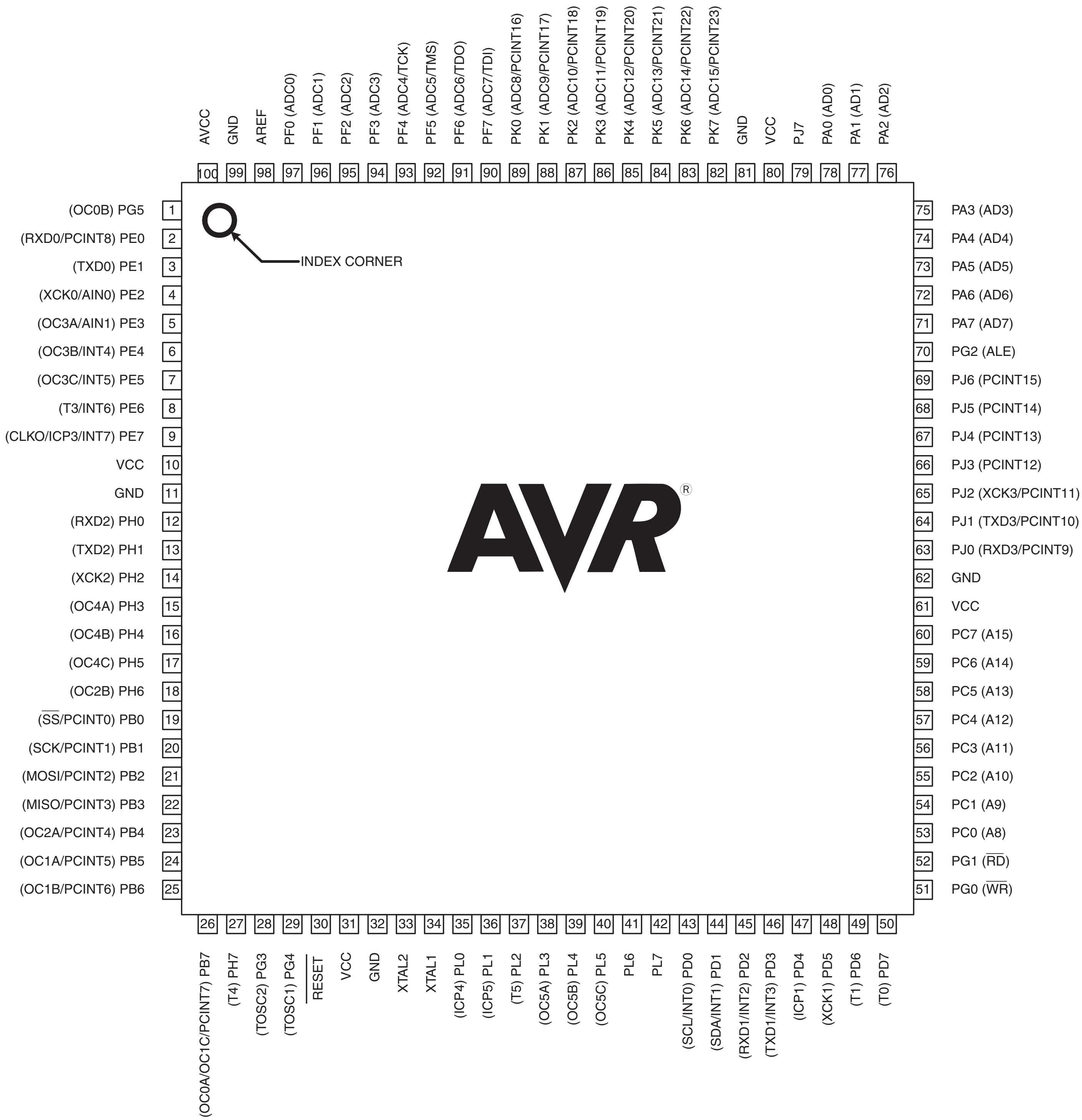
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	8MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega1280v-8au

1. Pin Configurations

Figure 1-1. TQFP-pinout ATmega640/1280/2560

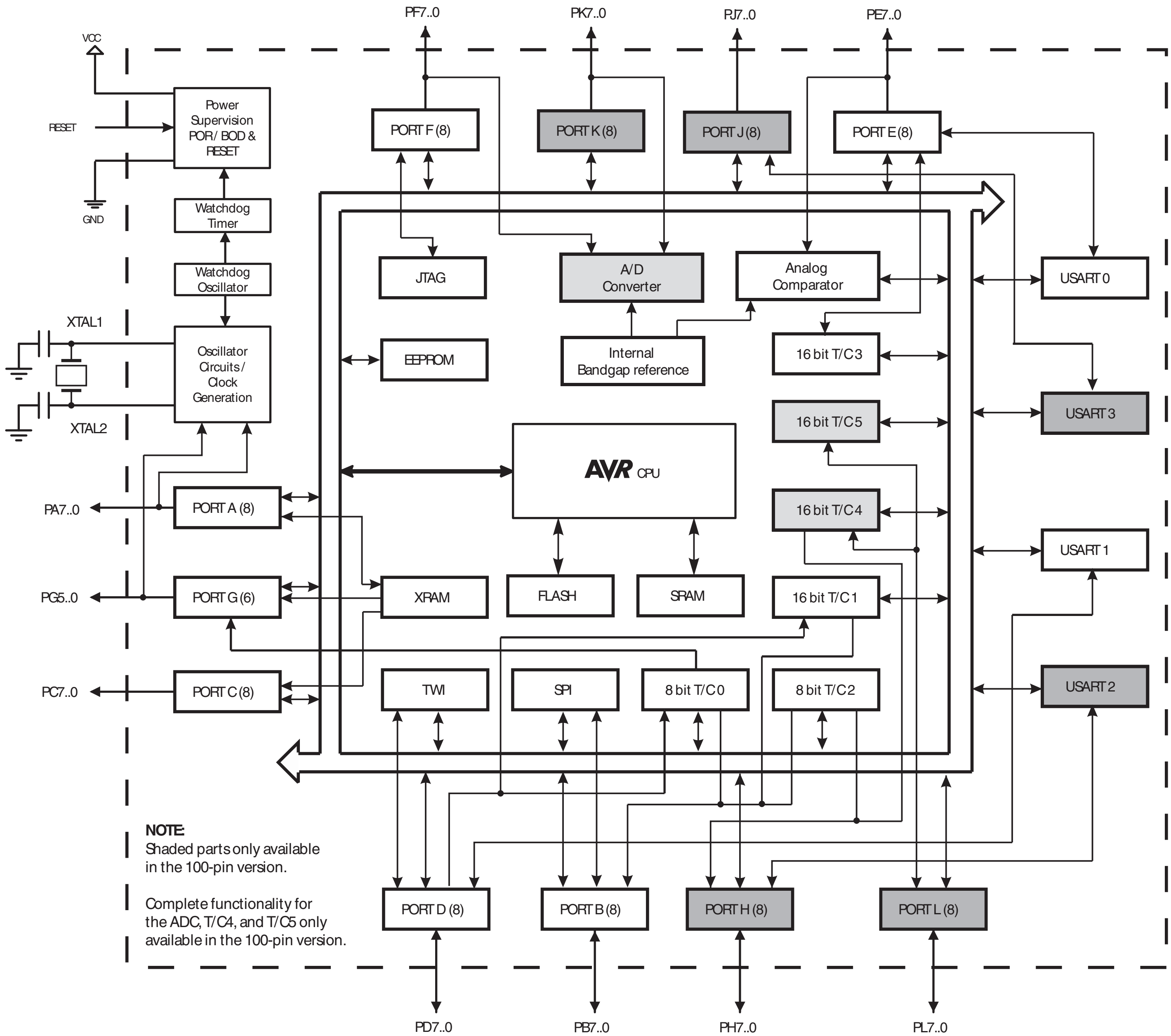


2. Overview

The ATmega640/1280/1281/2560/2561 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega640/1280/1281/2560/2561 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The Atmel® AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega640/1280/1281/2560/2561 provides the following features: 64K/128K/256K bytes of In-System Programmable Flash with Read-While-Write capabilities, 4Kbytes EEPROM, 8Kbytes SRAM, 54/86 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), six flexible Timer/Counters with compare modes and PWM, four USARTs, a byte oriented 2-wire Serial Interface, a 16-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE® std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offersrobust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using the Atmel high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega640/1280/1281/2560/2561 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega640/1280/1281/2560/2561 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Comparison Between ATmega1281/2561 and ATmega640/1280/2560

Each device in the ATmega640/1280/1281/2560/2561 family differs only in memory size and number of pins. Table 2-1 summarizes the different configurations for the six devices.

Table 2-1. Configuration Summary

Device	Flash	EEPROM	RAM	General Purpose I/O pins	16 bits resolution PWM channels	Serial USARTs	ADC Channels
ATmega640	64KB	4KB	8KB	86	12	4	16
ATmega1280	128KB	4KB	8KB	86	12	4	16
ATmega1281	128KB	4KB	8KB	54	6	2	8
ATmega2560	256KB	4KB	8KB	86	12	4	16
ATmega2561	256KB	4KB	8KB	54	6	2	8

2.3 Pin Descriptions

2.3.1 VCC

Digital supply voltage.

2.3.2 GND

Ground.

2.3.3 Port A (PA7..PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega640/1280/1281/2560/2561 as listed on page 75.

2.3.4 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the ATmega640/1280/1281/2560/2561 as listed on page 76.

2.3.5 Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmega640/1280/1281/2560/2561 as listed on page 79.

2.3.12 Port K (PK7..PK0)

Port K serves as analog inputs to the A/D Converter.

Port K is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port K output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port K pins that are externally pulled low will source current if the pull-up resistors are activated. The Port K pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port K also serves the functions of various special features of the ATmega640/1280/2560 as listed on page 92.

2.3.13 Port L (PL7..PL0)

Port L is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port L output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port L pins that are externally pulled low will source current if the pull-up resistors are activated. The Port L pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port L also serves the functions of various special features of the ATmega640/1280/2560 as listed on page 94.

2.3.14 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in "System and Reset Characteristics" on page 360. Shorter pulses are not guaranteed to generate a reset.

2.3.15 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.16 XTAL2

Output from the inverting Oscillator amplifier.

2.3.17 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.18 AREF

This is the analog reference pin for the A/D Converter.

3. Resources

A comprehensive set of development tools and application notes, and datasheets are available for download on http://www.atmel.com/avr.

4. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

5. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 ppm over 20 years at 85°C or 100 years at 25°C.

6. Capacitive touch sensing

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

7. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x1FF)	Reserved	-	-	-	-	-	-	-	-	
...	Reserved	-	-	-	-	-	-	-	-	
(0x13F)	Reserved									
(0x13E)	Reserved									
(0x13D)	Reserved									
(0x13C)	Reserved									
(0x13B)	Reserved									
(0x13A)	Reserved									
(0x139)	Reserved									
(0x138)	Reserved									
(0x137)	Reserved									
(0x136)	UDR3	USART3 I/O Data Register								page 218
(0x135)	UBRR3H	-	-	-	-	USART3 Baud Rate Register High Byte				page 222
(0x134)	UBRR3L	USART3 Baud Rate Register Low Byte								page 222
(0x133)	Reserved	-	-	-	-	-	-	-	-	
(0x132)	UCSR3C	UMSEL31	UMSEL30	UPM31	UPM30	USBS3	UCSZ31	UCSZ30	UCPOL3	page 235
(0x131)	UCSR3B	RXCIE3	TXCIE3	UDRIE3	RXEN3	TXEN3	UCSZ32	RXB83	TXB83	page 234
(0x130)	UCSR3A	RXC3	TXC3	UDRE3	FE3	DOR3	UPE3	U2X3	MPCM3	page 233
(0x12F)	Reserved	-	-	-	-	-	-	-	-	
(0x12E)	Reserved	-	-	-	-	-	-	-	-	
(0x12D)	OCR5CH	Timer/Counter5 - Output Compare Register C High Byte								page 160
(0x12C)	OCR5CL	Timer/Counter5 - Output Compare Register C Low Byte								page 160
(0x12B)	OCR5BH	Timer/Counter5 - Output Compare Register B High Byte								page 160
(0x12A)	OCR5BL	Timer/Counter5 - Output Compare Register B Low Byte								page 160
(0x129)	OCR5AH	Timer/Counter5 - Output Compare Register A High Byte								page 160
(0x128)	OCR5AL	Timer/Counter5 - Output Compare Register A Low Byte								page 160
(0x127)	ICR5H	Timer/Counter5 - Input Capture Register High Byte								page 161
(0x126)	ICR5L	Timer/Counter5 - Input Capture Register Low Byte								page 161
(0x125)	TCNT5H	Timer/Counter5 - Counter Register High Byte								page 158
(0x124)	TCNT5L	Timer/Counter5 - Counter Register Low Byte								page 158
(0x123)	Reserved	-	-	-	-	-	-	-	-	
(0x122)	TCCR5C	FOC5A	FOC5B	FOC5C	-	-	-	-	-	page 157
(0x121)	TCCR5B	ICNC5	ICES5	-	WGM53	WGM52	CS52	CS51	CS50	page 156
(0x120)	TCCR5A	COM5A1	COM5A0	COM5B1	COM5B0	COM5C1	COM5C0	WGM51	WGM50	page 154
(0x11F)	Reserved	-	-	-	-	-	-	-	-	
(0x11E)	Reserved	-	-	-	-	-	-	-	-	
(0x11D)	Reserved	-	-	-	-	-	-	-	-	
(0x11C)	Reserved	-	-	-	-	-	-	-	-	
(0x11B)	Reserved	-	-	-	-	-	-	-	-	
(0x11A)	Reserved	-	-	-	-	-	-	-	-	
(0x119)	Reserved	-	-	-	-	-	-	-	-	
(0x118)	Reserved	-	-	-	-	-	-	-	-	
(0x117)	Reserved	-	-	-	-	-	-	-	-	
(0x116)	Reserved	-	-	-	-	-	-	-	-	
(0x115)	Reserved	-	-	-	-	-	-	-	-	
(0x114)	Reserved	-	-	-	-	-	-	-	-	
(0x113)	Reserved	-	-	-	-	-	-	-	-	
(0x112)	Reserved	-	-	-	-	-	-	-	-	
(0x111)	Reserved	-	-	-	-	-	-	-	-	
(0x110)	Reserved	-	-	-	-	-	-	-	-	
(0x10F)	Reserved	-	-	-	-	-	-	-	-	
(0x10E)	Reserved	-	-	-	-	-	-	-	-	
(0x10D)	Reserved	-	-	-	-	-	-	-	-	
(0x10C)	Reserved	-	-	-	-	-	-	-	-	
(0x10B)	PORTL	PORTL7	PORTL6	PORTL5	PORTL4	PORTL3	PORTL2	PORTL1	PORTL0	page 100
(0x10A)	DDRL	DDL7	DDL6	DDL5	DDL4	DDL3	DDL2	DDL1	DDL0	page 100
(0x109)	PINL	PINL7	PINL6	PINL5	PINL4	PINL3	PINL2	PINL1	PINL0	page 100
(0x108)	PORTK	PORTK7	PORTK6	PORTK5	PORTK4	PORTK3	PORTK2	PORTK1	PORTK0	page 99
(0x107)	DDRK	DDK7	DDK6	DDK5	DDK4	DDK3	DDK2	DDK1	DDK0	page 99
(0x106)	PINK	PINK7	PINK6	PINK5	PINK4	PINK3	PINK2	PINK1	PINK0	page 99
(0x105)	PORTJ	PORTJ7	PORTJ6	PORTJ5	PORTJ4	PORTJ3	PORTJ2	PORTJ1	PORTJ0	page 99
(0x104)	DDRJ	DDJ7	DDJ6	DDJ5	DDJ4	DDJ3	DDJ2	DDJ1	DDJ0	page 99
(0x103)	PINJ	PINJ7	PINJ6	PINJ5	PINJ4	PINJ3	PINJ2	PINJ1	PINJ0	page 99
(0x102)	PORTH	PORTH7	PORTH6	PORTH5	PORTH4	PORTH3	PORTH2	PORTH1	PORTH0	page 98
(0x101)	DDRH	DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0	page 99

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	page 261
(0xBB)	TWDR	2-wire Serial Interface Data Register								page 263
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	page 263
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	page 262
(0xB8)	TWBR	2-wire Serial Interface Bit Rate Register								page 261
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	page 179
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	OCR2B	Timer/Counter2 Output Compare Register B								page 186
(0xB3)	OCR2A	Timer/Counter2 Output Compare Register A								page 186
(0xB2)	TCNT2	Timer/Counter2 (8 Bit)								page 186
(0xB1)	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20	page 185
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20	page 186
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	OCR4CH	Timer/Counter4 - Output Compare Register C High Byte								page 160
(0xAC)	OCR4CL	Timer/Counter4 - Output Compare Register C Low Byte								page 160
(0xAB)	OCR4BH	Timer/Counter4 - Output Compare Register B High Byte								page 160
(0xAA)	OCR4BL	Timer/Counter4 - Output Compare Register B Low Byte								page 160
(0xA9)	OCR4AH	Timer/Counter4 - Output Compare Register A High Byte								page 159
(0xA8)	OCR4AL	Timer/Counter4 - Output Compare Register A Low Byte								page 159
(0xA7)	ICR4H	Timer/Counter4 - Input Capture Register High Byte								page 161
(0xA6)	ICR4L	Timer/Counter4 - Input Capture Register Low Byte								page 161
(0xA5)	TCNT4H	Timer/Counter4 - Counter Register High Byte								page 158
(0xA4)	TCNT4L	Timer/Counter4 - Counter Register Low Byte								page 158
(0xA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	TCCR4C	FOC4A	FOC4B	FOC4C	-	-	-	-	-	page 157
(0xA1)	TCCR4B	ICNC4	ICES4	-	WGM43	WGM42	CS42	CS41	CS40	page 156
(0xA0)	TCCR4A	COM4A1	COM4A0	COM4B1	COM4B0	COM4C1	COM4C0	WGM41	WGM40	page 154
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	OCR3CH	Timer/Counter3 - Output Compare Register C High Byte								page 159
(0x9C)	OCR3CL	Timer/Counter3 - Output Compare Register C Low Byte								page 159
(0x9B)	OCR3BH	Timer/Counter3 - Output Compare Register B High Byte								page 159
(0x9A)	OCR3BL	Timer/Counter3 - Output Compare Register B Low Byte								page 159
(0x99)	OCR3AH	Timer/Counter3 - Output Compare Register A High Byte								page 159
(0x98)	OCR3AL	Timer/Counter3 - Output Compare Register A Low Byte								page 159
(0x97)	ICR3H	Timer/Counter3 - Input Capture Register High Byte								page 161
(0x96)	ICR3L	Timer/Counter3 - Input Capture Register Low Byte								page 161
(0x95)	TCNT3H	Timer/Counter3 - Counter Register High Byte								page 158
(0x94)	TCNT3L	Timer/Counter3 - Counter Register Low Byte								page 158
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	TCCR3C	FOC3A	FOC3B	FOC3C	-	-	-	-	-	page 157
(0x91)	TCCR3B	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30	page 156
(0x90)	TCCR3A	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30	page 154
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	OCR1CH	Timer/Counter1 - Output Compare Register C High Byte								page 159
(0x8C)	OCR1CL	Timer/Counter1 - Output Compare Register C Low Byte								page 159
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								page 159
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								page 159
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								page 159
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								page 159
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								page 160
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								page 160
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								page 158
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								page 158
(0x83)	Reserved	-	-	-	-	-	-	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B	FOC1C	-	-	-	-	-	page 157
(0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	page 156
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	page 154
(0x7F)	DIDR1	-	-	-	-	-	-	AIN1D	AIN0D	page 267
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	page 287
(0x7D)	DIDR2	ADC15D	ADC14D	ADC13D	ADC12D	ADC11D	ADC10D	ADC9D	ADC8D	page 288
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	page 281
(0x7B)	ADCSRB	-	ACME	-	-	MUX5	ADTS2	ADTS1	ADTS0	page 266, 282, 287
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 285
(0x79)	ADCH	ADC Data Register High byte								page 286

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x14 (0x34)	PORTG	-	-	PORTG5	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	page 98
0x13 (0x33)	DDRG	-	-	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	page 98
0x12 (0x32)	PING	-	-	PING5	PING4	PING3	PING2	PING1	PING0	page 98
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	page 97
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	page 98
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	page 98
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	page 97
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	page 97
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	page 98
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 97
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 97
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 97
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	page 97
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	page 97
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	page 97
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 96
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 96
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 96
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	page 96
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	page 96
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	page 96

Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O registers as data space using LD and ST instructions, $20 must be added to these addresses. The ATmega640/1280/1281/2560/2561 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from $60 - $1FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

Note: EICALL and EIJMP do not exist in ATmega640/1280/1281.
ELPM does not exist in ATmega640.

9.2 ATmega1280

Speed [MHz][2]	Power Supply	Ordering Code	Package[1][3]	Operation Range
8	1.8V - 5.5V	ATmega1280V-8AU ATmega1280V-8AUR[4] ATmega1280V-8CU ATmega1280V-8CUR[4]	100A 100A 100C1 100C1	Industrial (-40°C to 85°C)
16	2.7V - 5.5V	ATmega1280-16AU ATmega1280-16AUR[4] ATmega1280-16CU ATmega1280-16CUR[4]	100A 100A 100C1 100C1	

Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. See "Speed Grades" on page 357.
3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
4. Tape & Reel.

Package Type	
100A	100-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
100C1	100-ball, Chip Ball Grid Array (CBGA)

9.4 ATmega2560

Speed [MHz][2]	Power Supply	Ordering Code	Package[1][3]	Operation Range
8	1.8V - 5.5V	ATmega2560V-8AU ATmega2560V-8AUR[4] ATmega2560V-8CU ATmega2560V-8CUR[4]	100A 100A 100C1 100C1	Industrial (-40°C to 85°C)
16	4.5V - 5.5V	ATmega2560-16AU ATmega2560-16AUR[4] ATmega2560-16CU ATmega2560-16CUR[4]	100A 100A 100C1 100C1	

Notes:
1. This device can also be supplied in wafer form. Contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. See "Speed Grades" on page 357.
3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
4. Tape & Reel.

Package Type	
100A	100-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
100C1	100-ball, Chip Ball Grid Array (CBGA)

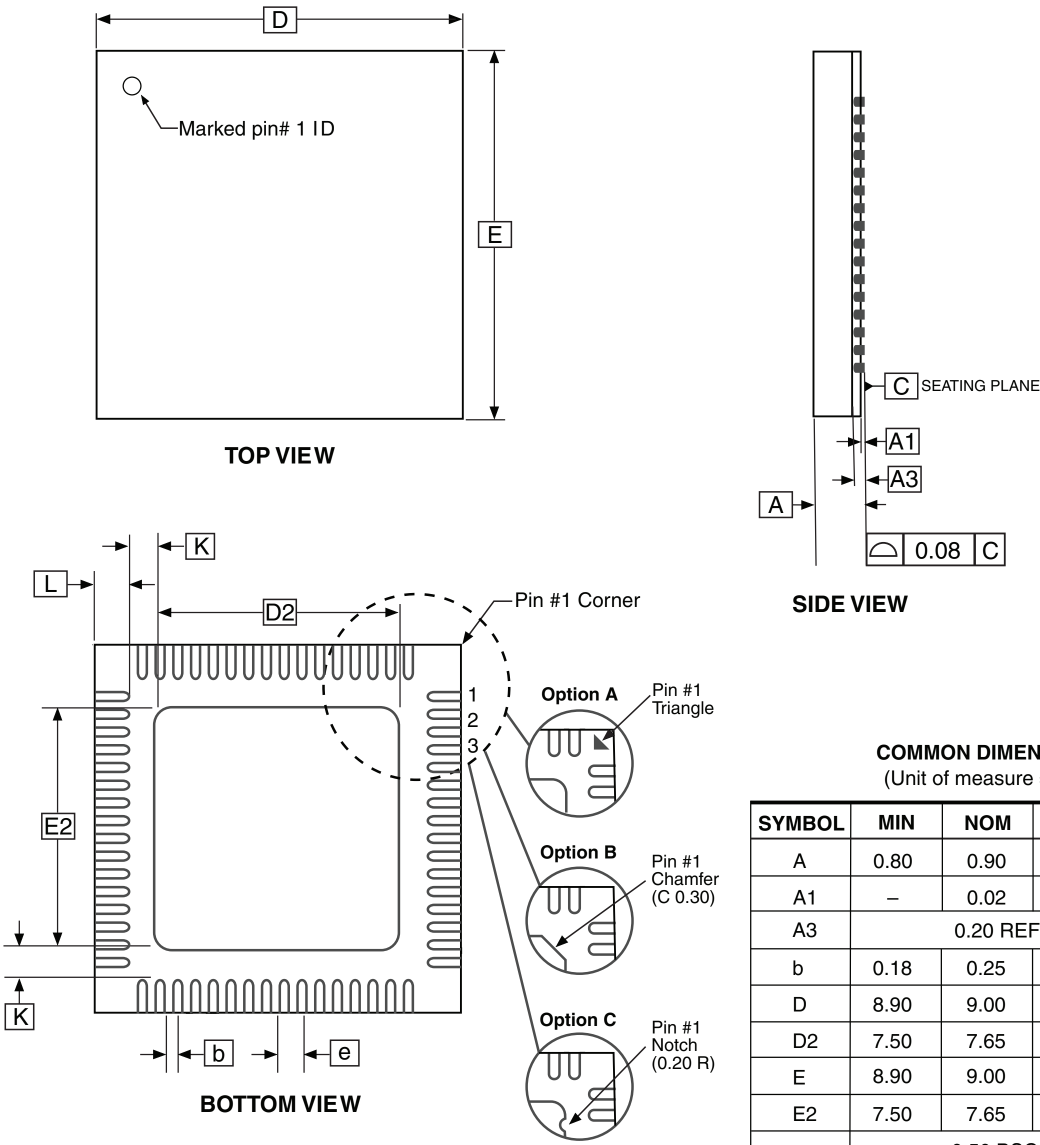
9.5 ATmega2561

Speed [MHz][2]	Power Supply	Ordering Code	Package[1][3]	Operation Range
8	1.8V - 5.5V	ATmega2561V-8AU ATmega2561V-8AUR[4] ATmega2561V-8MU ATmega2561V-8MUR[4]	64A 64A 64M2 64M2	Industrial (-40°C to 85°C)
16	4.5V - 5.5V	ATmega2561-16AU ATmega2561-16AUR[4] ATmega2561-16MU ATmega2561-16MUR[4]	64A 64A 64M2 64M2	

Notes:
1. This device can also be supplied in wafer form.Contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. See "Speed Grades" on page 357.
3. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
4. Tape & Reel.

Package Type	
64A	64-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
64M2	64-pad, 9mm × 9mm × 1.0mm Body, Quad Flat No-lead/Micro Lead Frame Package (QFN/MLF)

10.4 64M2



COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	7.50	7.65	7.80	
E	8.90	9.00	9.10	
E2	7.50	7.65	7.80	
e		0.50 BSC		
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	

Notes: 1. JEDEC Standard MO-220, (SAW Singulation) fig . 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2014-02-12

Atmel 2325 Orchard Parkway San Jose, CA 95131	TITLE **64M2**, 64-pad, 9 x 9 x 1.0mm Bod y, Lead Pitch 0.50mm , 7.65mm Exposed Pad, Micro Lead Frame Package (MLF)	DRAWING NO. 64M2	REV. E

11. Errata

11.1 ATmega640 rev. B

- **Inaccurate ADC conversion in differential mode with 200× gain**
- **High current consumption in sleep mode**

1. **Inaccurate ADC conversion in differential mode with 200× gain**
   With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

   Problem Fix/Workaround
   None.

2. **High current consumption in sleep mode**
   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround
   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.2 ATmega640 rev. A

- **Inaccurate ADC conversion in differential mode with 200× gain**
- **High current consumption in sleep mode**

1. **Inaccurate ADC conversion in differential mode with 200× gain**
   With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

   Problem Fix/Workaround
   None.

2. **High current consumption in sleep mode**
   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround
   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.3 ATmega1280 rev. B

- **High current consumption in sleep mode**

1. **High current consumption in sleep mode**
   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround
   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.4 ATmega1280 rev. A

- **Inaccurate ADC conversion in differential mode with 200× gain**
- **High current consumption in sleep mode**

1. **Inaccurate ADC conversion in differential mode with 200× gain**
   With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

Problem Fix/Workaround

None.

2. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround

   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.5 ATmega1281 rev. B

- **High current consumption in sleep mode**

1. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround

   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.6 ATmega1281 rev. A

- **Inaccurate ADC conversion in differential mode with 200× gain**
- **High current consumption in sleep mode**

1. **Inaccurate ADC conversion in differential mode with 200× gain**

   With AVCC <3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

   Problem Fix/Workaround

   None.

2. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround

   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.7 ATmega2560 rev. F

- **ADC differential input amplification by 46dB (200x) not functional**

1. **ADC differential input amplification by 46dB (200x) not functional**

   Problem Fix/Workaround

   None.

11.8 ATmega2560 rev. E

No known errata.

11.9 ATmega2560 rev. D

Not sampled.

11.10 ATmega2560 rev. C

- **High current consumption in sleep mode**

1. **High current consumption in sleep mode**

   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround

   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.11 ATmega2560 rev. B

Not sampled.

11.12 ATmega2560 rev. A

- **Non-Read-While-Write area of flash not functional**
- **Part does not work under 2.4 volts**
- **Incorrect ADC reading in differential mode**
- **Internal ADC reference has too low value**
- **IN/OUT instructions may be executed twice when Stack is in external RAM**
- **EEPROM read from application code does not work in Lock Bit Mode 3**

1. **Non-Read-While-Write area of flash not functional**

   The Non-Read-While-Write area of the flash is not working as expected. The problem is related to the speed of the part when reading the flash of this area.

   Problem Fix/Workaround

   - Only use the first 248K of the flash.

   - If boot functionality is needed, run the code in the Non-Read-While-Write area at maximum 1/4th of the maximum frequency of the device at any given voltage. This is done by writing the CLKPR register before entering the boot section of the code.

2. **Part does not work under 2.4 volts**

   The part does not execute code correctly below 2.4 volts.

   Problem Fix/Workaround

   Do not use the part at voltages below 2.4 volts.

3. **Incorrect ADC reading in differential mode**

   The ADC has high noise in differential mode. It can give up to 7 LSB error.

   Problem Fix/Workaround

   Use only the 7 MSB of the result when using the ADC in differential mode.

4. **Internal ADC reference has too low value**

   The internal ADC reference has a value lower than specified.

   Problem Fix/Workaround

   - Use AVCC or external reference.

   - The actual value of the reference can be measured by applying a known voltage to the ADC when using the internal reference. The result when doing later conversions can then be calibrated.

5. **IN/OUT instructions may be executed twice when Stack is in external RAM**
   If either an IN or an OUT instruction is executed directly before an interrupt occurs and the stack pointer is located in external ram, the instruction will be executed twice. In some cases this will cause a problem, for example:

   - If reading SREG it will appear that the I-flag is cleared.

   - If writing to the PIN registers, the port will toggle twice.

   - If reading registers with interrupt flags, the flags will appear to be cleared.

   Problem Fix/Workaround
   There are two application workarounds, where selecting one of them, will be omitting the issue:

   - Replace IN and OUT with LD/LDS/LDD and ST/STS/STD instructions.

   - Use internal RAM for stack pointer.

6. **EEPROM read from application code does not work in Lock Bit Mode 3**
   When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

   Problem Fix/Workaround
   Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

11.13 ATmega2561 rev. F

- **ADC differential input amplification by 46dB (200x) not functional**

1. **ADC differential input amplification by 46dB (200x) not functional**
   Problem Fix/Workaround
   None.

11.14 ATmega2561 rev. E

No known errata.

11.15 ATmega2561 rev. D

Not sampled.

11.16 ATmega2561 rev. C

- **High current consumption in sleep mode.**

1. **High current consumption in sleep mode**
   If a pending interrupt cannot wake the part up from the selected sleep mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

   Problem Fix/Workaround
   Before entering sleep, interrupts not used to wake the part from the sleep mode should be disabled.

11.17 ATmega2561 rev. B

Not sampled.

11.18 ATmega2561 rev. A

- **Non-Read-While-Write area of flash not functional**
- **Part does not work under 2.4 Volts**
- **Incorrect ADC reading in differential mode**
- **Internal ADC reference has too low value**
- **IN/OUT instructions may be executed twice when Stack is in external RAM**
- **EEPROM read from application code does not work in Lock Bit Mode 3**

1. Non-Read-While-Write area of flash not functional

The Non-Read-While-Write area of the flash is not working as expected. The problem is related to the speed of the part when reading the flash of this area.

Problem Fix/Workaround

- Only use the first 248K of the flash.

- If boot functionality is needed, run the code in the Non-Read-While-Write area at maximum 1/4th of the maximum frequency of the device at any given voltage. This is done by writing the CLKPR register before entering the boot section of the code.

2. Part does not work under 2.4 volts

The part does not execute code correctly below 2.4 volts.

Problem Fix/Workaround

Do not use the part at voltages below 2.4 volts.

3. Incorrect ADC reading in differential mode

The ADC has high noise in differential mode. It can give up to 7 LSB error.

Problem Fix/Workaround

Use only the 7 MSB of the result when using the ADC in differential mode.

4. Internal ADC reference has too low value

The internal ADC reference has a value lower than specified.

Problem Fix/Workaround

- Use AVCC or external reference.

- The actual value of the reference can be measured by applying a known voltage to the ADC when using the internal reference. The result when doing later conversions can then be calibrated.

5. IN/OUT instructions may be executed twice when Stack is in external RAM

If either an IN or an OUT instruction is executed directly before an interrupt occurs and the stack pointer is located in external ram, the instruction will be executed twice. In some cases this will cause a problem, for example:

- If reading SREG it will appear that the I-flag is cleared.

- If writing to the PIN registers, the port will toggle twice.

- If reading registers with interrupt flags, the flags will appear to be cleared.

Problem Fix/Workaround

There are two application workarounds, where selecting one of them, will be omitting the issue:

- Replace IN and OUT with LD/LDS/LDD and ST/STS/STD instructions.

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