E·XFL



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f629t-i-md

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION. QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV ISO/TS 16949:2002

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.



ISBN: 978-1-60932-160-4

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Pin Diagrams



NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC12F629/675. Additional information may be found in the PIC[®] Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this Data Sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC12F629 and PIC12F675 devices are covered by this Data Sheet. They are identical, except the PIC12F675 has a 10-bit A/D converter. They come in 8-pin PDIP, SOIC, MLF-S and DFN packages. Figure 1-1 shows a block diagram of the PIC12F629/ 675 devices. Table 1-1 shows the pinout description.



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Page
Bank 1											
80h	INDF ⁽¹⁾	Addressing	this Location	uses Conter	nts of FSR to	Address Dat	ta Memory			0000 0000	20,61
81h	OPTION_REG	GPPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	14,31
82h	PCL	Program Co	gram Counter's (PC) Least Significant Byte				0000 0000	19			
83h	STATUS	IRP ⁽²⁾	RP1 ⁽²⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	14
84h	FSR	Indirect Data	a Memory Ad	dress Pointe	er				•	xxxx xxxx	20
85h	TRISIO	_	—	TRISI05	TRISIO4	TRISIO3	TRISIO2	TRISI01	TRISIO0	11 1111	21
86h	_	Unimpleme	nted	•			•	•	•	_	_
87h	_	Unimpleme	nted							—	_
88h	_	Unimpleme	nted							—	_
89h	_	Unimpleme	nted							—	—
8Ah	PCLATH	_	—	_	Write Buffer	for Upper 5	bits of Progra	am Counter		0 0000	19
8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	15
8Ch	PIE1	EEIE	ADIE	_	_	CMIE	_	_	TMR1IE	0000	16
8Dh	—	Unimpleme	nted							_	—
8Eh	PCON	—	_	—	—	—	—	POR	BOD	0x	18
8Fh	—	Unimpleme	nted							—	—
90h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	_	1000 00	18
91h	—	Unimpleme	nted							—	—
92h	—	Unimpleme	nted							—	—
93h	—	Unimpleme	nted							—	—
94h	—	Unimpleme	nted							—	—
95h	WPU	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	11 -111	21
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	00 0000	23
97h	—	Unimpleme	nted							—	—
98h	—	Unimplemen	nted							—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	42
9Ah	EEDATA	Data EEPR	OM Data Reg	gister						0000 0000	49
9Bh	EEADR	—	Data EEPR	OM Address	Register					-000 0000	49
9Ch	EECON1	_	—	_	—	WRERR	WREN	WR	RD	x000	50
9Dh	EECON2 ⁽¹⁾	EEPROM C	ontrol Regist	er 2							50
9Eh	ADRESL ⁽³⁾	Least Signif	icant 2 bits o	f the Left Shi	fted A/D Res	ult of 8 bits o	r the Right S	hifted Result		xxxx xxxx	44
9Fh	ANSEL ⁽³⁾	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	46,61

TABLE 2-1: SPECIAL FUNCTION REGISTERS SUMMARY (CONTINUED)

Legend: — = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: This is not a physical register.

2: These bits are reserved and should always be maintained as '0'.

3: PIC12F675 only.

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO port change and external GP2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh OR 8Bh)

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| GIE | PEIE | TOIE | INTE | GPIE | TOIF | INTF | GPIF |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	GIE: Global Interrupt Enable bit
	1 = Enables all unmasked interrupts
	0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit
	 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	T0IE: TMR0 Overflow Interrupt Enable bit
	 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt
bit 4	INTE: GP2/INT External Interrupt Enable bit
	1 = Enables the GP2/INT external interrupt
	0 = Disables the GP2/INT external interrupt
bit 3	GPIE: Port Change Interrupt Enable bit ⁽¹⁾
	1 = Enables the GPIO port change interrupt
	0 = Disables the GPIO port change interrupt
bit 2	T0IF: TMR0 Overflow Interrupt Flag bit ⁽²⁾
	1 = TMR0 register has overflowed (must be cleared in software)
	0 = IMRU register did not overflow
bit 1	INTF: GP2/INT External Interrupt Flag bit
	 1 = The GP2/INT external interrupt occurred (must be cleared in software) 0 = The GP2/INT external interrupt did not occur
bit 0	GPIF: Port Change Interrupt Flag bit
	 1 = When at least one of the GP5:GP0 pins changed state (must be cleared in software) 0 = None of the GP5:GP0 pins have changed state
Note 1:	IOC register must also be enabled to enable an interrupt-on-change.

2: T0IF bit is set when TIMER0 rolls over. TIMER0 is unchanged on Reset and should be initialized before clearing T0IF bit.

2.2.2.6 PCON Register

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Detect (BOD)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON Register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER (ADDRESS: 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-x
—	_	_	—	—	—	POR	BOD
bit 7			•	•			bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2	Unimplemented: Read as '0'
bit 1	POR: Power-on Reset Status bit
	 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
bit 0	BOD: Brown-out Detect Status bit
	 1 = No Brown-out Detect occurred 0 = A Brown-out Detect occurred (must be set in software after a Brown-out Detect occurs)

2.2.2.7 OSCCAL Register

The Oscillator Calibration register (OSCCAL) is used to calibrate the internal 4 MHz oscillator. It contains 6 bits to adjust the frequency up or down to achieve 4 MHz.

The OSCCAL register bits are shown in Register 2-7.

REGISTER 2-7: OSCCAL: OSCILLATOR CALIBRATION REGISTER (ADDRESS: 90h)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	_	_
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 7-2	CAL5:CAL0:	6-bit Signed O	scillator Calib	ration bits			
	111111 = Ma	ximum frequen	ю				

100000 =	Center	frequency

000000 = Minimum frequency

bit 1-0 Unimplemented: Read as '0'

2.3 PCL and PCLATH

The Program Counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the PC (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note, *"Implementing a Table Read"* (AN556).

2.3.2 STACK

The PIC12F629/675 family has an 8-level deep x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed, or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

3.0 GPIO PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Note:	Additional information on I/O ports may be
	found in the PIC [®] Mid-Range Reference
	Manual, (DS33023).

3.1 GPIO and the TRISIO Registers

GPIO is an 6-bit wide, bidirectional port. The corresponding data direction register is TRISIO. Setting a TRISIO bit (= 1) will make the corresponding GPIO pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISIO bit (= 0) will make the corresponding GPIO pin an output (i.e., put the contents of the output latch on the selected pin). The exception is GP3, which is input-only and its TRISIO bit will always read as '1'. Example 3-1 shows how to initialize GPIO.

Reading the GPIO register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the PORT data latch. GP3 reads '0' when MCLREN = 1.

The TRISIO register controls the direction of the GP pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO

register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

Note:	The ANSEL (9Fh) and CMCON (19h)
	registers (9Fh) must be initialized to
	configure an analog channel as a digital
	input. Pins configured as analog inputs will
	read '0'. The ANSEL register is defined for
	the PIC12F675.

EXAMPLE 3-1: INITIALIZING GPIO

BCF	STATUS, RPO	;Bank 0
CLRF	GPIO	;Init GPIO
MOVLW	07h	;Set GP<2:0> to
MOVWF	CMCON	;digital IO
BSF	STATUS, RPO	;Bank 1
CLRF	ANSEL	;Digital I/O
MOVLW	0Ch	;Set GP<3:2> as inputs
MOVWF	TRISIO	;and set GP<5:4,1:0>
		;as outputs
1		

3.2 Additional Pin Functions

Every GPIO pin on the PIC12F629/675 has an interrupt-on-change option and every GPIO pin, except GP3, has a weak pull-up option. The next two sections describe these functions.

3.2.1 WEAK PULL-UP

Each of the GPIO pins, except GP3, has an individually configurable weak internal pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 3-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the GPPU bit (OPTION<7>).

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
bit 7							bit 0

REGISTER 3-1: GPIO: GPIO REGISTER (ADDRESS: 05h)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **GPIO<5:0>**: General Purpose I/O pin 1 = Port pin is >VIH 0 = Port pin is <VIL

7.3 A/D Operation During Sleep

The A/D converter module can operate during Sleep. This requires the A/D clock source to be set to the internal RC oscillator. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared, and the result is loaded into the ADRESH:ADRESL registers. If the A/D interrupt is enabled, the device awakens from Sleep. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set. When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted, and the A/D module is turned off. The ADON bit remains set.

7.4 Effects of Reset

A device Reset forces all registers to their Reset state. Thus the A/D module is turned off and any pending conversion is aborted. The ADRESH:ADRESL registers are unchanged.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
05h	GPIO		—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	xx xxxx	uu uuuu
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000u
0Ch	PIR1	EEIF	ADIF			CMIF	_	—	TMR1IF	00 00	00 00
1Eh	ADRESH	Most Signif	icant 8 bits c	f the Left Sh	ifted A/D res	sult or 2 bits	of the Right	Shifted Re	esult	XXXX XXXX	սսսս սսսս
1Fh	ADCON0	ADFM	VCFG	-	-	CHS1	CHS0	GO	ADON	00 0000	00 0000
85h	TRISIO	_	_	TRISI05	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISI00	11 1111	11 1111
8Ch	PIE1	EEIE	ADIE	-	-	CMIE	—	—	TMR1IE	00 00	00 00
9Eh	ADRESL	Least Signi	Least Significant 2 bits of the Left Shifted A/D Result or 8 bits of the Right Shifted Result						Result	XXXX XXXX	uuuu uuuu
9Fh	ANSEL		ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111

TABLE 7-2: SUMMARY OF A/D REGISTERS

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D converter module.

8.7 Data EEPROM Operation During Code Protect

Data memory can be code protected by programming the CPD bit to '0'.

When the data memory is code protected, the CPU is able to read and write data to the data EEPROM. It is recommended to code protect the program memory when code protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPS) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations to '0' will also help prevent data memory code protection from becoming breached.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,	e on BOD	Value otł Res	on all 1er sets
0Ch	PIR1	EEIF	ADIF	_	—	CMIF	_		TMR1IF	00	00	00	00
9Ah	EEDATA	EEPROM	1 Data Reg	gister						0000	0000	0000	0000
9Bh	EEADR	_	EEPRON	EPROM Address Register						-000	0000	-000	0000
9Ch	EECON1	_	_	_	_	WRERR	WREN	WR	RD		x000		q000
9Dh	EECON2 ⁽¹⁾	EEPROM	EPROM Control Register 2										

TABLE 8-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

 $\label{eq:logarder} \mbox{Legend: x = unknown, u = unchanged, - = unimplemented read as `0', q = value depends upon condition. Shaded cells are not used by data EEPROM module.}$

Note 1: EECON2 is not a physical register.

9.3.1 MCLR

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 9-5, is suggested.

An internal MCLR option is enabled by setting the MCLRE bit in the Configuration Word. When enabled, MCLR is internally tied to VDD. No internal pull-up option is available for the MCLR pin.

FIGURE 9-5: RECOMMENDED MCLR CIRCUIT



9.3.2 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details (see Section 12.0 "Electrical Specifications"). If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in Reset until VDD reaches VBOD (see Section 9.3.5 "Brown-Out Detect (BOD)").

Note:	The POR circuit does not produce a	ın
	internal Reset when VDD declines.	

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting".

9.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Detect. The Power-up Timer operates on an internal RC oscillator. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the <u>VDD to</u> rise to an acceptable level. A Configuration bit, PWRTE can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Detect is enabled.

The Power-up Time delay will vary from chip to chip and due to:

- VDD variation
- Temperature variation
- · Process variation.

See DC parameters for details (Section 12.0 "Electrical Specifications").

9.3.4 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from Sleep.

FIGURE 9-10: INTERRUPT LOGIC



10.0 INSTRUCTION SET SUMMARY

The PIC12F629/675 instruction set is highly orthogonal and is comprised of three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- · Literal and control operations

Each PIC12F629/675 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 10-1, while the various opcode fields are summarized in Table 10-1.

Table 10-2 lists the instructions recognized by the MPASMTM assembler. A complete description of each instruction is also available in the PIC[®] Mid-Range Reference Manual (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μ s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with
	future products, do not use the OPTION
	and TRISIO instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

10.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register. For example, a CLRF GPIO instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended result that the condition that sets the GPIF flag would be cleared.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
то	Time-out bit
PD	Power-down bit

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS



Param No.	Sym	Characteristic	Freq. Tolerance	Min	Тур†	Max	Units	Conditions
F10	Fosc	Internal Calibrated	±1	3.96	4.00	4.04	MHz	VDD = 3.5V, 25°C
_		INTOSC Frequency	±2	3.92	4.00	4.08	MHz	$2.5V \leq V\text{DD} \leq 5.5V$
								$0^{\circ}C \le TA \le +85^{\circ}C$
			±5	3.80	4.00	4.20	MHz	$2.0V \leq V\text{DD} \leq 5.5V$
								$-40^{\circ}C \le TA \le +85^{\circ}C (IND)$
								$-40^{\circ}C \le TA \le +125^{\circ}C \text{ (EXT)}$
F14	TIOSCST	Oscillator Wake-up from			6	8	μS	VDD = 2.0V, -40°C to +85°C
		Sleep start-up time*	—	—	4	6	μS	VDD = 3.0V, -40°C to +85°C
				_	3	5	μS	VDD = 5.0V, -40°C to +85°C
*	These p	parameters are characteriz	zed but not t	ested.				

TABLE 12-2: PRECISION INTERNAL OSCILLATOR PARAMETERS

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 12-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER,
AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
30	ТмсL	MCLR Pulse Width (low)	2 TBD	— TBD	 TBD	μs ms	VDD = 5V, -40°C to +85°C Extended temperature
31	Тwdt	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5V, -40°C to +85°C Extended temperature
32	Tost	Oscillation Start-up Timer Period		1024Tosc		_	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	28* TBD	72 TBD	132* TBD	ms ms	V _{DD} = 5V, -40°C to +85°C Extended Temperature
34	Tioz	I/O High-impedance from MCLR Low or Watchdog Timer Reset	_		2.0	μS	
	Bvdd	Brown-out Detect Voltage	2.025	_	2.175	V	
		Brown-out Hysteresis	TBD	—	—	—	
35	Твор	Brown-out Detect Pulse Width	100*	_	_	μS	$VDD \le BVDD (D005)$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
A01	NR	Resolution		—	10 bits	bit	
A02	Eabs	Total Absolute Error*	_	—	±1	LSb	VREF = 5.0V
A03	EIL	Integral Error		_	±1	LSb	VREF = 5.0V
A04	Edl	Differential Error	_	_	±1	LSb	No missing codes to 10 bits VREF = 5.0V
A05	Efs	Full Scale Range	2.2*	—	5.5*	V	
A06	EOFF	Offset Error		—	±1	LSb	VREF = 5.0V
A07	Egn	Gain Error	—	—	±1	LSb	VREF = 5.0V
A10	—	Monotonicity	—	guaranteed ⁽³⁾	_	—	$Vss \leq Vain \leq Vref+$
A20 A20A	VREF	Reference Voltage	2.0 2.5	_	 Vdd + 0.3	V	Absolute minimum to ensure 10-bit accuracy
A21	VREF	Reference V High (VDD or VREF)	Vss	—	Vdd	V	
A25	Vain	Analog Input Voltage	Vss	_	VREF	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	_	_	10	kΩ	
A50	IREF	VREF Input Current ⁽²⁾	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
*	These				10	μA	During A/D conversion cycle.

TABLE 12-8:	PIC12F675 A/D CONVERTER CHARACTERISTICS:
-------------	--

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from External VREF or VDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

13.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. "Typical" represents the mean of the distribution at 25°C. "Max" or "min" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.











FIGURE 13-6: MAXIMUM IPD vs. VDD OVER TEMP (+125°C)





WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://support.microchip.com Web Address: www.microchip.com

Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455

Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088

Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075

Cleveland Independence, OH Tel: 216-447-0464 Fax: 216-447-0643

Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924

Detroit Farmington Hills, MI Tel: 248-538-2250 Fax: 248-538-2260

Kokomo Kokomo, IN Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608

Santa Clara Santa Clara, CA Tel: 408-961-6444 Fax: 408-961-6445

Toronto Mississauga, Ontario, Canada Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon Hong Kong Tel: 852-2401-1200 Fax: 852-2401-3431

Australia - Sydney Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing Tel: 86-10-8528-2100 Fax: 86-10-8528-2104

China - Chengdu Tel: 86-28-8665-5511 Fax: 86-28-8665-7889

China - Chongqing Tel: 86-23-8980-9588 Fax: 86-23-8980-9500

China - Hong Kong SAR Tel: 852-2401-1200 Fax: 852-2401-3431

China - Nanjing Tel: 86-25-8473-2460

Fax: 86-25-8473-2470 China - Qingdao Tel: 86-532-8502-7355 Fax: 86-532-8502-7205

China - Shanghai Tel: 86-21-5407-5533 Fax: 86-21-5407-5066

China - Shenyang Tel: 86-24-2334-2829 Fax: 86-24-2334-2393

China - Shenzhen Tel: 86-755-8203-2660 Fax: 86-755-8203-1760

China - Wuhan Tel: 86-27-5980-5300 Fax: 86-27-5980-5118

China - Xian Tel: 86-29-8833-7252 Fax: 86-29-8833-7256

China - Xiamen Tel: 86-592-2388138 Fax: 86-592-2388130

China - Zhuhai Tel: 86-756-3210040 Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore Tel: 91-80-3090-4444 Fax: 91-80-3090-4123

India - New Delhi Tel: 91-11-4160-8631 Fax: 91-11-4160-8632

India - Pune Tel: 91-20-2566-1512 Fax: 91-20-2566-1513

Japan - Yokohama Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea - Daegu Tel: 82-53-744-4301 Fax: 82-53-744-4302

Korea - Seoul Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934

Malaysia - Kuala Lumpur Tel: 60-3-6201-9857 Fax: 60-3-6201-9859

Malaysia - Penang Tel: 60-4-227-8870 Fax: 60-4-227-4068

Philippines - Manila Tel: 63-2-634-9065 Fax: 63-2-634-9069

Singapore Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan - Hsin Chu Tel: 886-3-6578-300 Fax: 886-3-6578-370

Taiwan - Kaohsiung Tel: 886-7-536-4818 Fax: 886-7-536-4803

Taiwan - Taipei Tel: 886-2-2500-6610 Fax: 886-2-2508-0102

Thailand - Bangkok Tel: 66-2-694-1351 Fax: 66-2-694-1350

EUROPE

Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4450-2828 Fax: 45-4485-2829

France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781

Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340

Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91

UK - Wokingham Tel: 44-118-921-5869 Fax: 44-118-921-5820

01/05/10