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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN-S (6x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12f675-i-mf">https://www.e-xfl.com/product-detail/microchip-technology/pic12f675-i-mf</a>

# PIC12F629/675

## 2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

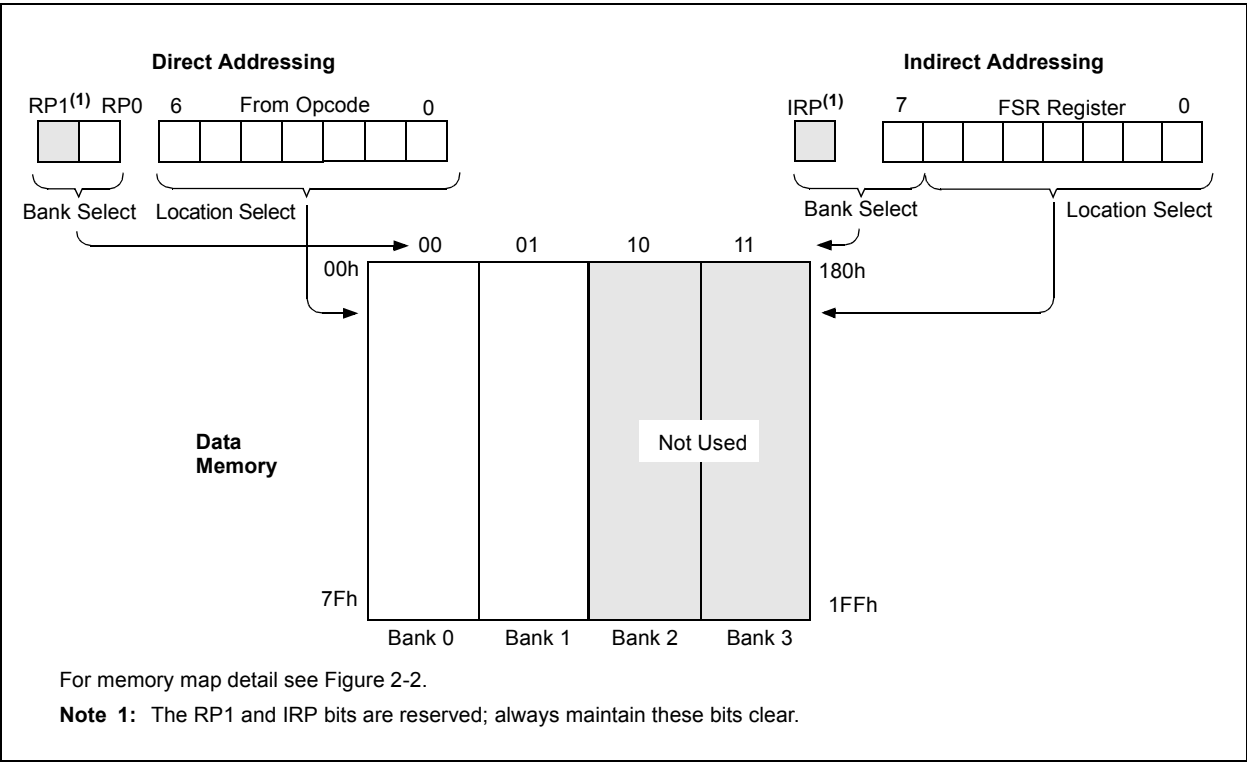
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-2.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

### EXAMPLE 2-1: INDIRECT ADDRESSING

```
MOVLW 0x20 ;initialize pointer
MOVWF FSR ;to RAM
NEXT   CLRF INDF ;clear INDF register
      INCF FSR ;inc pointer
      BTFSS FSR,4 ;all done?
      GOTO NEXT ;no clear next
CONTINUE ;yes continue
```

FIGURE 2-2: DIRECT/INDIRECT ADDRESSING PIC12F629/675



## 4.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION\_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION\_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x...etc.) will clear the prescaler. When assigned to WDT, a CLRWDWT instruction will clear the prescaler along with the Watchdog Timer.

### 4.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 4-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

### EXAMPLE 4-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF    STATUS,RP0    ;Bank 0
CLRWDWT                ;Clear WDT
CLRF    TMR0          ;Clear TMR0 and
                        ; prescaler
BSF     STATUS,RP0    ;Bank 1

MOVLW   b'00101111'  ;Required if desired
MOVWF   OPTION_REG    ; PS2:PS0 is
CLRWDWT                ; 000 or 001
                        ;
MOVLW   b'00101xxx'   ;Set postscaler to
MOVWF   OPTION_REG    ; desired WDT rate
BCF     STATUS,RP0    ;Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 4-2. This precaution must be taken even if the WDT is disabled.

### EXAMPLE 4-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDWT                ;Clear WDT and
                        ; postscaler
BSF     STATUS,RP0    ;Bank 1

MOVLW   b'xxxx0xxx'   ;Select TMR0,
                        ; prescale, and
                        ; clock source
MOVWF   OPTION_REG    ;
BCF     STATUS,RP0    ;Bank 0
```

**TABLE 4-1: REGISTERS ASSOCIATED WITH TIMER0**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000u
81h	OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

**Legend:** — = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown.  
Shaded cells are not used by the Timer0 module.

## 6.2 Comparator Configuration

There are eight modes of operation for the comparator. The CMCON register, shown in Register 6-1, is used to select the mode. Figure 6-2 shows the eight possible modes. The TRISIO register controls the data direction of the comparator pins for each mode. If the Comparator mode is changed, the comparator output level may not be valid for a specified period of time. Refer to the specifications in **Section 12.0 “Electrical Specifications”**.

**Note:** Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

**FIGURE 6-2: COMPARATOR I/O OPERATING MODES**

<p>Comparator Reset (POR Default Value - low power) CM2:CM0 = 000</p>	<p>Comparator Off (Lowest power) CM2:CM0 = 111</p>
<p>Comparator without Output CM2:CM0 = 010</p>	<p>Comparator w/o Output and with Internal Reference CM2:CM0 = 100</p>
<p>Comparator with Output and Internal Reference CM2:CM0 = 011</p>	<p>Multiplexed Input with Internal Reference and Output CM2:CM0 = 101</p>
<p>Comparator with Output CM2:CM0 = 001</p>	<p>Multiplexed Input with Internal Reference CM2:CM0 = 110</p>
<p>A = Analog Input, ports always reads '0' D = Digital Input CIS = Comparator Input Switch (CMCON&lt;3&gt;)</p>	

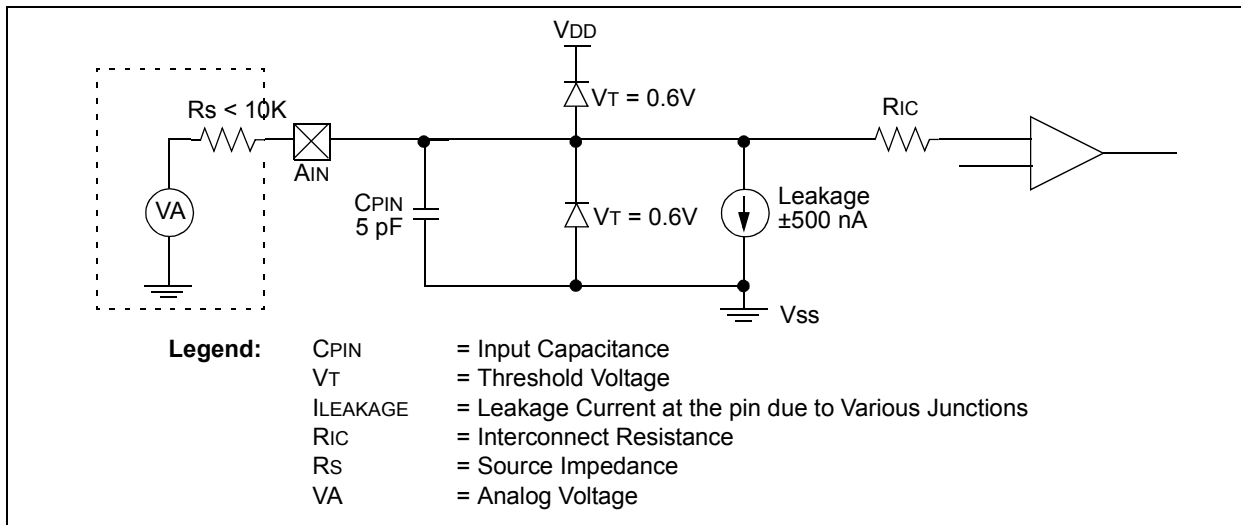
# PIC12F629/675

### 6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this

range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 k $\Omega$  is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

### FIGURE 6-3: ANALOG INPUT MODE



## 6.4 Comparator Output

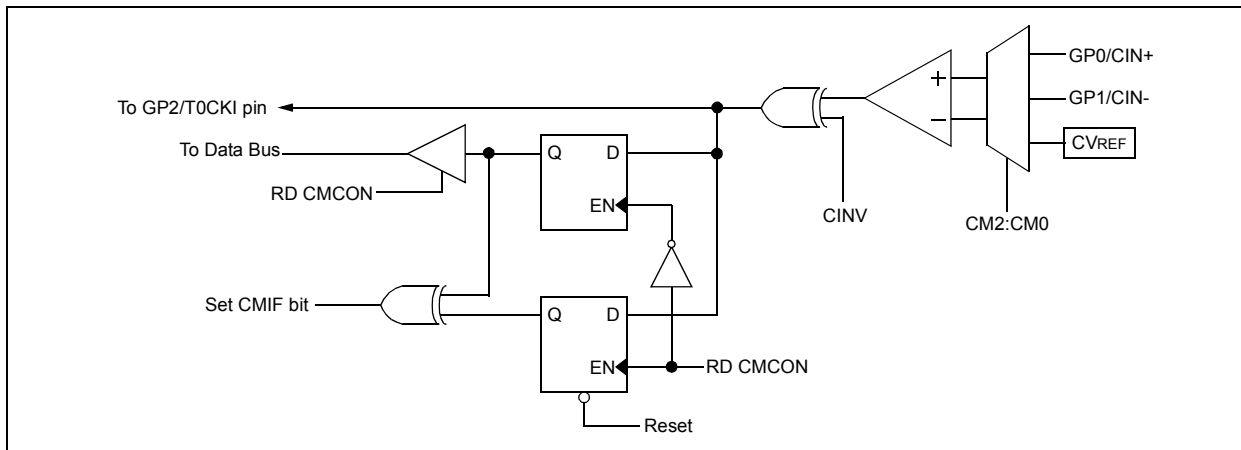
The comparator output, COUT, is read through the CMCON register. This bit is read-only. The comparator output may also be directly output to the GP2 pin in three of the eight possible modes, as shown in Figure 6-2. When in one of these modes, the output on GP2 is asynchronous to the internal clock. Figure 6-4 shows the comparator output block diagram.

The TRISIO<2> bit functions as an output enable/disable for the GP2 pin while the comparator is in an Output mode.

**Note 1:** When reading the GPIO register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the TTL input specification.

**2:** Analog levels on any pin that is defined as a digital input, may cause the input buffer to consume more current than is specified.

**FIGURE 6-4: MODIFIED COMPARATOR OUTPUT BLOCK DIAGRAM**



## 6.5 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for four of the eight Comparator modes. The VRCON register, Register 6-2, controls the voltage reference module shown in Figure 6-5.

### 6.5.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equations determine the output voltages:

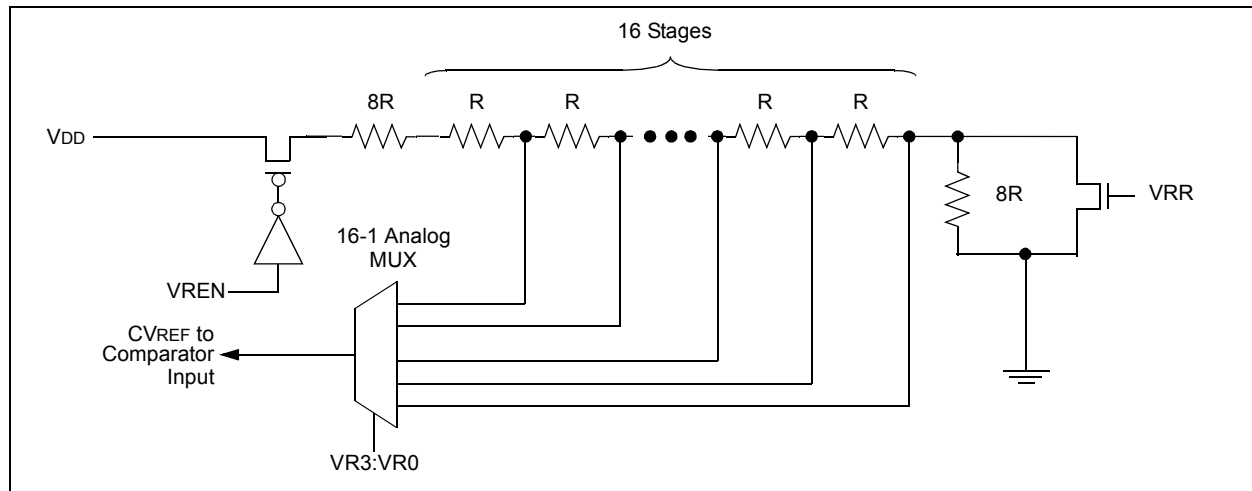
$$VRR = 1 \text{ (low range): } CVREF = (VR3:VR0 / 24) \times VDD$$

$$VRR = 0 \text{ (high range): } CVREF = (VDD / 4) + (VR3:VR0 \times VDD / 32)$$

### 6.5.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 6-5) keep CVREF from approaching VSS or VDD. The Voltage Reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 12.0 "Electrical Specifications"**.

**FIGURE 6-5: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**



## 6.6 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 12-7).

## 6.7 Operation During Sleep

Both the comparator and voltage reference, if enabled before entering Sleep mode, remain active during Sleep. This results in higher Sleep currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in Sleep mode, turn off the comparator, CM2:CM0 = 111, and voltage reference, VRCON<7> = 0.

While the comparator is enabled during Sleep, an interrupt will wake-up the device. If the device wakes up from Sleep, the contents of the CMCON and VRCON registers are not affected.

## 6.8 Effects of a Reset

A device Reset forces the CMCON and VRCON registers to their Reset states. This forces the comparator module to be in the Comparator Reset mode, CM2:CM0 = 000 and the voltage reference to its off state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.

## 8.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F629/675 devices have 128 bytes of data EEPROM with an address range from 0h to 7Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip to chip. Please refer to AC Specifications for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the data EEPROM is available in the PIC® Mid-Range Reference Manual, (DS33023).

### REGISTER 8-1: EEDAT: EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

**EEDATn:** Byte value to write to or read from data EEPROM

### REGISTER 8-2: EEADR: EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

**Unimplemented:** Should be set to '0'

bit 6-0

**EEADR:** Specifies one of 128 locations for EEPROM Read/Write Operation

# PIC12F629/675

## 9.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations, as shown in Register 9.2. These bits are mapped in program memory location 2007h.

**Note:** Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See PIC12F629/675 Programming Specification for more information.

**REGISTER 9-1: CONFIG: CONFIGURATION WORD (ADDRESS: 2007h)**

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
BG1	BG0	—	—	—	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	BODEN	MCLRE	$\overline{\text{PWRT}}\text{E}$	WDTE	F0SC2	F0SC1	F0SC0
bit 13													bit 0

**Legend:**

P = Programmed using ICSP™

R = Readable bit

Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

bit 13-12 **BG1:BG0:** Bandgap Calibration bits for BOD and POR voltage<sup>(1)</sup>

00 = Lowest bandgap voltage

11 = Highest bandgap voltage

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **CPD:** Data Code Protection bit<sup>(2)</sup>

1 = Data memory code protection is disabled

0 = Data memory code protection is enabled

bit 7 **CP:** Code Protection bit<sup>(3)</sup>

1 = Program Memory code protection is disabled

0 = Program Memory code protection is enabled

bit 6 **BODEN:** Brown-out Detect Enable bit<sup>(4)</sup>

1 = BOD enabled

0 = BOD disabled

bit 5 **MCLRE:** GP3/ $\overline{\text{MCLR}}$  Pin Function Select bit<sup>(5)</sup>

1 = GP3/ $\overline{\text{MCLR}}$  pin function is  $\overline{\text{MCLR}}$

0 = GP3/ $\overline{\text{MCLR}}$  pin function is digital I/O,  $\overline{\text{MCLR}}$  internally tied to VDD

bit 4 **PWRT** $\overline{\text{E}}$ : Power-up Timer Enable bit

1 = PWRT disabled

0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 2-0 **FOSC2:FOSC0:** Oscillator Selection bits

111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN

110 = RC oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN

101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN

100 = INTOSC oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN

011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN

010 = HS oscillator: High speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

000 = LP oscillator: Low-power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

**Note 1:** The Bandgap Calibration bits are factory programmed and must be read and saved prior to erasing the device as specified in the PIC12F629/675 Programming Specification. These bits are reflected in an export of the Configuration Word. Microchip Development Tools maintain all Calibration bits to factory settings.

**2:** The entire data EEPROM will be erased when the code protection is turned off.

**3:** The entire program memory will be erased, including OSCCAL value, when the code protection is turned off.

**4:** Enabling Brown-out Detect does not automatically enable Power-up Timer.

**5:** When  $\overline{\text{MCLR}}$  is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.



## 9.2 Oscillator Configurations

### 9.2.1 OSCILLATOR TYPES

The PIC12F629/675 can be operated in eight different oscillator option modes. The user can program three Configuration bits (FOSC2 through FOSC0) to select one of these eight modes:

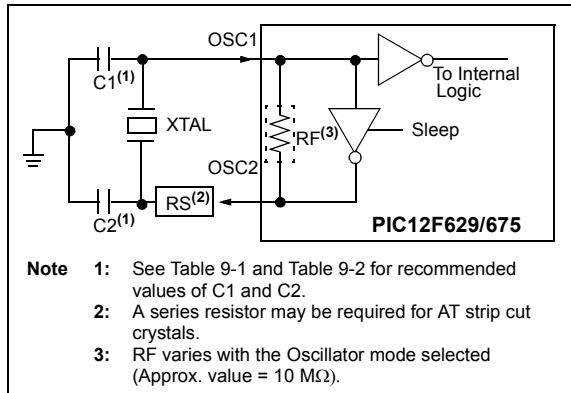
- LP Low-Power Crystal
- XT Crystal/Resonator
- HS High-Speed Crystal/Resonator
- RC External Resistor/Capacitor (2 modes)
- INTOSC Internal Oscillator (2 modes)
- EC External Clock In

**Note:** Additional information on oscillator configurations is available in the PIC® Mid-Range Reference Manual, (DS33023).

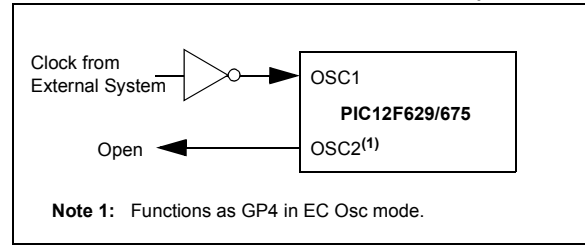
### 9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (see Figure 9-1). The PIC12F629/675 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may yield a frequency outside of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (see Figure 9-2).

**FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) HS, XT OR LP OSC CONFIGURATION**



**FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT, EC, OR LP OSC CONFIGURATION)**



**TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS**

Ranges Characterized:			
Mode	Freq.	OSC1(C1)	OSC2(C2)
XT	455 kHz	68-100 pF	68-100 pF
	2.0 MHz	15-68 pF	15-68 pF
	4.0 MHz	15-68 pF	15-68 pF
HS	8.0 MHz	10-68 pF	10-68 pF
	16.0 MHz	10-22 pF	10-22 pF

**Note 1:** Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR**

Mode	Freq.	OSC1(C1)	OSC2(C2)
LP	32 kHz	68-100 pF	68-100 pF
XT	100 kHz	68-150 pF	150-200 pF
	2 MHz	15-30 pF	15-30 pF
	4 MHz	15-30 pF	15-30 pF
HS	8 MHz	15-30 pF	15-30 pF
	10 MHz	15-30 pF	15-30 pF
	20 MHz	15-30 pF	15-30 pF

**Note 1:** Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

<b>RETFIE</b>	<b>Return from Interrupt</b>
Syntax:	[ <i>label</i> ] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>RETFIE</pre> <p>After Interrupt</p> <pre>PC = TOS GIE = 1</pre>

<b>RETLW</b>	<b>Return with literal in W</b>
Syntax:	[ <i>label</i> ] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>CALL TABLE;W contains table ;offset value ;W now has table value . . . ADDWF PCL;W = offset RETLW k1 ;Begin table RETLW k2 ; . . . RETLW kn ; End of table</pre> <p>Before Instruction W = 0x07</p> <p>After Instruction W = value of k8</p>

<b>RETURN</b>	<b>Return from Subroutine</b>
Syntax:	[ <i>label</i> ] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

<b>XORLW</b>	<b>Exclusive OR Literal with W</b>
Syntax:	<code>[label] XORLW k</code>
Operands:	$0 \leq k \leq 255$
Operation:	$(W) \text{ .XOR. } k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

<b>XORWF</b>	<b>Exclusive OR W with f</b>
Syntax:	<code>[label] XORWF f,d</code>
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) \text{ .XOR. } (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

# PIC12F629/675

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NOTES:

## 11.11 PICKit 2 Development Programmer/Debugger and PICKit 2 Debug Express

The PICKit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICKit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICKit 2 Debug Express include the PICKit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 11.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 11.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

## 12.2 DC Characteristics: PIC12F629/675-I (Industrial)

		Standard Operating Conditions (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	Supply Current (IDD)	—	9	16	μA	2.0	Fosc = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011		—	110	150	μA	2.0	Fosc = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012		—	220	280	μA	2.0	Fosc = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013		—	70	110	μA	2.0	Fosc = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014		—	180	250	μA	2.0	Fosc = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015		—	340	450	μA	2.0	Fosc = 4 MHz INTOSC Mode
		—	500	700	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016		—	180	250	μA	2.0	Fosc = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017		—	2.1	2.95	mA	4.5	Fosc = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The test conditions for all I<sub>DD</sub> measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V<sub>DD</sub>; MCLR = V<sub>DD</sub>; WDT disabled.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

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**TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT DETECT REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 TBD	— TBD	— TBD	μs ms	VDD = 5V, -40°C to +85°C Extended temperature
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5V, -40°C to +85°C Extended temperature
32	TOST	Oscillation Start-up Timer Period	—	1024Tosc	—	—	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	28* TBD	72 TBD	132* TBD	ms ms	VDD = 5V, -40°C to +85°C Extended Temperature
34	TIOZ	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
	BVDD	Brown-out Detect Voltage	2.025	—	2.175	V	
		Brown-out Hysteresis	TBD	—	—	—	
35	TBOD	Brown-out Detect Pulse Width	100*	—	—	μs	VDD ≤ BVDD (D005)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 12-8: PIC12F675 A/D CONVERTER CHARACTERISTICS:**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	
A02	EABS	Total Absolute Error*	—	—	±1	LSb	VREF = 5.0V
A03	EIL	Integral Error	—	—	±1	LSb	VREF = 5.0V
A04	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.0V
A05	EFS	Full Scale Range	2.2*	—	5.5*	V	
A06	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.0V
A07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.0V
A10	—	Monotonicity	—	guaranteed <sup>(3)</sup>	—	—	VSS ≤ VAIN ≤ VREF+
A20 A20A	VREF	Reference Voltage	2.0 2.5	—	— VDD + 0.3	V	Absolute minimum to ensure 10-bit accuracy
A21	VREF	Reference V High (VDD or VREF)	VSS	—	VDD	V	
A25	VAIN	Analog Input Voltage	VSS	—	VREF	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	IREF	VREF Input Current <sup>(2)</sup>	10 —	— —	1000 10	μA μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. During A/D conversion cycle.

\* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

**2:** VREF current is from External VREF or VDD pin, whichever is selected as reference input.

**3:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.



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FIGURE 13-3: TYPICAL IPD vs. VDD OVER TEMP (+125°C)

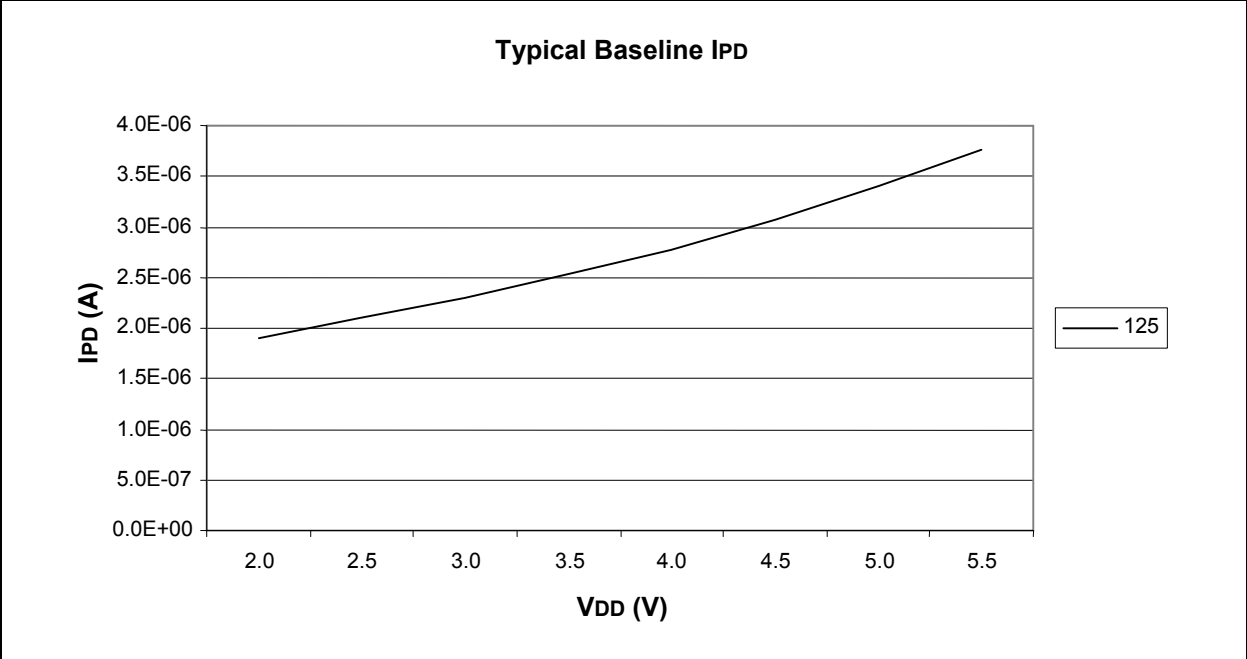
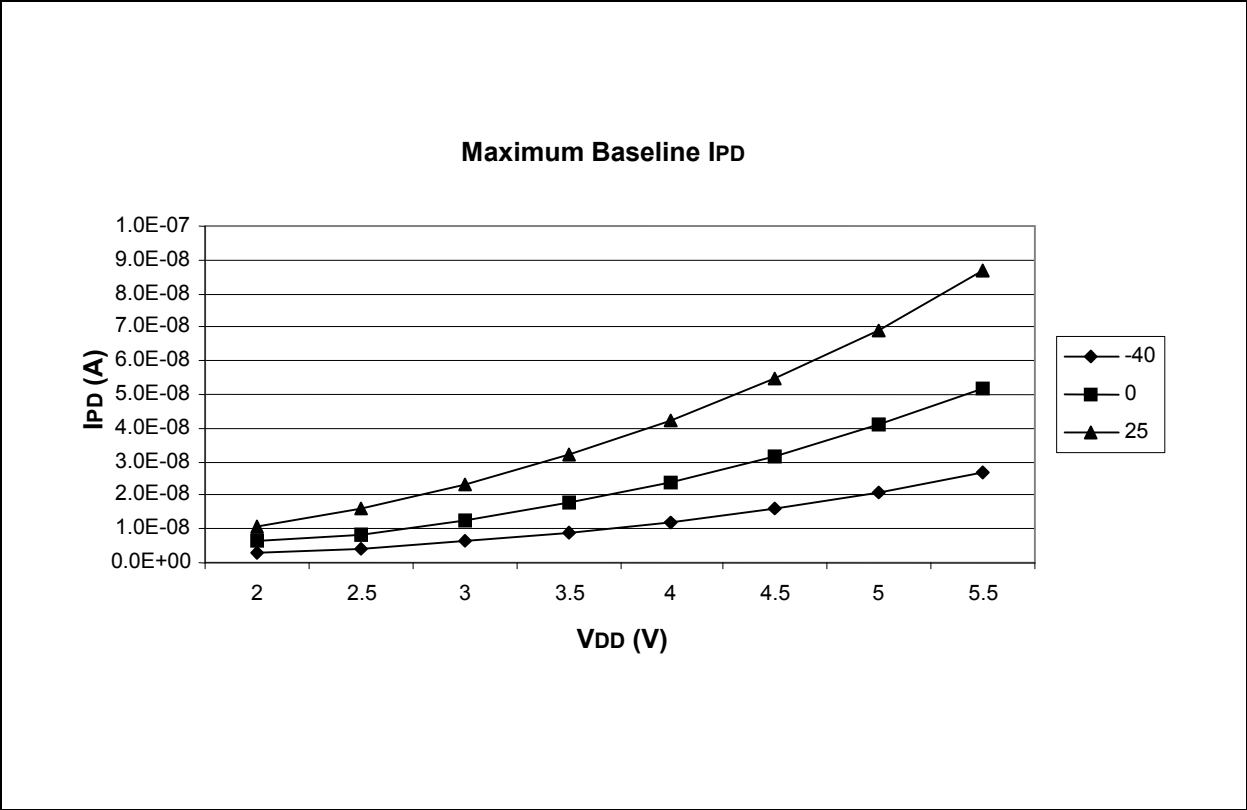


FIGURE 13-4: MAXIMUM IPD vs. VDD OVER TEMP (-40°C TO +25°C)



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FIGURE 13-11: TYPICAL  $I_{PD}$  WITH A/D ENABLED vs.  $V_{DD}$  OVER TEMP (+125°C)

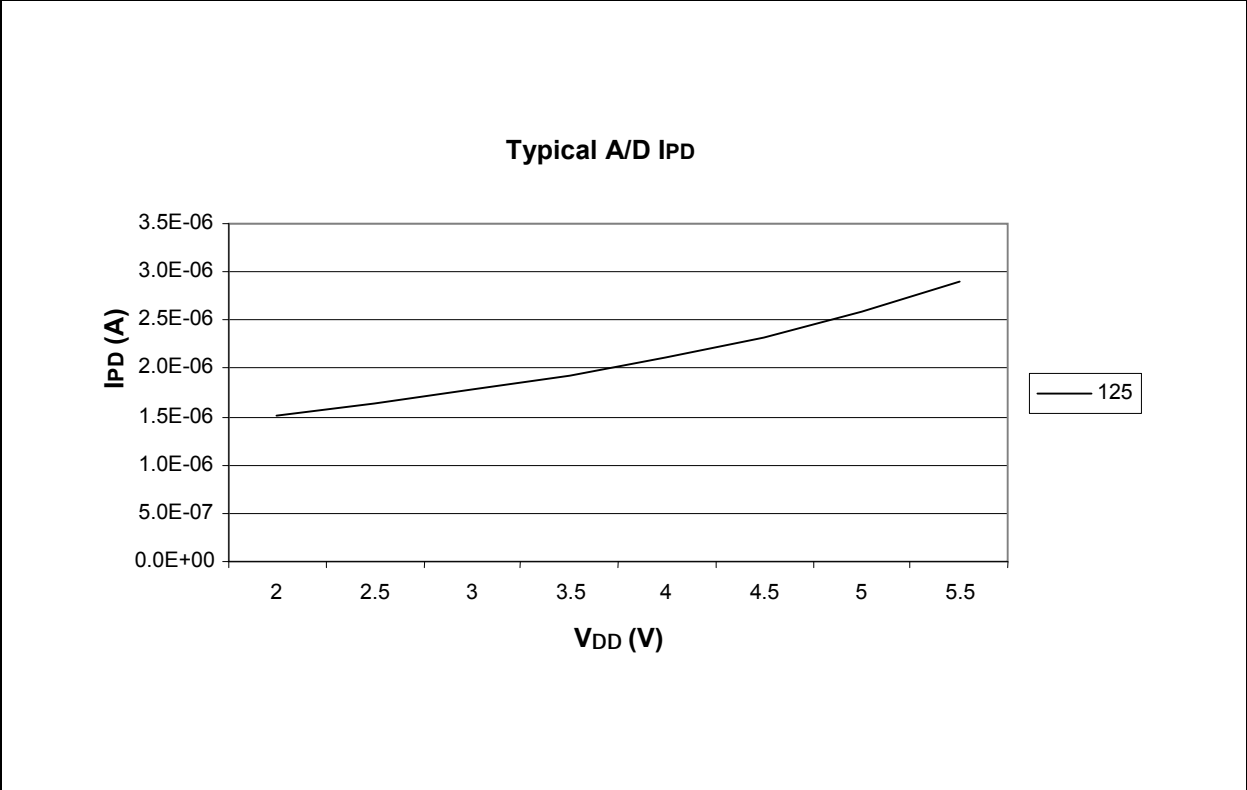
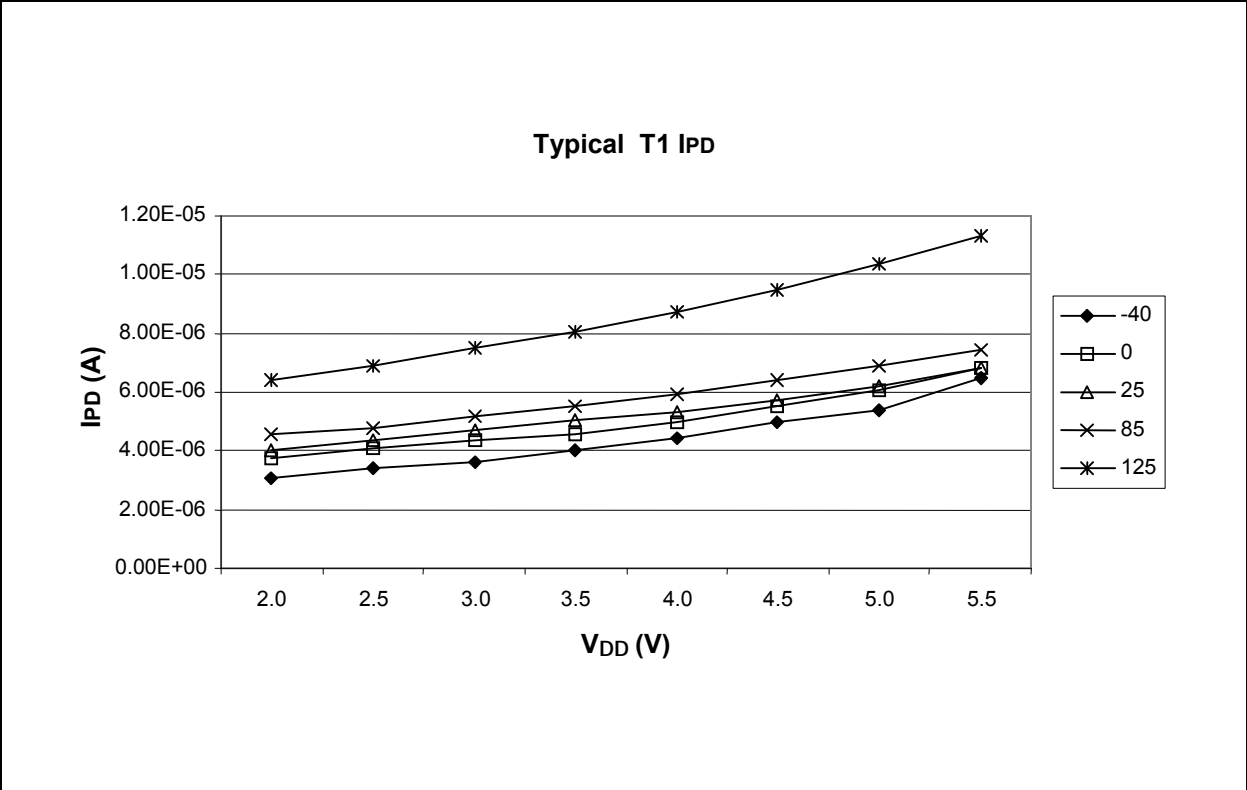


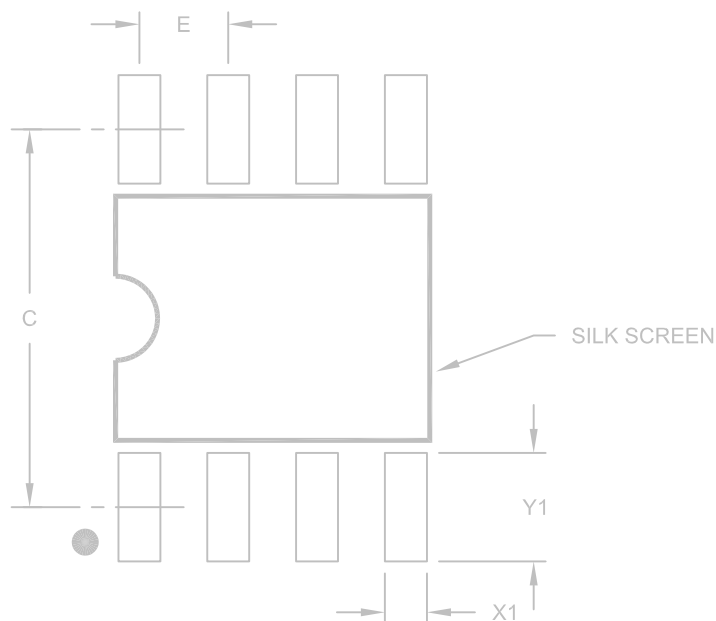
FIGURE 13-12: TYPICAL  $I_{PD}$  WITH T1 OSC ENABLED vs.  $V_{DD}$  OVER TEMP (-40°C TO +125°C), 32 kHz, C1 AND C2=50 pF)



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## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

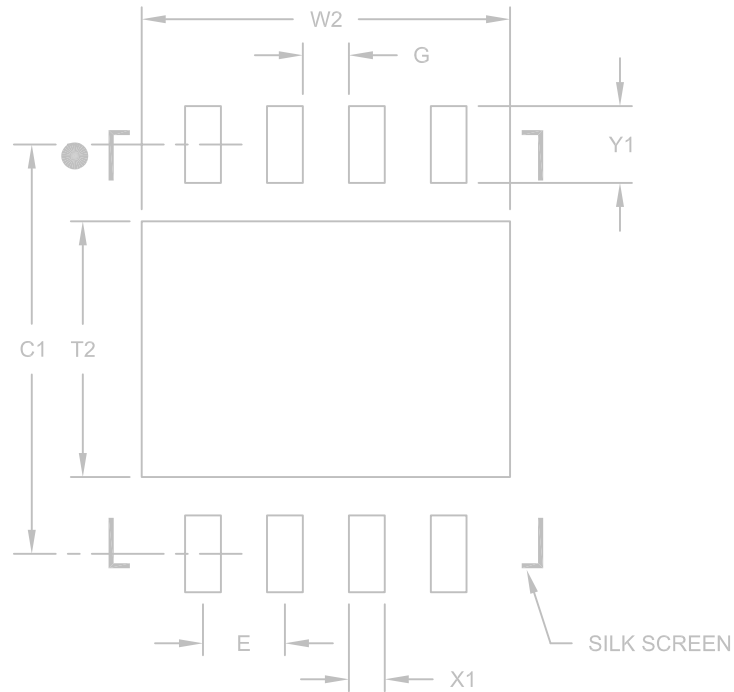
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

## 8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131B

## APPENDIX C: DEVICE MIGRATIONS

This section is intended to describe the functional and electrical specification differences when migrating between functionally similar devices (such as from a PIC16C74A to a PIC16C74B).

**Not Applicable**

## APPENDIX D: MIGRATING FROM OTHER PIC<sup>®</sup> DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC12F6XX family of devices.

### D.1 PIC12C67X to PIC12F6XX

**TABLE 1: FEATURE COMPARISON**

Feature	PIC12C67X	PIC12F6XX
Max Operating Speed	10 MHz	20 MHz
Max Program Memory	2048 bytes	1024 bytes
A/D Resolution	8-bit	10-bit
Data EEPROM	16 bytes	64 bytes
Oscillator Modes	5	8
Brown-out Detect	N	Y
Internal Pull-ups	GP0/1/3	GP0/1/2/4/5
Interrupt-on-change	GP0/1/3	GP0/1/2/3/4/5
Comparator	N	Y

**Note:** This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

**Note:** The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.