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Details

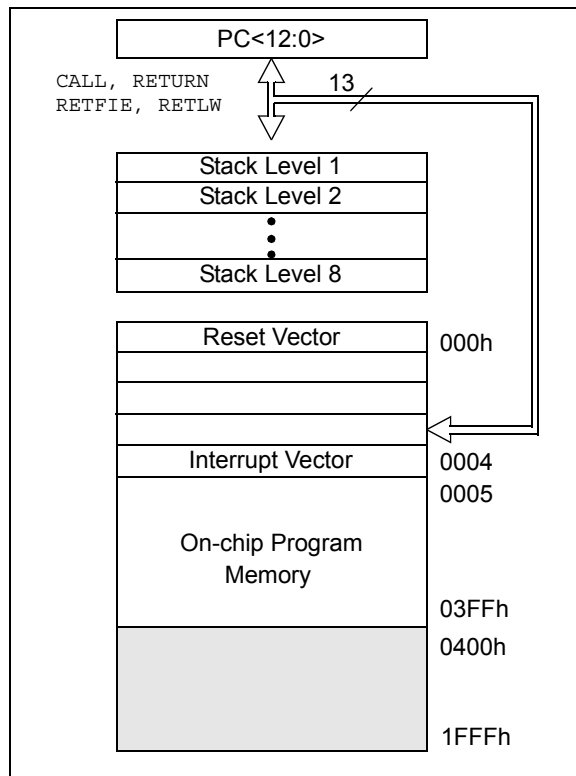
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f675-i-sn

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F629/675 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) for the PIC12F629/675 devices is physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 1K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE DSTEMP/675



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected

Note: The IRP and RP1 bits STATUS<7:6> are reserved and should always be maintained as '0's.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC12F629/675 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

4.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x...etc.) will clear the prescaler. When assigned to WDT, a CLRWDWT instruction will clear the prescaler along with the Watchdog Timer.

4.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 4-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 4-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS,RP0    ;Bank 0
CLRWDWT                ;Clear WDT
CLRF    TMR0          ;Clear TMR0 and
                        ; prescaler
BSF     STATUS,RP0    ;Bank 1

MOVLW   b'00101111'  ;Required if desired
MOVWF   OPTION_REG    ; PS2:PS0 is
CLRWDWT                ; 000 or 001
                        ;
MOVLW   b'00101xxx'   ;Set postscaler to
MOVWF   OPTION_REG    ; desired WDT rate
BCF     STATUS,RP0    ;Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 4-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 4-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDWT                ;Clear WDT and
                        ; postscaler
BSF     STATUS,RP0    ;Bank 1

MOVLW   b'xxxx0xxx'   ;Select TMR0,
                        ; prescale, and
                        ; clock source
MOVWF   OPTION_REG    ;
BCF     STATUS,RP0    ;Bank 0
```

TABLE 4-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
01h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000u
81h	OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown.
Shaded cells are not used by the Timer0 module.

6.0 COMPARATOR MODULE

The PIC12F629/675 devices have one analog comparator. The inputs to the comparator are multiplexed with the GP0 and GP1 pins. There is an on-chip Comparator Voltage Reference that can also be applied to an input of the comparator. In addition, GP2 can be configured as the comparator output.

The Comparator Control Register (CMCON), shown in Register 6-1, contains the bits to control the comparator.

REGISTER 6-1: CMCON: COMPARATOR CONTROL REGISTER (ADDRESS: 19h)

U-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COUT	—	CINV	CIS	CM2	CM1	CM0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **COUT:** Comparator Output bit

When CINV = 0:

1 = $V_{IN+} > V_{IN-}$

0 = $V_{IN+} < V_{IN-}$

When CINV = 1:

1 = $V_{IN+} < V_{IN-}$

0 = $V_{IN+} > V_{IN-}$

bit 5 **Unimplemented:** Read as '0'

bit 4 **CINV:** Comparator Output Inversion bit

1 = Output inverted

0 = Output not inverted

bit 3 **CIS:** Comparator Input Switch bit

When CM2:CM0 = 110 or 101:

1 = V_{IN-} connects to CIN+

0 = V_{IN-} connects to CIN-

bit 2-0 **CM2:CM0:** Comparator Mode bits

Figure 6-2 shows the Comparator modes and CM2:CM0 bit settings

7.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-3. The source impedance (R_s) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}), see Figure 7-3. **The maximum recommended impedance for analog sources is 10 k Ω .** As the impedance

is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, T_{ACQ} , see the PIC® Mid-Range Reference Manual (DS33023).

EQUATION 7-1: ACQUISITION TIME

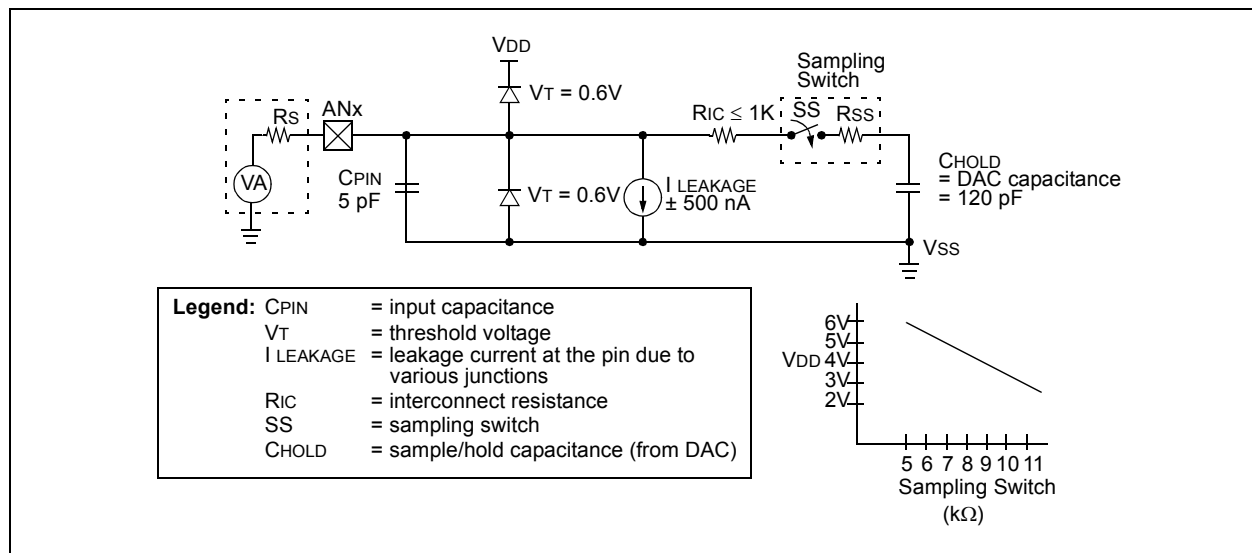
$$\begin{aligned}
 T_{ACQ} &= \text{Amplifier Settling Time} + \\
 &\quad \text{Hold Capacitor Charging Time} + \\
 &\quad \text{Temperature Coefficient} \\
 &= T_{AMP} + T_C + T_{COFF} \\
 &= 2\mu s + T_C + [(\text{Temperature} - 25^\circ\text{C})(0.05\mu s/^\circ\text{C})] \\
 T_C &= \text{CHOLD} (R_{IC} + R_{SS} + R_s) \ln(1/2047) \\
 &= 120\text{pF} (1\text{k}\Omega + 7\text{k}\Omega + 10\text{k}\Omega) \ln(0.0004885) \\
 &= 16.47\mu s \\
 T_{ACQ} &= 2\mu s + 16.47\mu s + [(50^\circ\text{C} - 25^\circ\text{C})(0.05\mu s/^\circ\text{C})] \\
 &= 19.72\mu s
 \end{aligned}$$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

FIGURE 7-3: ANALOG INPUT MODEL



8.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F629/675 devices have 128 bytes of data EEPROM with an address range from 0h to 7Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip to chip. Please refer to AC Specifications for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the data EEPROM is available in the PIC® Mid-Range Reference Manual, (DS33023).

REGISTER 8-1: EEDAT: EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

EEDATn: Byte value to write to or read from data EEPROM

REGISTER 8-2: EEADR: EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

Unimplemented: Should be set to '0'

bit 6-0

EEADR: Specifies one of 128 locations for EEPROM Read/Write Operation

9.0 SPECIAL FEATURES OF THE CPU

Certain special circuits that deal with the needs of real time applications are what sets a microcontroller apart from other processors. The PIC12F629/675 family has a host of such features intended to:

- maximize system reliability
- minimize cost through elimination of external components
- provide power saving operating modes and offer code protection

These features are:

- Oscillator selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC12F629/675 has a Watchdog Timer that is controlled by Configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can provide at least a 72 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 9.2).

PIC12F629/675

9.2.3 EXTERNAL CLOCK IN

For applications where a clock is already available elsewhere, users may directly drive the PIC12F629/675 provided that this external clock source meets the AC/DC timing requirements listed in **Section 12.0 “Electrical Specifications”**. Figure 9-2 shows how an external clock circuit should be configured.

9.2.4 RC OSCILLATOR

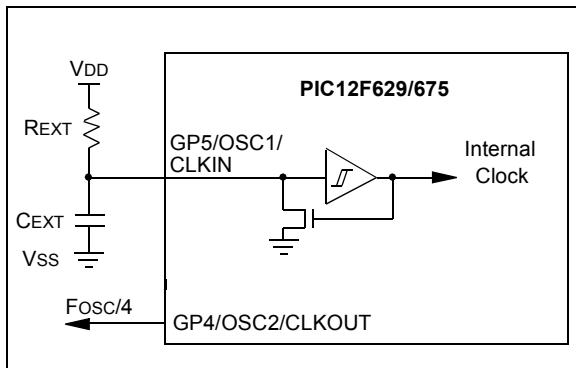
For applications where precise timing is not a requirement, the RC oscillator option is available. The operation and functionality of the RC oscillator is dependent upon a number of variables. The RC oscillator frequency is a function of:

- Supply voltage
- Resistor (REXT) and capacitor (CEXT) values
- Operating temperature.

The oscillator frequency will vary from unit to unit due to normal process parameter variation. The difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to account for the tolerance of the external R and C components. Figure 9-3 shows how the R/C combination is connected.

Two options are available for this Oscillator mode which allow GP4 to be used as a general purpose I/O or to output Fosc/4.

FIGURE 9-3: RC OSCILLATOR MODE



9.2.5 INTERNAL 4 MHz OSCILLATOR

When calibrated, the internal oscillator provides a fixed 4 MHz (nominal) system clock. See Electrical Specifications, **Section 12.0 “Electrical Specifications”**, for information on variation over voltage and temperature.

Two options are available for this Oscillator mode which allow GP4 to be used as a general purpose I/O or to output Fosc/4.

9.2.5.1 Calibrating the Internal Oscillator

A calibration instruction is programmed into the last location of program memory. This instruction is a RETLW XX, where the literal is the calibration value. The literal is placed in the OSCCAL register to set the calibration of the internal oscillator. Example 9-1 demonstrates how to calibrate the internal oscillator. For best operation, decouple (with capacitance) VDD and VSS as close to the device as possible.

Note: Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing part as specified in the PIC12F629/675 Programming specification. Microchip Development Tools maintain all Calibration bits to factory settings.

EXAMPLE 9-1: CALIBRATING THE INTERNAL OSCILLATOR

```
BSF    STATUS, RP0    ;Bank 1
CALL   3FFh           ;Get the cal value
MOVWF  OSCCAL          ;Calibrate
BCF    STATUS, RP0    ;Bank 0
```

9.2.6 CLKOUT

The PIC12F629/675 devices can be configured to provide a clock out signal in the INTOSC and RC oscillator modes. When configured, the oscillator frequency divided by four (Fosc/4) is output on the GP4/OSC2/CLKOUT pin. Fosc/4 can be used for test purposes or to synchronize other logic.

FIGURE 9-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

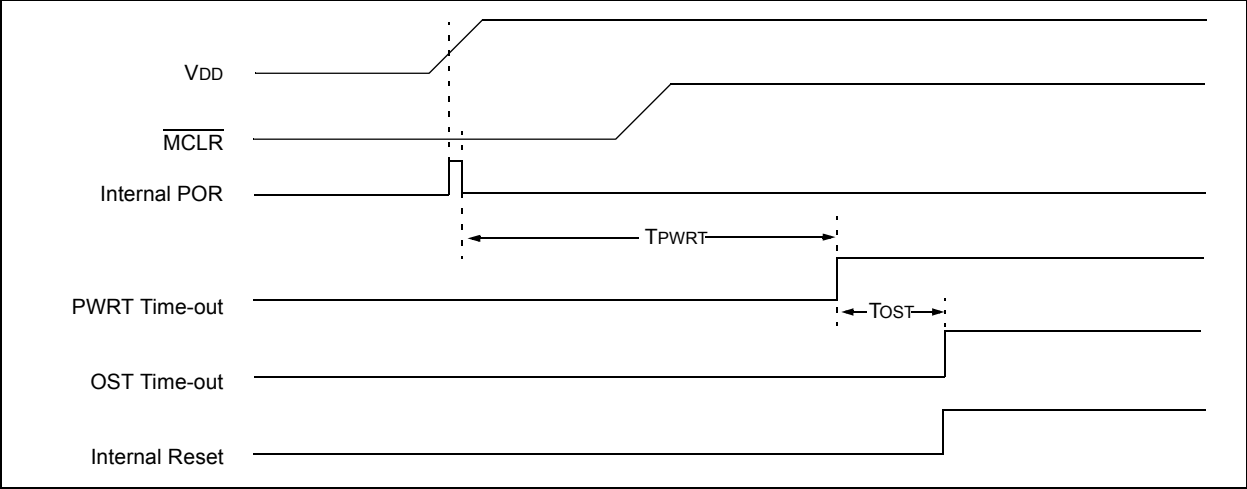


FIGURE 9-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

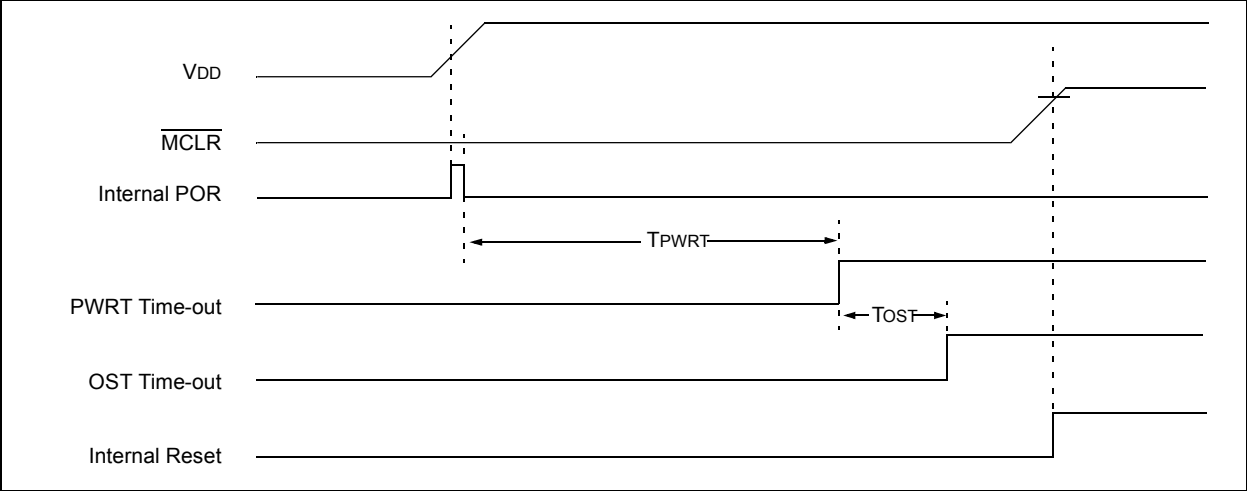
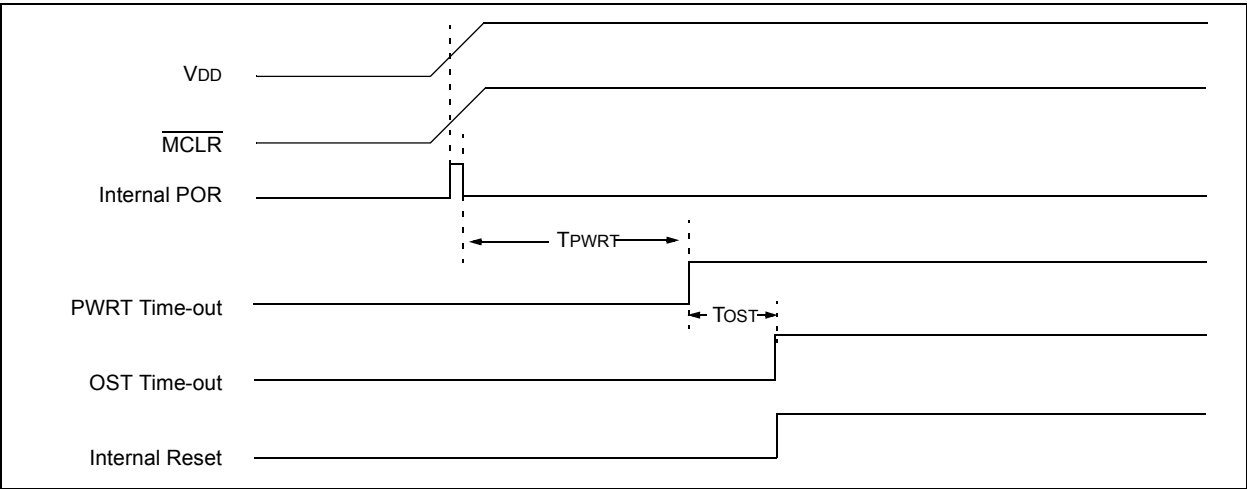


FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})



9.4.1 GP2/INT INTERRUPT

External interrupt on GP2/INT pin is edge-triggered; either rising if INTEDG bit (OPTION<6>) is set, of falling, if INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See **Section 9.7 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 9-13 for timing of wake-up from Sleep through GP2/INT interrupt.

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC12F675.

9.4.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see **Section 4.0 “Timer0 Module”**.

9.4.3 GPIO INTERRUPT

An input change on GPIO change sets the GPIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the GPIE (INTCON<3>) bit. Plus individual pins can be configured through the IOC register.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the GPIF interrupt flag may not get set.

9.4.4 COMPARATOR INTERRUPT

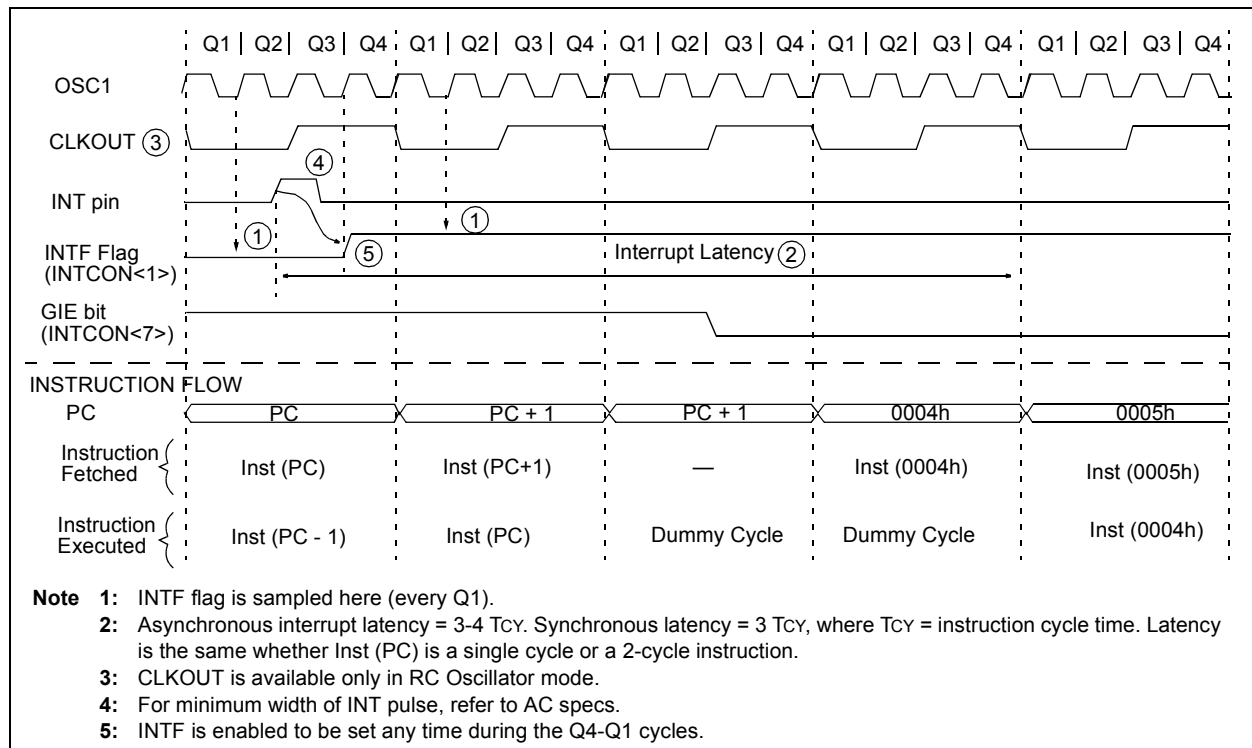
See **Section 6.9 “Comparator Interrupts”** for description of comparator interrupt.

9.4.5 A/D CONVERTER INTERRUPT

After a conversion is complete, the ADIF flag (PIR<6>) is set. The interrupt can be enabled/disabled by setting or clearing ADIE (PIE<6>).

See **Section 7.0 “Analog-to-Digital Converter (A/D) Module (PIC12F675 only)”** for operation of the A/D converter interrupt.

FIGURE 9-11: INT PIN INTERRUPT TIMING



PIC12F629/675

MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, the destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	<pre>MOVF FSR, 0</pre> <p>After Instruction</p> <p>W = value in FSR register Z = 1</p>

MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	<pre>MOVLW 0x5A</pre> <p>After Instruction</p> <p>W = 0x5A</p>

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	<pre>MOVWF OPTION</pre> <p>Before Instruction</p> <p>OPTION = 0xFF W = 0x4F</p> <p>After Instruction</p> <p>OPTION = 0x4F W = 0x4F</p>

NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	<pre>NOP</pre>

11.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

11.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

11.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias	-40 to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3 to +6.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS	-0.3 to +13.5V
Voltage on all other pins with respect to VSS	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all GPIO	125 mA
Maximum current sourced all GPIO	125 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

† **NOTICE:** Stresses above those listed under ‘Absolute Maximum Ratings’ may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below VSS at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ pin, rather than pulling this pin directly to VSS.

TABLE 12-8: PIC12F675 A/D CONVERTER CHARACTERISTICS:

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	
A02	EABS	Total Absolute Error*	—	—	±1	LSb	VREF = 5.0V
A03	EIL	Integral Error	—	—	±1	LSb	VREF = 5.0V
A04	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.0V
A05	EFS	Full Scale Range	2.2*	—	5.5*	V	
A06	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.0V
A07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.0V
A10	—	Monotonicity	—	guaranteed ⁽³⁾	—	—	VSS ≤ VAIN ≤ VREF+
A20 A20A	VREF	Reference Voltage	2.0 2.5	—	— VDD + 0.3	V	Absolute minimum to ensure 10-bit accuracy
A21	VREF	Reference V High (VDD or VREF)	VSS	—	VDD	V	
A25	VAIN	Analog Input Voltage	VSS	—	VREF	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	IREF	VREF Input Current ⁽²⁾	10 —	— —	1000 10	μA μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from External VREF or VDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

FIGURE 13-13: TYPICAL IPD WITH CVREF ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

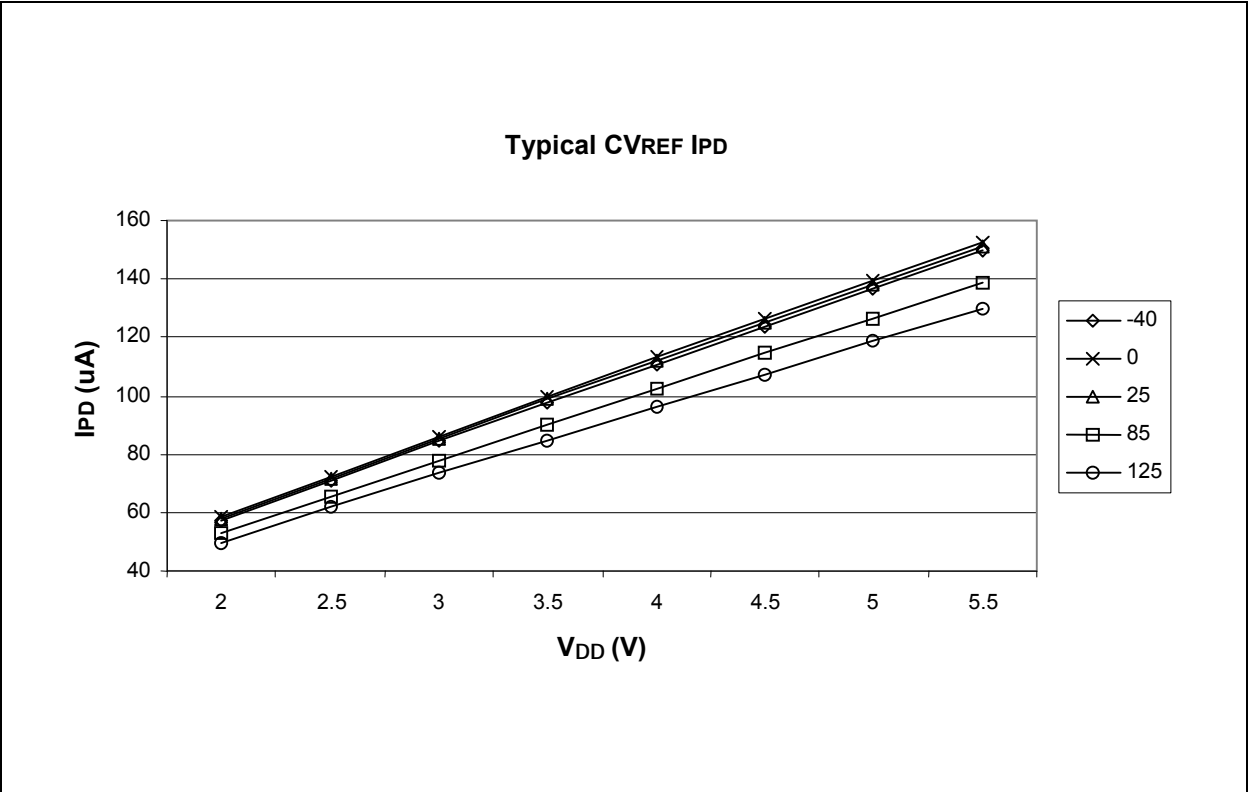
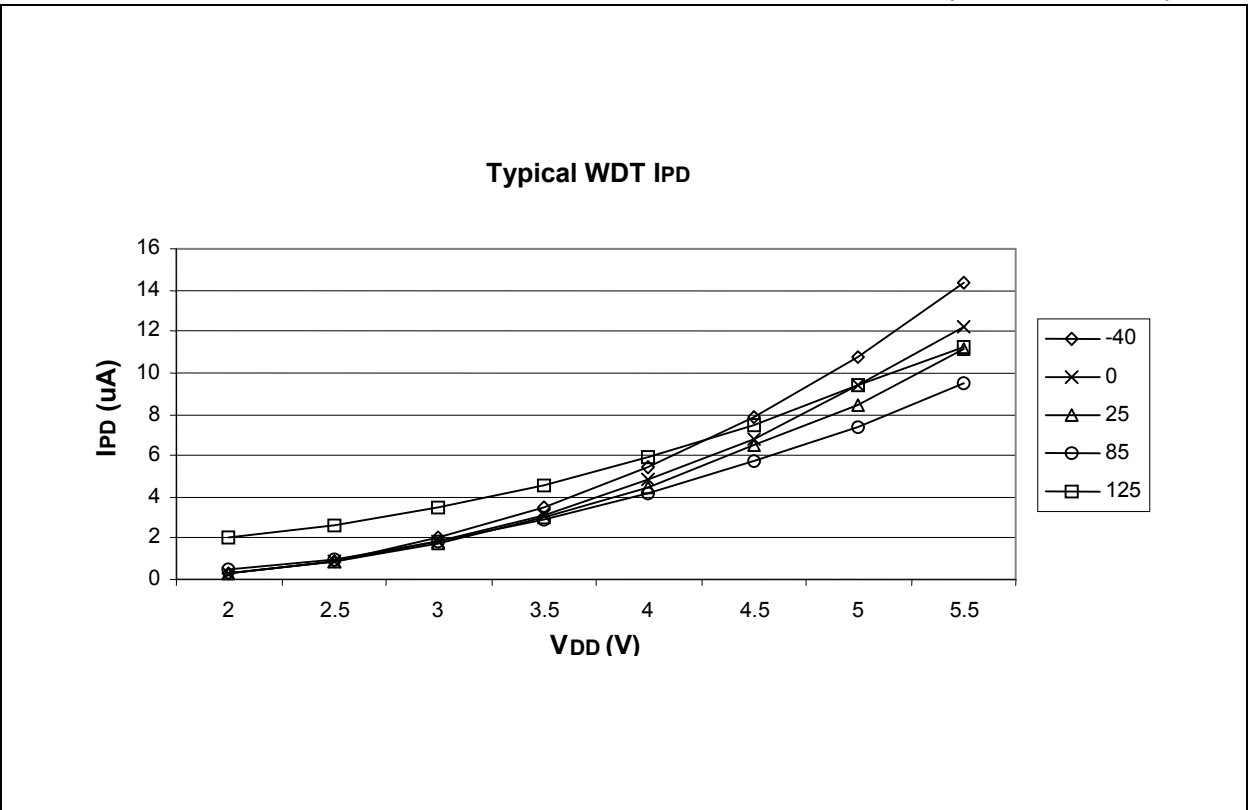


FIGURE 13-14: TYPICAL IPD WITH WDT ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)



14.0 PACKAGING INFORMATION

14.1 Package Marking Information

8-Lead PDIP (Skinny DIP)



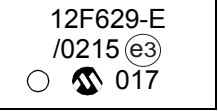
Example



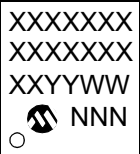
8-Lead SOIC



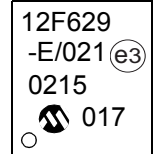
Example



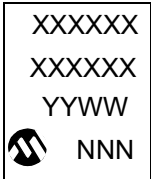
8-Lead DFN-S



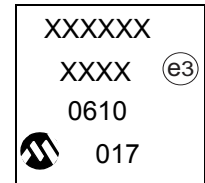
Example



8-Lead DFN (4x4 mm)



Example



Legend:

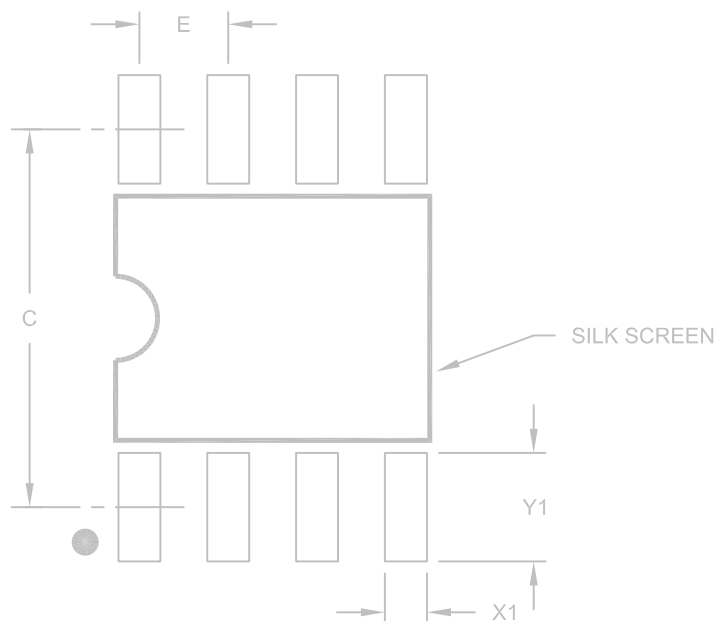
XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PIC12F629/675

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

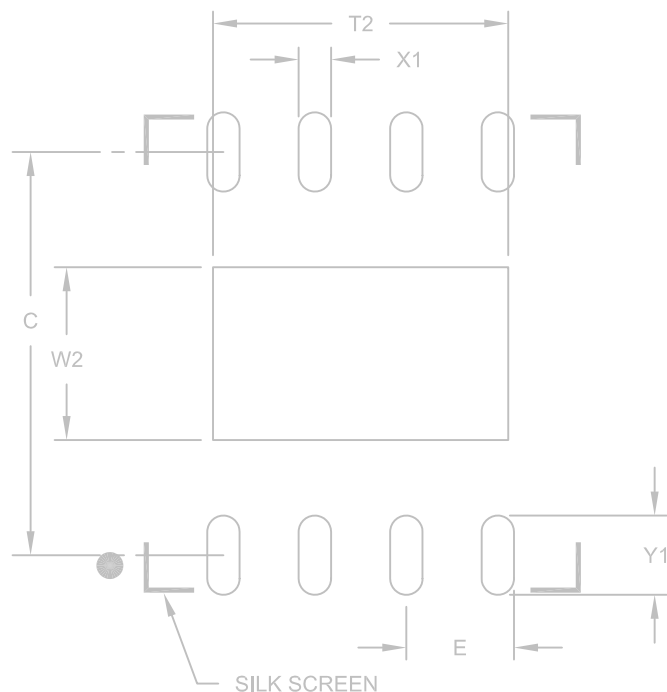
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

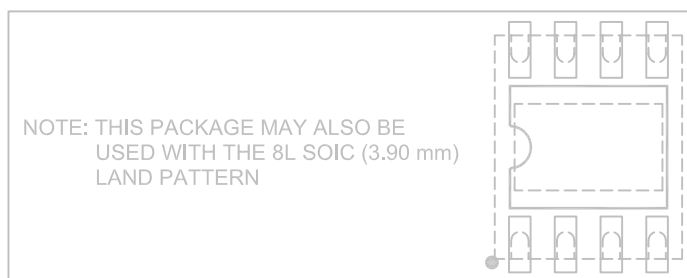
PIC12F629/675

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			4.10
Contact Pad Spacing	C		5.60	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

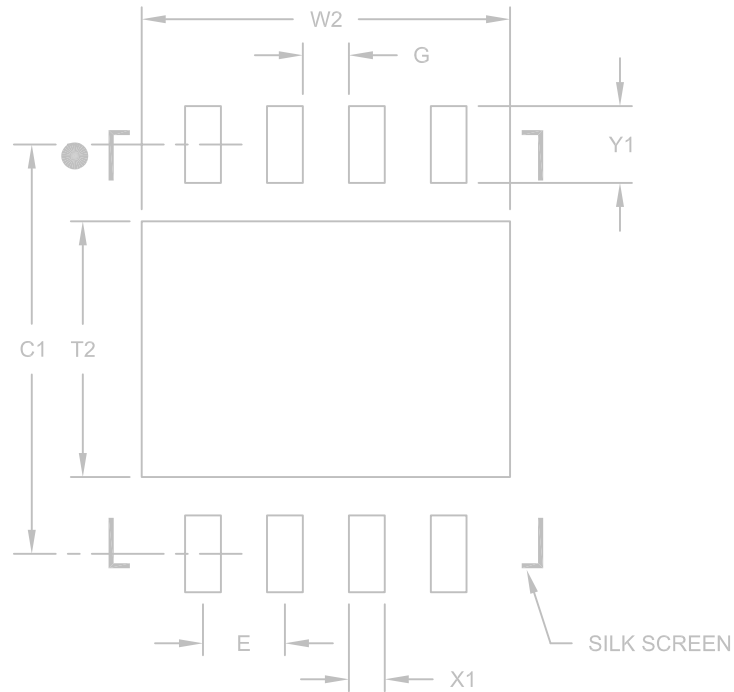
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2122A

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131B

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