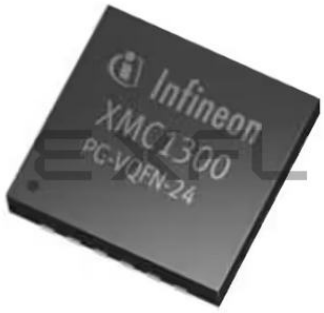
# Infineon Technologies - XMC1302T028X0016ABXUMA1 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 14x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-28-16 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302t028x0016abxuma1 |

# Table of Contents

**Table 1 Synopsis of XMC1300 Device Types** (cont'd)

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1302-T016X0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1302-T016X0032 | PG-TSSOP-16-8 | 32 | 16 |
| XMC1302-T028X0016 | PG-TSSOP-28-8 | 16 | 16 |
| XMC1302-T028X0032 | PG-TSSOP-28-8 | 32 | 16 |
| XMC1302-T028X0064 | PG-TSSOP-28-8 | 64 | 16 |
| XMC1302-T028X0128 | PG-TSSOP-28-8 | 128 | 16 |
| XMC1302-T028X0200 | PG-TSSOP-28-8 | 200 | 16 |
| XMC1301-T038F0008 | PG-TSSOP-38-9 | 8 | 16 |
| XMC1301-T038F0016 | PG-TSSOP-38-9 | 16 | 16 |
| XMC1301-T038F0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1301-T038X0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1301-T038F0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1302-T038X0016 | PG-TSSOP-38-9 | 16 | 16 |
| XMC1302-T038X0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1302-T038X0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1302-T038X0128 | PG-TSSOP-38-9 | 128 | 16 |
| XMC1302-T038X0200 | PG-TSSOP-38-9 | 200 | 16 |
| XMC1301-Q024F0008 | PG-VQFN-24-19 | 8 | 16 |
| XMC1301-Q024F0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1302-Q024F0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1302-Q024F0032 | PG-VQFN-24-19 | 32 | 16 |
| XMC1302-Q024F0064 | PG-VQFN-24-19 | 64 | 16 |
| XMC1302-Q024X0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1302-Q024X0032 | PG-VQFN-24-19 | 32 | 16 |
| XMC1302-Q024X0064 | PG-VQFN-24-19 | 64 | 16 |
| XMC1301-Q040F0008 | PG-VQFN-40-13 | 8 | 16 |
| XMC1301-Q040F0016 | PG-VQFN-40-13 | 16 | 16 |
| XMC1301-Q040F0032 | PG-VQFN-40-13 | 32 | 16 |
| XMC1302-Q040X0016 | PG-VQFN-40-13 | 16 | 16 |
| XMC1302-Q040X0032 | PG-VQFN-40-13 | 32 | 16 |

# 2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

## 2.1 Logic Symbols

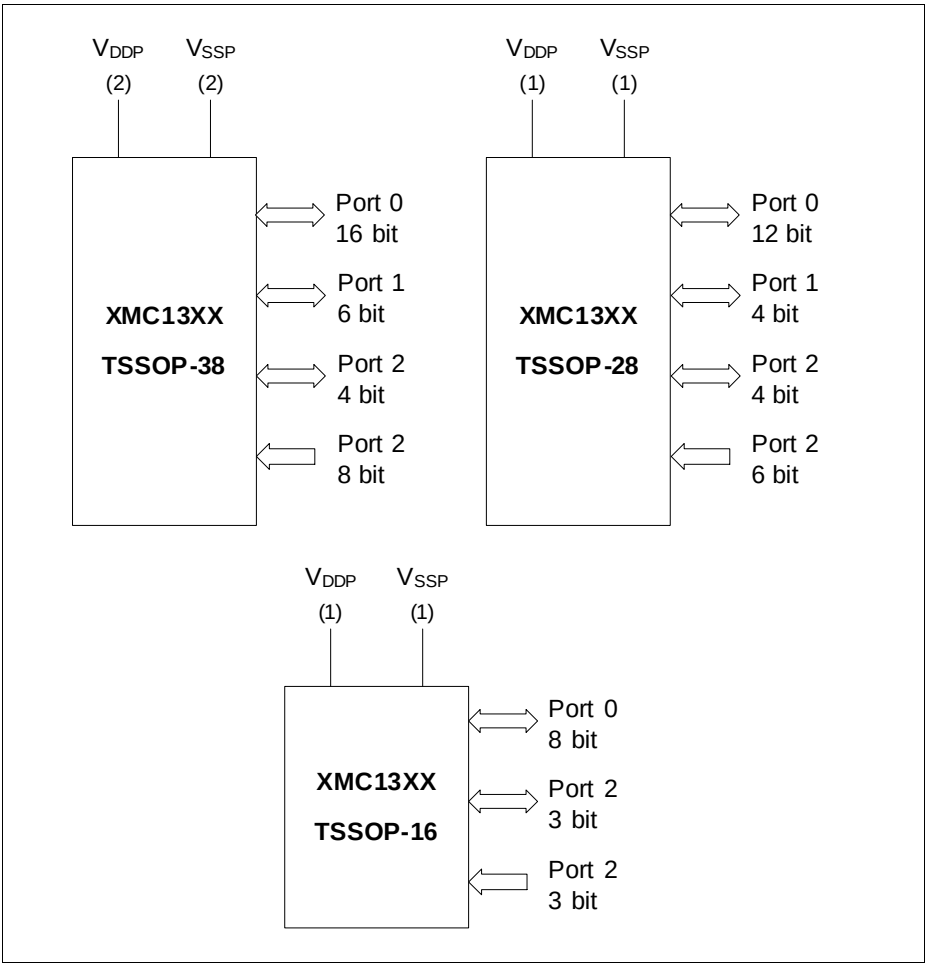



**Figure 2 XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16**

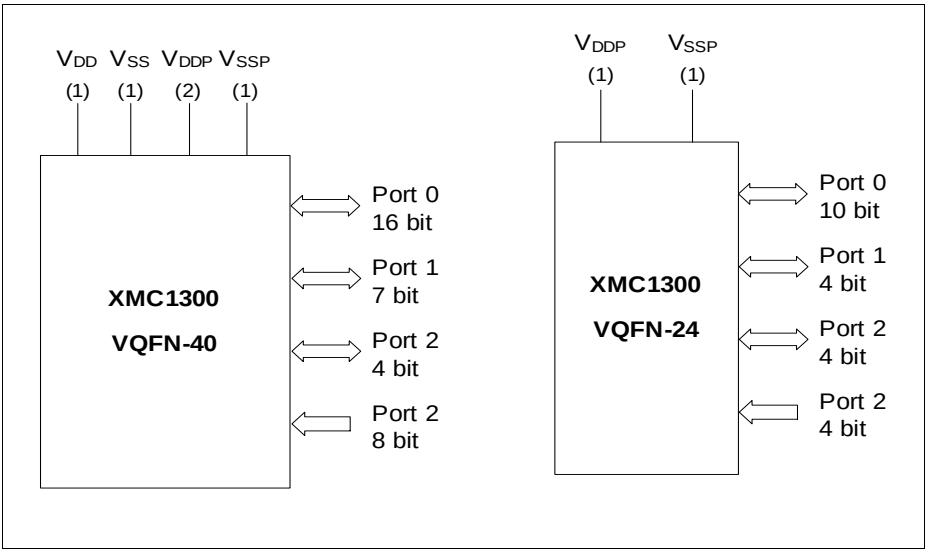



**Figure 3 XMC1300 Logic Symbol for VQFN-24 and VQFN-40**

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

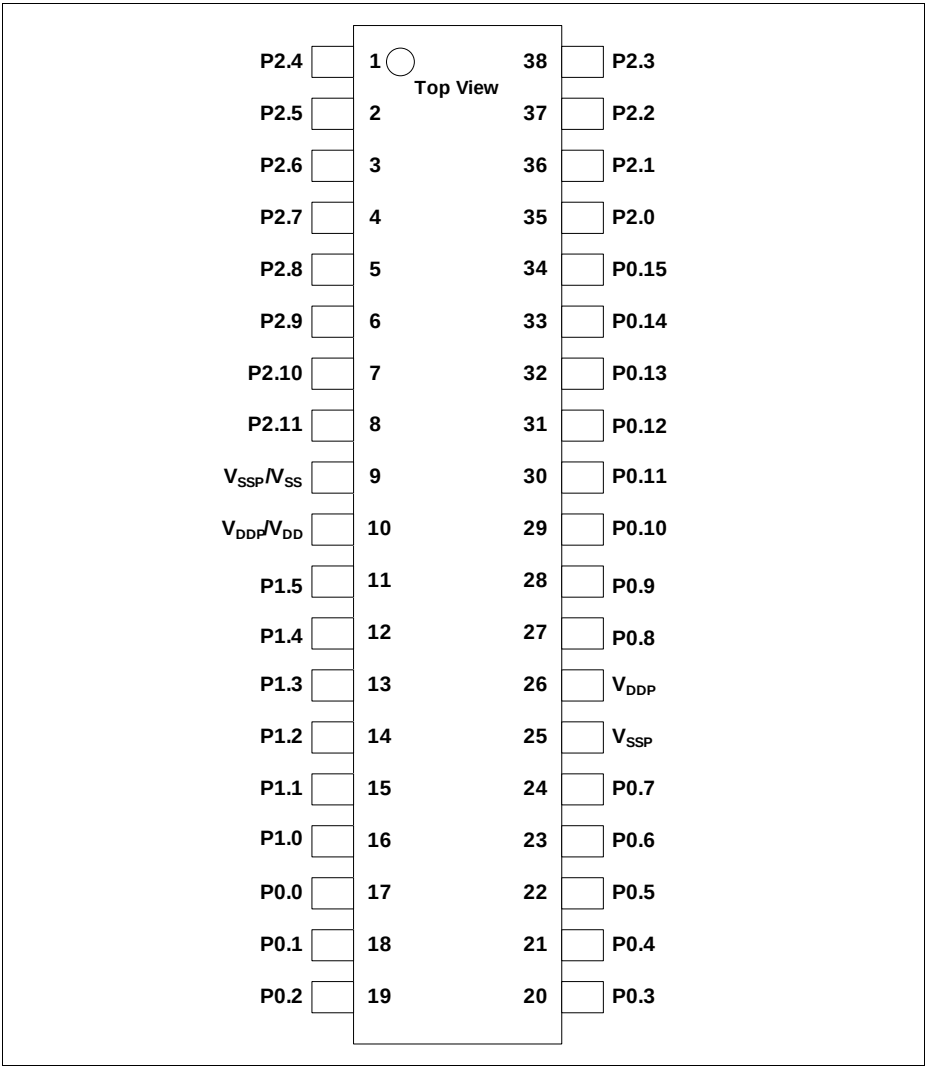



**Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration** (top view)

**Table 6 Package Pin Mapping** (cont'd)

| Function | VQFN 40 | TSSOP 38 | TSSOP 28 | VQFN 24 | TSSOP 16 | Pad Type | Notes |
|---|---|---|---|---|---|---|---|
| P0.7 | 30 | 24 | 17 | 18 | 10 | STD_IN OUT | |
| P0.8 | 33 | 27 | 18 | 19 | 11 | STD_IN OUT | |
| P0.9 | 34 | 28 | 19 | 20 | 12 | STD_IN OUT | |
| P0.10 | 35 | 29 | 20 | - | - | STD_IN OUT | |
| P0.11 | 36 | 30 | - | - | - | STD_IN OUT | |
| P0.12 | 37 | 31 | 21 | 21 | - | STD_IN OUT | |
| P0.13 | 38 | 32 | 22 | 22 | - | STD_IN OUT | |
| P0.14 | 39 | 33 | 23 | 23 | 13 | STD_IN OUT | |
| P0.15 | 40 | 34 | 24 | 24 | 14 | STD_IN OUT | |
| P1.0 | 22 | 16 | 12 | 14 | - | High Current | |
| P1.1 | 21 | 15 | 11 | 13 | - | High Current | |
| P1.2 | 20 | 14 | 10 | 12 | - | High Current | |
| P1.3 | 19 | 13 | 9 | 11 | - | High Current | |
| P1.4 | 18 | 12 | - | - | - | High Current | |
| P1.5 | 17 | 11 | - | - | - | High Current | |
| P1.6 | 16 | - | - | - | - | STD_IN OUT | |
| P2.0 | 1 | 35 | 25 | 1 | 15 | STD_IN OUT/AN | |

### 2.2.3 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

**Table 8 Hardware Controlled I/O Function Description**

| Function | Outputs | Inputs | Pull Control | |
|---|---|---|---|---|
| | **HWO0** | **HWI0** | **HW0_PD** | **HW0_PU** |
| P0.0 | MODB.OUT | MODB.INA | | |
| Pn.y | | | $\overline{\text{MODC.OUT}}$ | MODC.OUT |

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the **Hardware Controlled I/O Functions** table for the complete hardware I/O and pull control function mapping.

## 3.2 DC Parameters

### 3.2.1 Input/Output Characteristics

**Table 14** provides the characteristics of the input/output pins of the XMC1300.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

**Table 14 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Output low voltage on port pins (with standard pads) | $V_{OLP}$ | CC | – | 1.0 | V | $I_{OL}$ = 11 mA (5 V)<br>$I_{OL}$ = 7 mA (3.3 V) |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA (5 V)<br>$I_{OL}$ = 3.5 mA (3.3 V) |
| Output low voltage on high current pads | $V_{OLP1}$ | CC | – | 1.0 | V | $I_{OL}$ = 50 mA (5 V)<br>$I_{OL}$ = 25 mA (3.3 V) |
| | | | – | 0.32 | V | $I_{OL}$ = 10 mA (5 V) |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA (3.3 V) |
| Output high voltage on port pins (with standard pads) | $V_{OHP}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -10 mA (5 V)<br>$I_{OH}$ = -7 mA (3.3 V) |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -4.5 mA (5 V)<br>$I_{OH}$ = -2.5 mA (3.3 V) |
| Output high voltage on high current pads | $V_{OHP1}$ | CC | $V_{DDP}$ - 0.32 | – | V | $I_{OH}$ = -6 mA (5 V) |
| | | | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -8 mA (3.3 V) |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -4 mA (3.3 V) |
| Input low voltage on port pins (Standard Hysteresis) | $V_{ILPS}$ | SR | – | 0.19 × $V_{DDP}$ | V | CMOS Mode (5 V, 3.3 V & 2.2 V) |

### 3.2.4 Analog Comparator Characteristics

**Table 17** below shows the Analog Comparator characteristics.

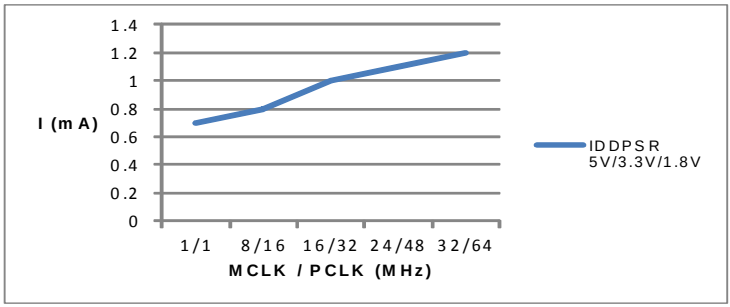
*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 17 Analog Comparator Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Notes/ Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input Voltage | $V_{CMP}$ | SR | -0.05 | – | $V_{DDP}$ + 0.05 | V | |
| Input Offset | $V_{CMPOFF}$ | CC | – | +/-3 | – | mV | High power mode $\Delta V_{CMP}$ < 200 mV |
| | | | – | +/-20 | – | mV | Low power mode $\Delta V_{CMP}$ < 200 mV |
| Propagation Delay[1)] | $t_{PDELAY}$ | CC | – | 25 | – | ns | High power mode, $\Delta V_{CMP}$ = 100 mV |
| | | | – | 80 | – | ns | High power mode, $\Delta V_{CMP}$ = 25 mV |
| | | | – | 250 | – | ns | Low power mode, $\Delta V_{CMP}$ = 100 mV |
| | | | – | 700 | – | ns | Low power mode, $\Delta V_{CMP}$ = 25 mV |
| Current Consumption | $I_{ACMP}$ | CC | – | 100 | – | µA | First active ACMP in high power mode, $\Delta V_{CMP}$ > 30 mV |
| | | | – | 66 | – | µA | Each additional ACMP in high power mode, $\Delta V_{CMP}$ > 30 mV |
| | | | – | 10 | – | µA | First active ACMP in low power mode |
| | | | – | 6 | – | µA | Each additional ACMP in low power mode |
| Input Hysteresis | $V_{HYS}$ | CC | – | +/-15 | – | mV | |
| Filter Delay[1)] | $t_{FDELAY}$ | CC | – | 5 | – | ns | |

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

**Figure 15** shows typical graphs for sleep mode current for $V_{DDP}$ = 5V, $V_{DDP}$ = 3.3V, $V_{DDP}$ = 1.8V across different clock frequencies.




Condition:
1. TA = +25° C

**Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current $I_{DDPSR}$ over supply voltage $V_{DDP}$ for different clock frequencies**

Table 20 provides the active current consumption of some modules operating at 5 V power supply at 25° C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

**Table 20 Typical Active Current Consumption**

| Active Current Consumption | Symbol | Limit Values | Unit | Test Condition |
|---|---|---|---|---|
| | | Typ. | | |
| Baseload current | $I_{CPUDDC}$ | 5.04 | mA | Modules including Core, SCU, PORT, memories, ANATOP[1)] |
| VADC and SHS | $I_{ADCDDC}$ | 3.4 | mA | Set CGATCLR0.VADC to 1[2)] |
| USIC0 | $I_{USIC0DDC}$ | 0.87 | mA | Set CGATCLR0.USIC0 to 1[3)] |
| CCU40 | $I_{CCU40DDC}$ | 0.94 | mA | Set CGATCLR0.CCU40 to 1[4)] |
| CCU80 | $I_{CCU80DDC}$ | 0.42 | mA | Set CGATCLR0.CCU80 to 1[5)] |
| POSIF0 | $I_{PIF0DDC}$ | 0.26 | mA | Set CGATCLR0.POSIF0 to 1[6)] |
| BCCU0 | $I_{BCCU0DDC}$ | 0.24 | mA | Set CGATCLR0.BCCU0 to 1[7)] |
| MATH | $I_{MATHDDC}$ | 0.35 | mA | Set CGATCLR0.MATH to 1[8)] |
| WDT | $I_{WDTDDC}$ | 0.03 | mA | Set CGATCLR0.WDT to 1[9)] |
| RTC | $I_{RTCDDC}$ | 0.01 | mA | Set CGATCLR0.RTC to 1[10)] |

1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode

3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms

4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle

5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%

6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode

7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s

8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11

9) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s

10) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

### 3.2.7 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 21 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per page / sector | $t_{ERASE}$ CC | 6.8 | 7.1 | 7.6 | ms | |
| Program time per block | $t_{PSER}$ CC | 102 | 152 | 204 | µs | |
| Wake-Up time | $t_{WU}$ CC | – | 32.2 | – | µs | |
| Read time per word | $t_a$ CC | – | 50 | – | ns | |
| Data Retention Time | $t_{RET}$ CC | 10 | – | – | years | Max. 100 erase / program cycles |
| Flash Wait States [1] | $N_{WSFLASH}$ CC | 0 | 0 | 0 | | $f_{MCLK}$ = 8 MHz |
| | | 0 | 1 | 1 | | $f_{MCLK}$ = 16 MHz |
| | | 1 | 1.3 | 2 | | $f_{MCLK}$ = 32 MHz |
| Fixed Flash Wait States configured in bit NVM_NVMCONF.WS | $N_{FWSFLASH}$ SR | 0 | 0 | 1 | | NVM_CONFIG1.FIXWS = $1_B$, $f_{MCLK} \leq$ 16 MHz |
| | | 1 | 1 | 1 | | NVM_CONFIG1.FIXWS = $1_B$, 16 MHz < $f_{MCLK} \leq$ 32 MHz |
| Erase Cycles | $N_{ECYC}$ CC | – | – | $5*10^4$ | cycles | Sum of page and sector erase cycles |
| Total Erase Cycles | $N_{TECYC}$ CC | – | – | $2*10^6$ | cycles | |

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

## 3.3 AC Parameters

### 3.3.1 Testing Waveforms

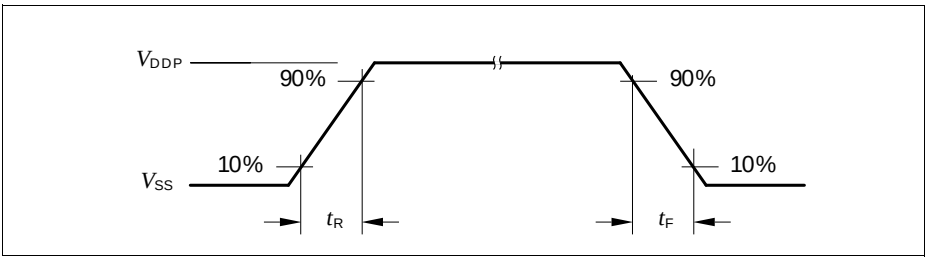



**Figure 16 Rise/Fall Time Parameters**

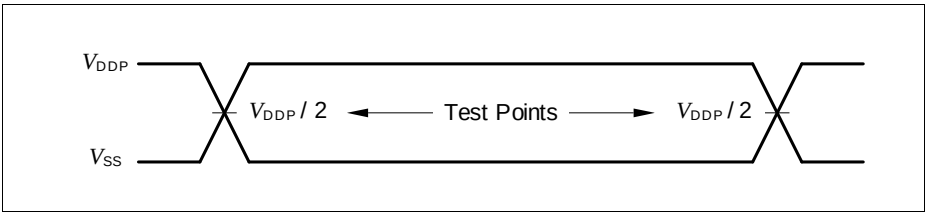



**Figure 17 Testing Waveform, Output Delay**

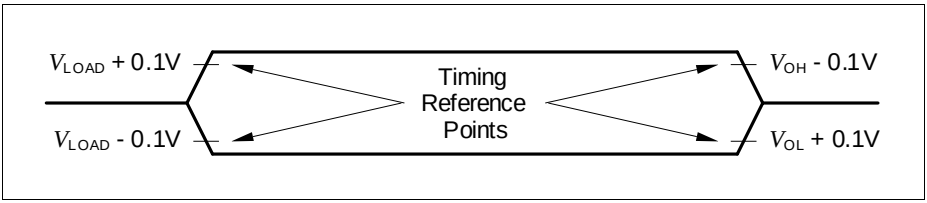



**Figure 18 Testing Waveform, Output High Impedance**

### 3.3.2 Power-Up and Supply Monitoring Characteristics

**Table 22** provides the characteristics of the power-up and supply monitoring in XMC1300.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while $V_{DDP}$ is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 22 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DDP}$ ramp-up time | $t_{RAMPUP}$ SR | $V_{DDP}$/ $S_{VDDPrise}$ | – | $10^7$ | µs | |
| $V_{DDP}$ slew rate | $S_{VDDPOP}$ SR | 0 | – | 0.1 | V/µs | Slope during normal operation |
| | $S_{VDDP10}$ SR | 0 | – | 10 | V/µs | Slope during fast transient within +/- 10% of $V_{DDP}$ |
| | $S_{VDDPrise}$ SR | 0 | – | 10 | V/µs | Slope during power-on or restart after brownout event |
| | $S_{VDDPfall}$ [1] SR | 0 | – | 0.25 | V/µs | Slope during supply falling out of the +/-10% limits[2] |
| $V_{DDP}$ prewarning voltage | $V_{DDPPW}$ CC | 2.1 | 2.25 | 2.4 | V | ANAVDEL.VDEL_SELECT = $00_B$ |
| | | 2.85 | 3 | 3.15 | V | ANAVDEL.VDEL_SELECT = $01_B$ |
| | | 4.2 | 4.4 | 4.6 | V | ANAVDEL.VDEL_SELECT = $10_B$ |

### 3.3.3 On-Chip Oscillator Characteristics

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23** provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

**Table 23 64 MHz DCO1 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | – | 64 | – | MHz | under nominal conditions[1] after trimming |
| Accuracy[2] | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature ($T_A$ = 0 °C to 85 °C) |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature ($T_A$ = -40 °C to 105 °C) |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

2) The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

**Figure 20** shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

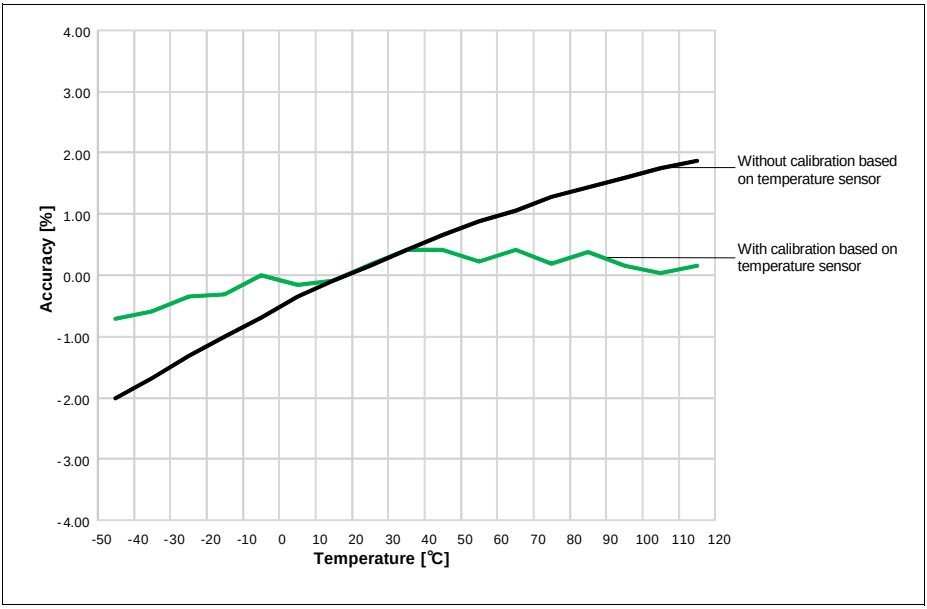



**Figure 20 Typical DCO1 accuracy over temperature**

**Table 24** provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

**Table 24 32 kHz DCO2 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | – | 32.75 | – | kHz | under nominal conditions[1] after trimming |
| Accuracy | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C) |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C) |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

### 3.3.5 SPD Timing Requirements

The optimum SPD decision time between $0_B$ and $1_B$ is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

**Table 26 Optimum Number of Sample Clocks for SPD**

| Sample Freq. | Sampling Factor | Sample Clocks $0_B$ | Sample Clocks $1_B$ | Effective Decision Time[1)] | Remark |
|---|---|---|---|---|---|
| 8 MHz | 4 | 1 to 5 | 6 to 12 | 0.69 µs | The other closest option (0.81 µs) for the effective decision time is less robust. |

1) Nominal sample frequency period multiplied with 0.5 + (max. number of $0_B$ sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

### 3.3.6 Peripheral Timings

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: Operating Conditions apply.*

**Table 27 USIC SSC Master Mode Timing**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| SCLKOUT master clock period | $t_{CLK}$ | CC | 62.5 | – | – | ns | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ | CC | 80 | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ | CC | 0 | – | – | ns | |
| Data output DOUT[3:0] valid time | $t_3$ | CC | -10 | – | 10 | ns | |
| Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge | $t_4$ | SR | 80 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from SCLKOUT receive edge | $t_5$ | SR | 0 | – | – | ns | |

# 4 Package and Reliability

The XMC1300 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

## 4.1 Package Parameters

**Table 33** provides the thermal characteristics of the packages used in XMC1300.

**Table 33 Thermal Characteristics of the Packages**

| Parameter | Symbol | Limit Values | | Unit | Package Types |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Exposed Die Pad Dimensions | Ex × Ey CC | - | 2.7 × 2.7 | mm | PG-VQFN-24-19 |
| | | - | 3.7 × 3.7 | mm | PG-VQFN-40-13 |
| Thermal resistance Junction-Ambient | $R_{\Theta JA}$ CC | - | 104.6 | K/W | PG-TSSOP-16-8[1)] |
| | | - | 83.2 | K/W | PG-TSSOP-28-16[1)] |
| | | - | 70.3 | K/W | PG-TSSOP-38-9[1)] |
| | | - | 46.0 | K/W | PG-VQFN-24-19[1)] |
| | | - | 38.4 | K/W | PG-VQFN-40-13[1)] |

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

*Note: For electrical reasons, it is required to connect the exposed pad to the board ground $V_{SSP}$, independent of EMC and thermal requirements.*

### 4.1.1 Thermal Considerations

When operating the XMC1300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

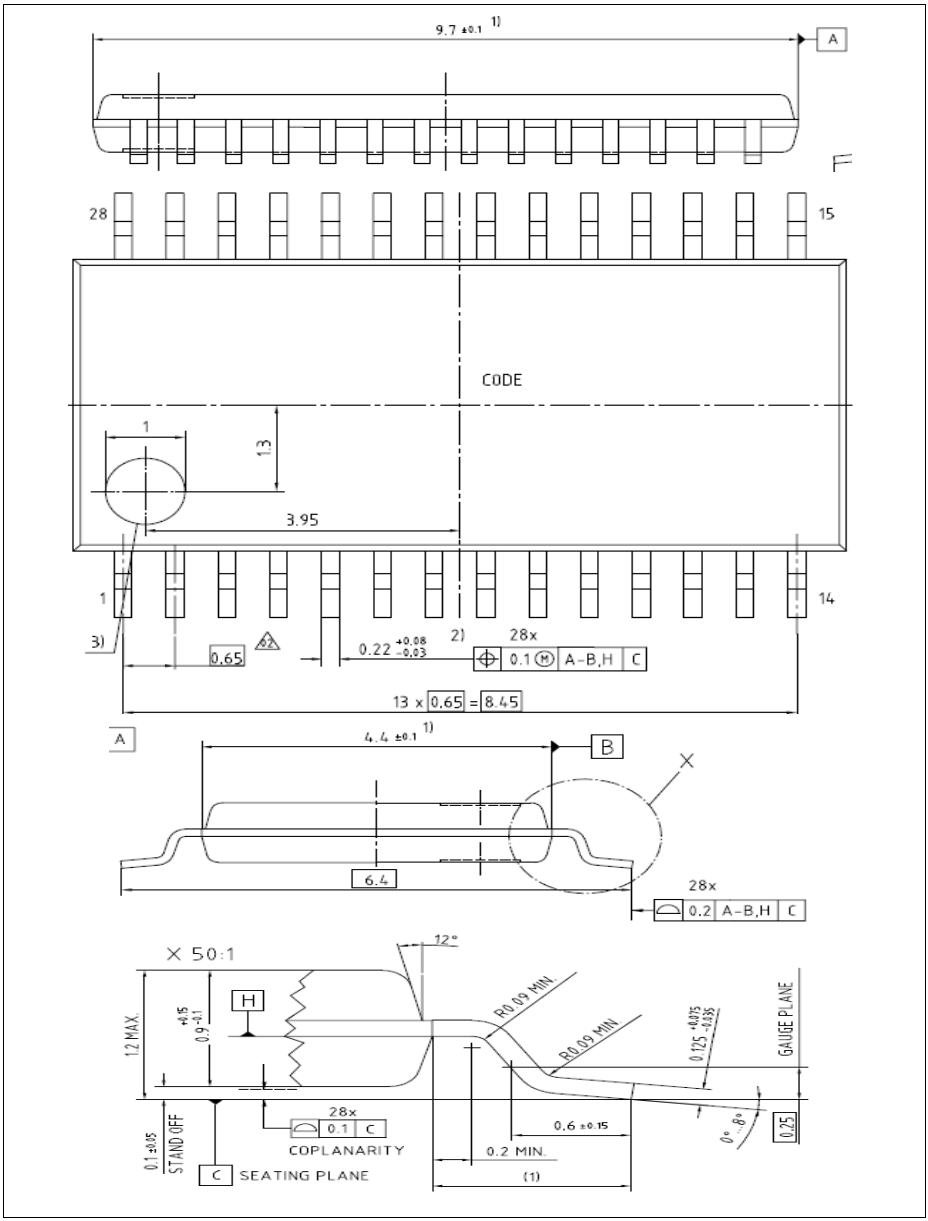



**Figure 27 PG-TSSOP-28-16**