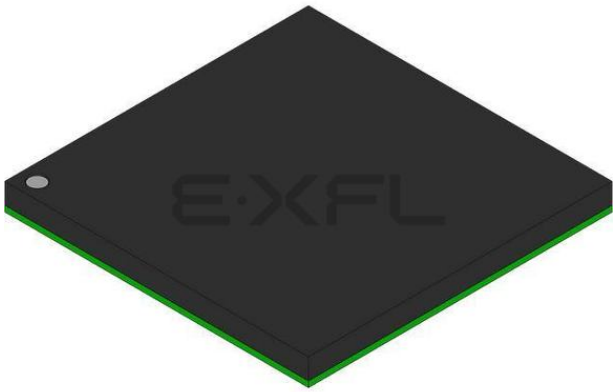

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc94mx21dvkn3

- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Target Applications

The i.MX21 is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers based on the popular Palm OS platform, and messaging applications.

1.3 Reference Documentation

The following documents are required for a complete description of the i.MX21 and are necessary to design properly with the device. Especially for those not familiar with the ARM926EJ-S processor the following documents are helpful when used in conjunction with this manual.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM7TDMI Data Sheet (ARM Ltd., order number ARM DDI 0029)

ARM920T Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

MC9328MX21 Product Brief (order number MC9328MX21P)

MC9328MX21 Reference Manual (order number MC9328MX21RM)

The Freescale manuals are available on the Freescale Semiconductor Web site at http://www.freescale.com. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

1.4 Ordering Information

Table 1 provides ordering information for the device. See Table 4 on page 14 for core frequency and supply voltage requirements.

Table 1. Ordering Information

Part Order Number	Package Size	Package Type	Operating Range
MC94MX21DVKN3	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	-30°C–70°C

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
CSPI	
CSPI1_MOSI	Master Out/Slave In signal
CSPI1_MISO	Master In/Slave Out signal
CSPI1_SS[2:0]	Slave Select (Selectable polarity) signal. CSPI1_SS2 is also multiplexed with USBG_RXDAT and CSPI1_SS1 is multiplexed with $\overline{\text{EXT\_DMAGRANT}}$.
CSPI1_SCLK	Serial Clock signal
CSPI1_$\overline{\text{RDY}}$	Serial Data Ready signal. Also multiplexed with $\overline{\text{EXT\_DMAREQ}}$.
CSPI2_MOSI	Master Out/Slave In signal. This signal is multiplexed with USBH2_TXDP signal of USB OTG.
CSPI2_MISO	Master In/Slave Out signal. This signal is multiplexed with USBH2_TXDM signal of USB OTG.
CSPI2_SS[2:0]	Slave Select (Selectable polarity) signals. These signals are multiplexed with USBH2_FS, USBH2_RXDP and USBH2_RXDM signal of USB OTG
CSPI2_SCLK	Serial Clock signal. This signal is multiplexed with $\overline{\text{USBH2\_OE}}$ signal of USB OTG
CSPI3_MOSI	Master Out/Slave In signal. This signal is multiplexed with SD1_CMD.
CSPI3_MISO	Master In/Slave Out signal. This signal is multiplexed with SD1_D0.
CSPI3_SS	Slave Select (Selectable polarity) signal multiplexed with SD1_D3.
CSPI3_SCLK	Serial Clock signal. This signal is multiplexed with SD1_CLK.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to all 3 timers simultaneously. This signal is muxed with the Walk-up Guard Mode $\overline{\text{WKGD}}$ signal in the PLL, Clock, and Reset Controller module.
TOUT1 (or simply TOUT)	Timer Output signal from General Purpose Timer1 (GPT1). This signal is multiplexed with SYS_CLK1 and SYS_CLK2 signal of SSI1 and SSI2. The pin name of this signal is simply TOUT.
TOUT2	Timer Output signal from General Purpose Timer1 (GPT2). This signal is multiplexed with PWMO.
TOUT3	Timer Output signal from General Purpose Timer1 (GPT3). This signal is multiplexed with PWMO.
USB On-The-Go	
$\overline{\text{USB\_BYP}}$	USB Bypass input active low signal. This signal can only be used for USB function, not for GPIO.
USB_PWR	USB Power output signal
$\overline{\text{USB\_OC}}$	USB Over current input signal. This signal can only be used for USB function, not for GPIO.
USBG_RXDP	USB OTG Receive Data Plus input signal. This signal is muxed with SLCDC1_DAT15.
USBG_RXDM	USB OTG Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT14.
USBG_TXDP	USB OTG Transmit Data Plus output signal. This signal is muxed with SLCDC1_DAT13.
USBG_TXDM	USB OTG Transmit Data Minus output signal. This signal is muxed with SLCDC1_DAT12.
USBG_RXDAT	USB OTG Transceiver differential data receive signal. Multiplexed with CSPI1_SS2.
$\overline{\text{USBG\_OE}}$	USB OTG Output Enable signal. This signal is muxed with SLCDC1_DAT11.
$\overline{\text{USBG\_ON}}$	USB OTG Transceiver ON output signal. This signal is muxed with SLCDC1_DAT9.
USBG_FS	USB OTG Full Speed output signal. This signal is multiplexed with external transceiver $\overline{\text{USBG\_TXR\_INT}}$ signal of USB OTG. This signal is muxed with SLCDC1_DAT10.

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V
Input leakage current (no pull-up or pull-down)	I_{in}	V_{in} = 0 or NVDD	–	–	±1	µA
I/O leakage current	I_{OZ}	$V_{I/O}$ = NVDD or 0 I/O = High impedance state	–	–	±5	µA

1. Data labeled Typical is not guaranteed, but is intended as an indication of the IC's potential performance.
2. For DSCR definition refer to the System Control chapter in the reference manual.

Table 6 shows the input and output capacitance for the device.

Table 6. Input/Output Capacitance

Parameter	Symbol	Min	Typ	Max	Units
Input capacitance	C_i	_	_	5	pF
Output capacitance	C_o	_	_	5	pF

can write data to BMI RxFIFO anytime as CPU or DMA can move data out from RxFIFO much faster than the BMI interface. Overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

3.8.1.1.1 MMD Read BMI Timing

Figure 6 shows the MMD read BMI timing when the MMD drives clock.

On each rising edge of BMI_CLK/CS BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a read cycle. It puts data into the data bus and enables the data out on the rising edge of BMI_CLK/CS if BMI_WRITE is logic high. The BMI_READ_REQ is negated one hclk cycle after the BMI_CLK/CS rising edge of last data read. The MMD cannot issues read command when BMI_READ_REQ is low (no data in TxFIFO).

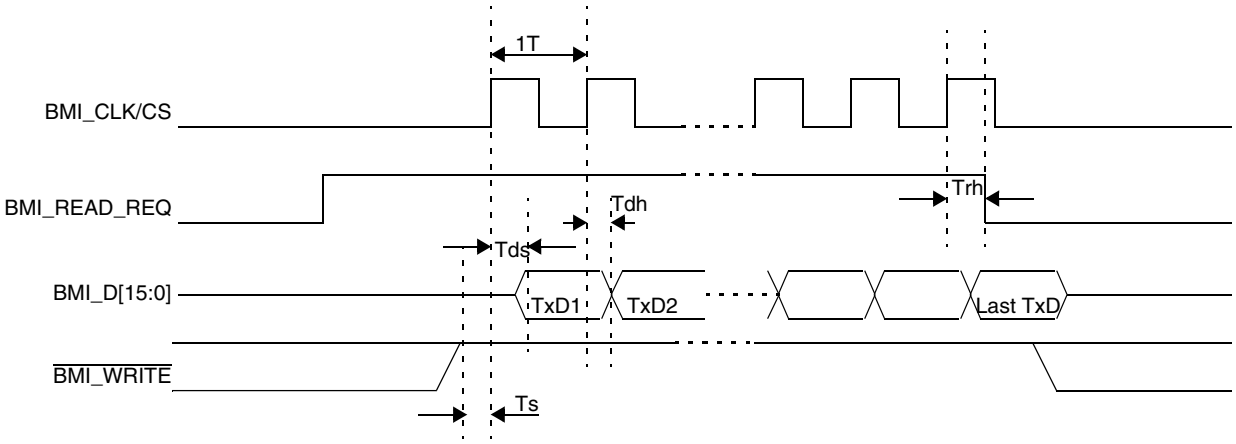


Figure 6. MMD (ATI) Drives Clock, MMD Read BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0,MMD_CLKOUT=0)

Table 13. MMD Read BMI Timing Table when MMD Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Clock period	1T	33.3	–	–	ns
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
read_req hold time	Trh	6	–	24	ns
transfer data setup time	Tds	6	–	14	ns
transfer data hold time	Tdh	6	-	14	ns

Note: All the timings assume that the hclk is running at 133 MHz.

Note: The MIN period of the 1T is assumed that MMD latch data at falling edge.

Note: If the MMD latch data at next rising edge, the ideally max clock can be as much as double, but because the BMI data pads are slow pads and it max frequency can only up to 18MHz, the max clock frequency can only up to 36 MHz.

becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO.

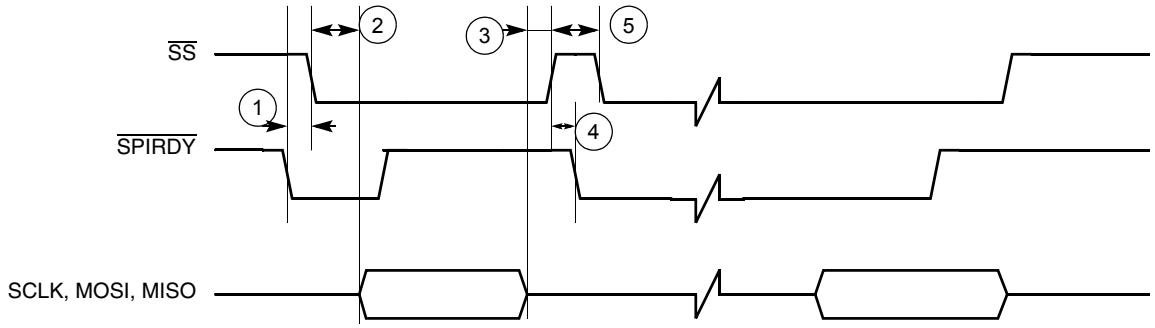


Figure 14. Master CSPI Timing Diagram Using SPI_RDY Edge Trigger

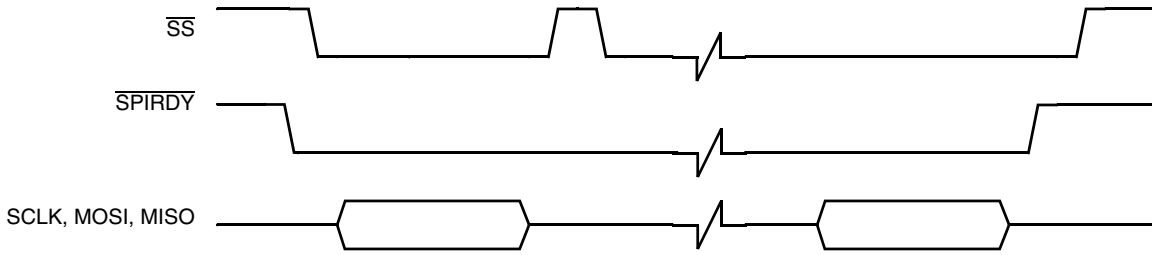


Figure 15. Master CSPI Timing Diagram Using SPI_RDY Level Trigger

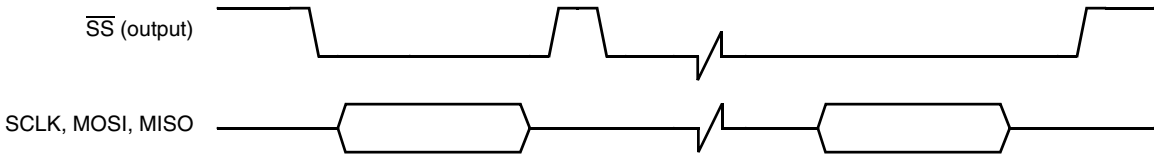


Figure 16. Master CSPI Timing Diagram Ignore SPI_RDY Level Trigger

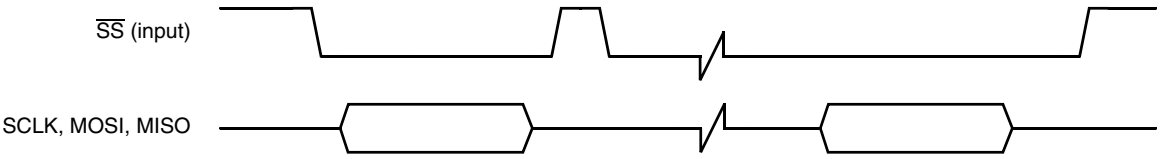


Figure 17. Slave CSPI Timing Diagram FIFO Advanced by BIT COUNT

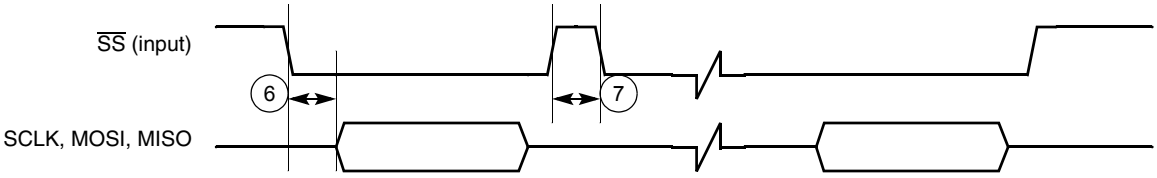


Figure 18. Slave CSPI Timing Diagram FIFO Advanced by SS Rising Edge

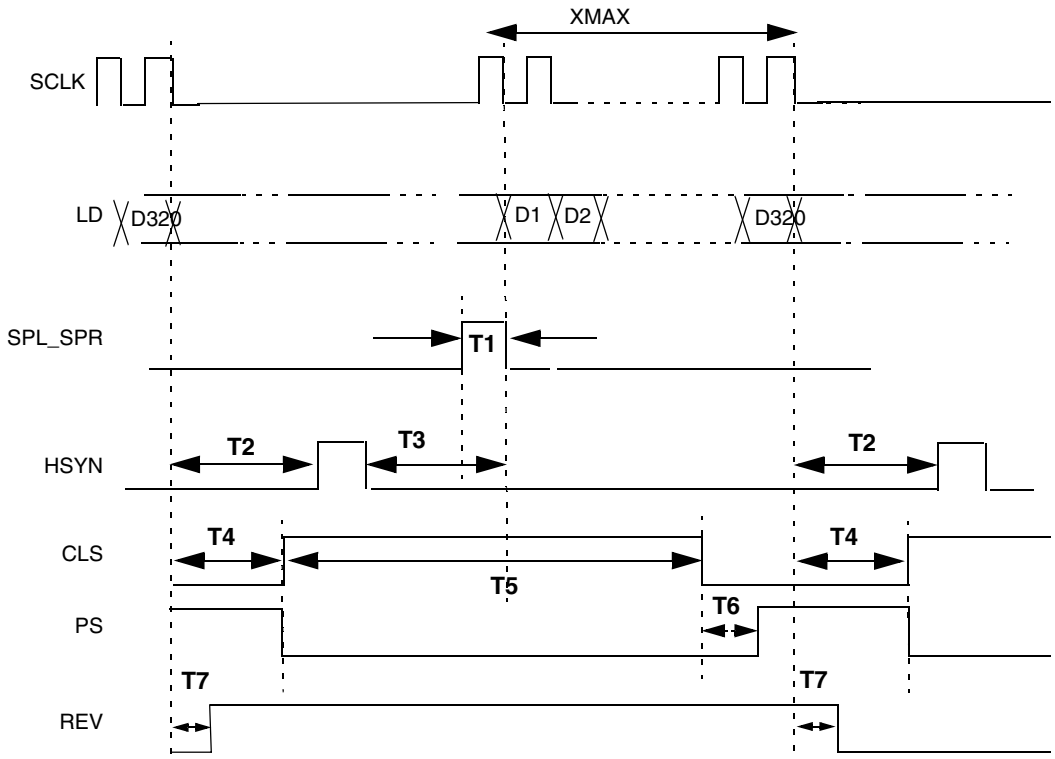


Figure 21. Sharp TFT Panel Timing

Table 21. Sharp TFT Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	SPL/SPR pulse width	–	1	Ts
T2	End of LD of line to beginning of HSYN	1	HWAIT1+1	Ts
T3	End of HSYN to beginning of LD of line	4	HWAIT2 + 4	Ts
T4	CLS rise delay from end of LD of line	3	CLS_RISE_DELAY+1	Ts
T5	CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	PS rise delay from CLS negation	0	PS_RISE_DELAY	Ts
T7	REV toggle delay from last LD of line	1	REV_TOGGLE_DELAY+1	Ts

Note:
- Falling of SPL/SPR aligns with first LD of line.
- Falling of PS aligns with rising edge of CLS.
- REV toggles in every HSYN period.

3.11 Smart LCD Controller

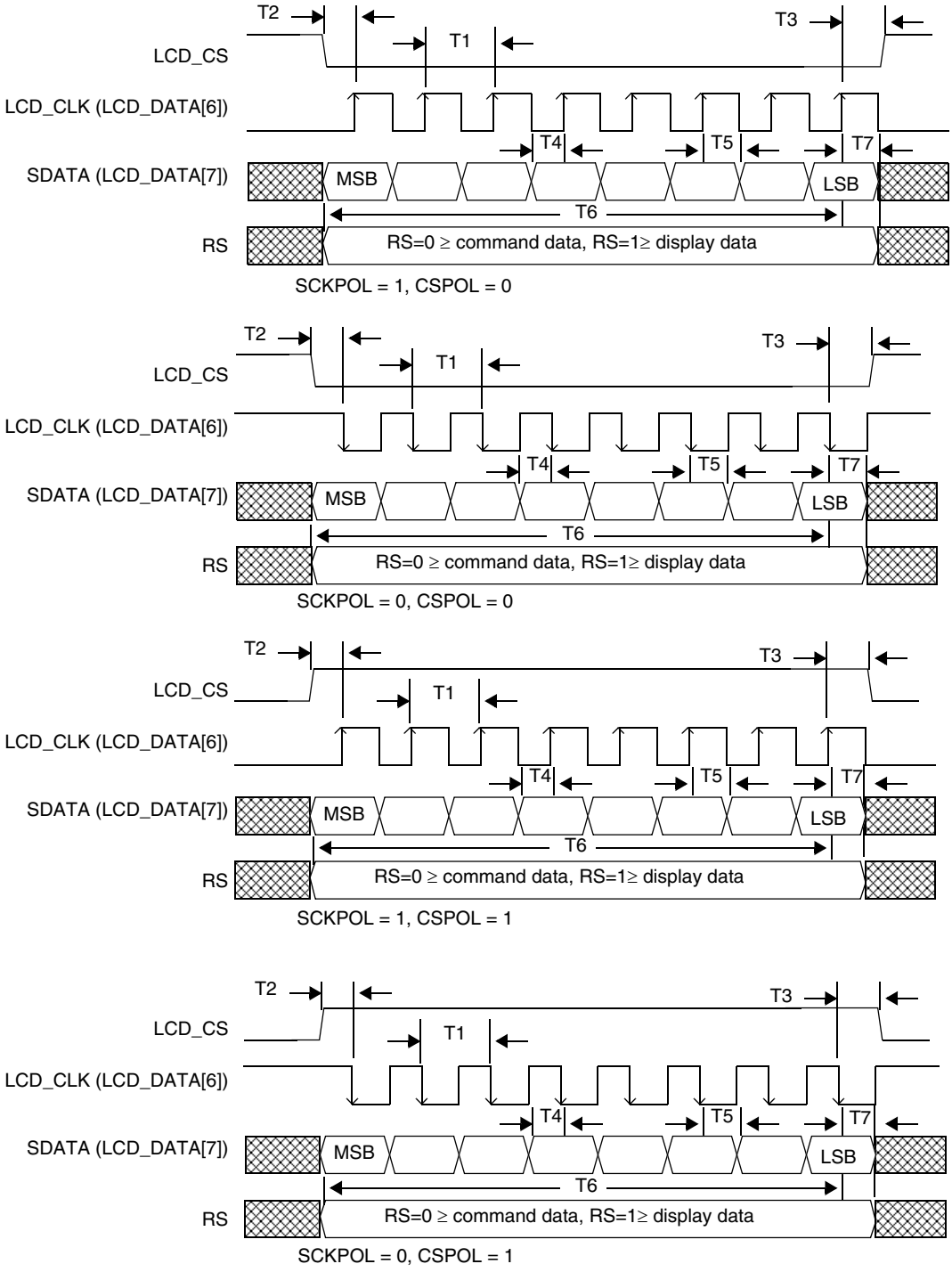
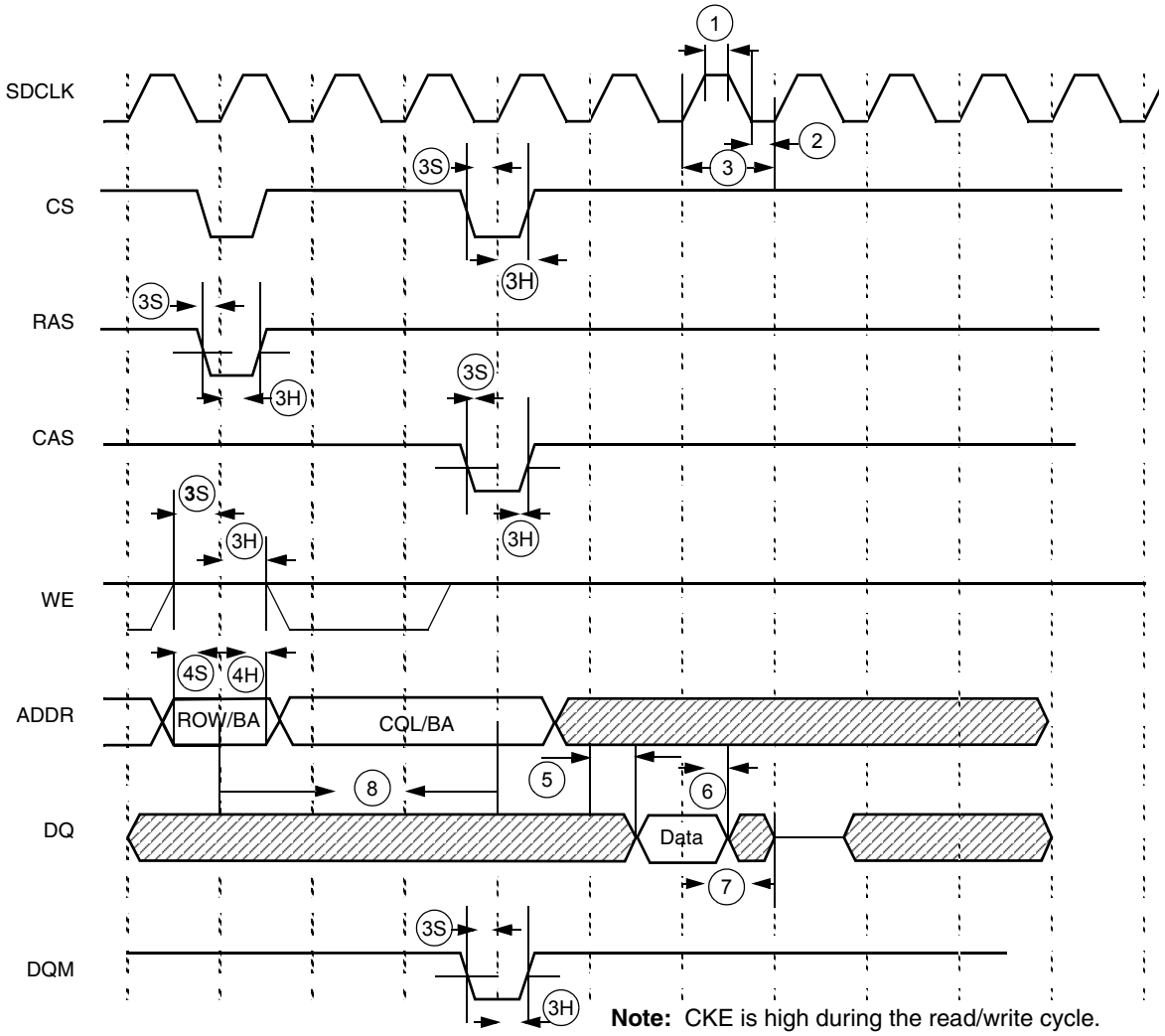


Figure 23. SLCDC Serial Transfer Timing

3.15 SDRAM Memory Controller

The following figures (Figure 38 through Figure 41) and their associated tables specify the timings related to the SDRAMC module in the i.MX21.



Note: CKE is high during the read/write cycle.

Figure 38. SDRAM Read Cycle Timing Diagram

Table 30. SDRAM Read Cycle Timing Parameter

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	SDRAM clock low-level width	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
3S	CS, RAS, CAS, WE, DQM setup time	4.78	–	3	–	ns
3H	CS, RAS, CAS, WE, DQM hold time	3.03	–	2	–	ns

Table 31. SDRAM Write Cycle Timing Parameter

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	SDRAM clock low-level width	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
4	Address setup time	3.67	–	2	–	ns
5	Address hold time	2.95	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP}[2]	–	ns
7	Active to read/write command delay	t_{RCD}[2]	–	t_{RCD}[2]	–	ns
8	Data setup time	3.41	–	2	–	ns
9	Data hold time	2.45	–	2	–	ns

1. Precharge cycle timing is included in the write timing diagram.
2. t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

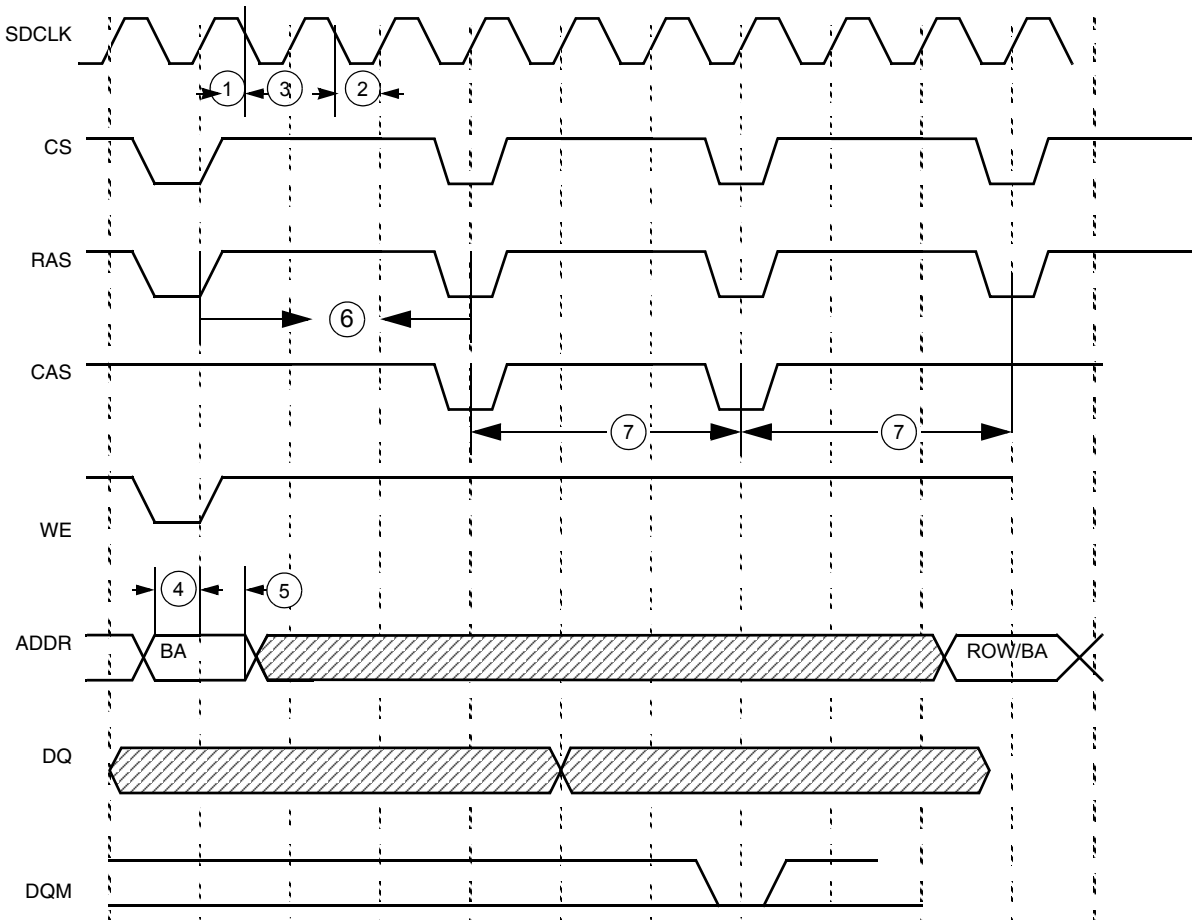


Figure 40. SDRAM Refresh Timing Diagram

Table 32. SDRAM Refresh Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	3.00	–	3	–	ns
2	SDRAM clock low-level width	3.00	–	3	–	ns
3	SDRAM clock cycle time	7.5	–	7.5	–	ns
4	Address setup time	3.67	–	2	–	ns
5	Address hold time	2.95	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP}[1]	–	ns
7	Auto precharge command period	t_{RC}[1]	–	t_{RC}[1]	–	ns

1. t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

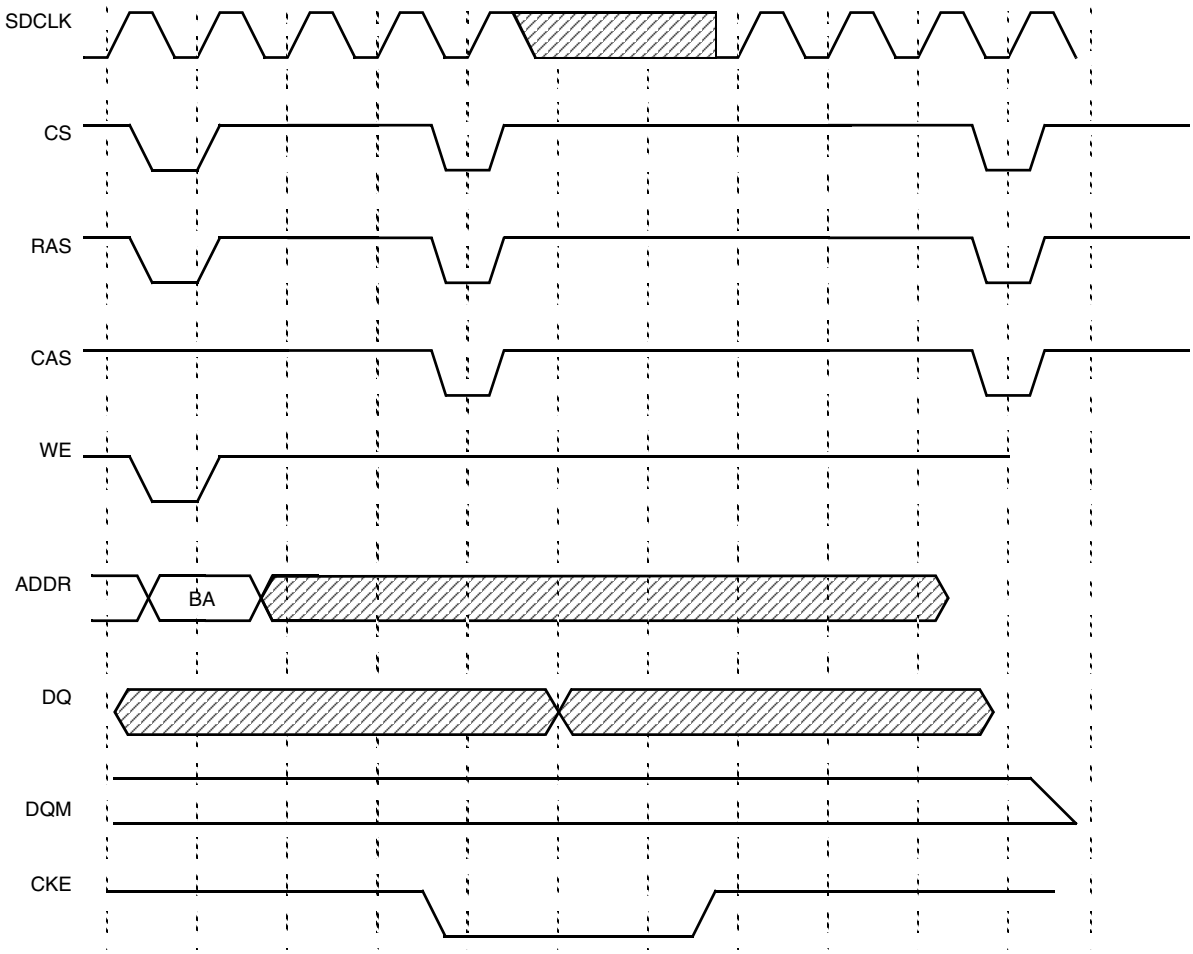


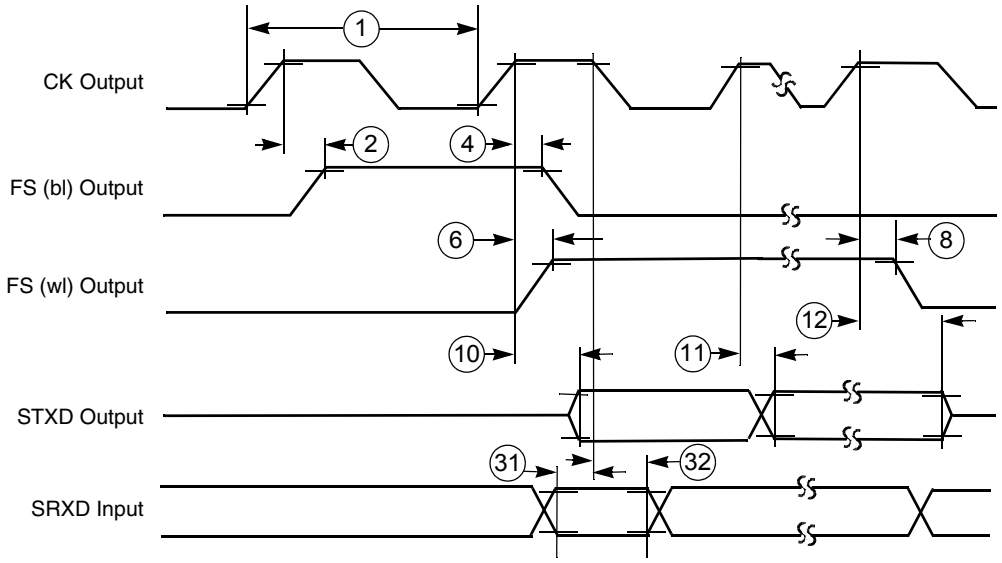
Figure 41. SDRAM Self-Refresh Cycle Timing Diagram

3.16 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 42 through Figure 45.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.

The SSI can be connected to 4 set of ports, SAP, SSI1, SSI2 and SSI3.



Note: SRXD input in synchronous mode only.

Figure 42. SSI Transmitter Internal Clock Timing Diagram

Note: Signals listed with lower case letters are internal to the device.

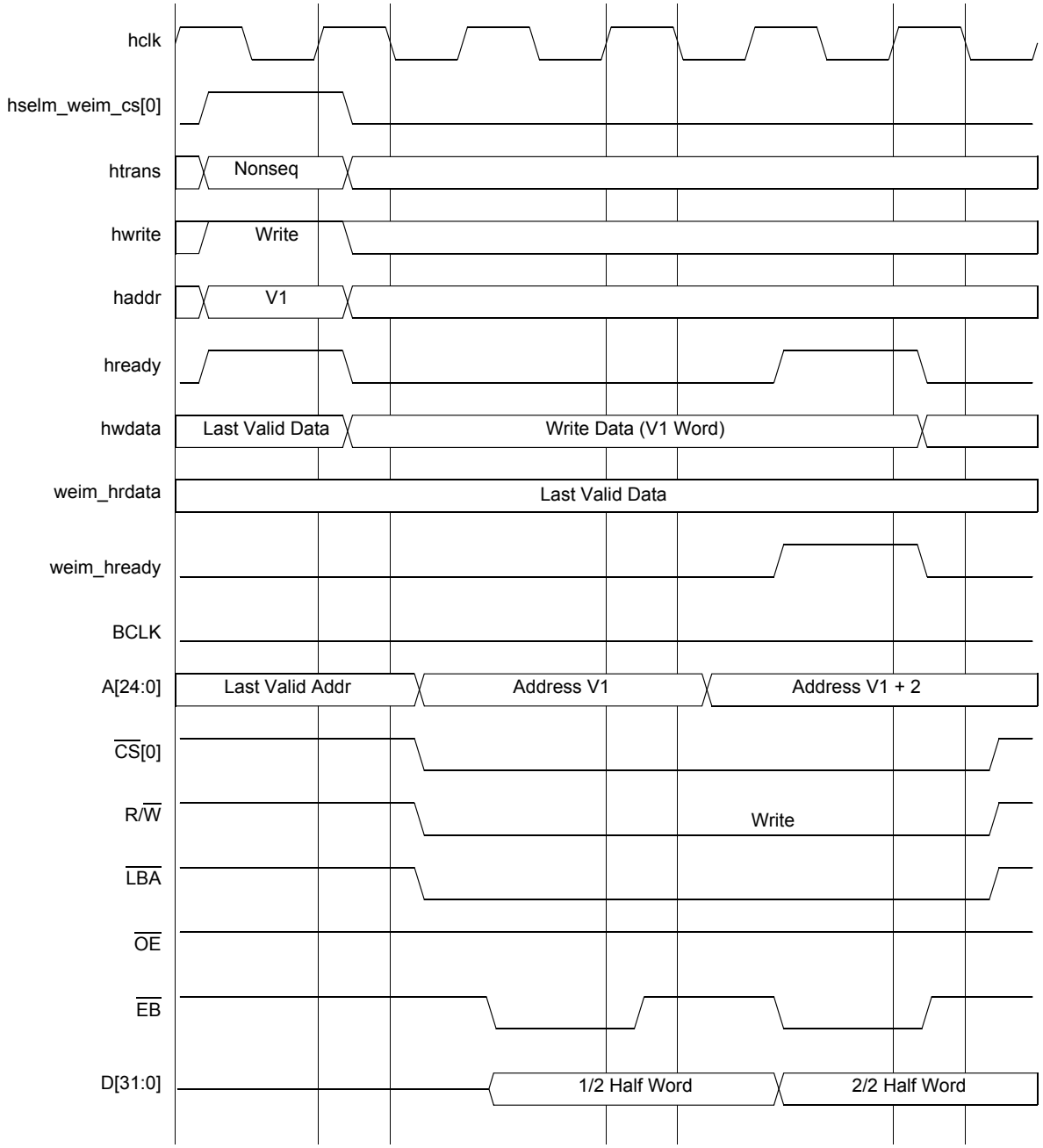


Figure 57. WSC = 1, WEA = 1, WEN = 1, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

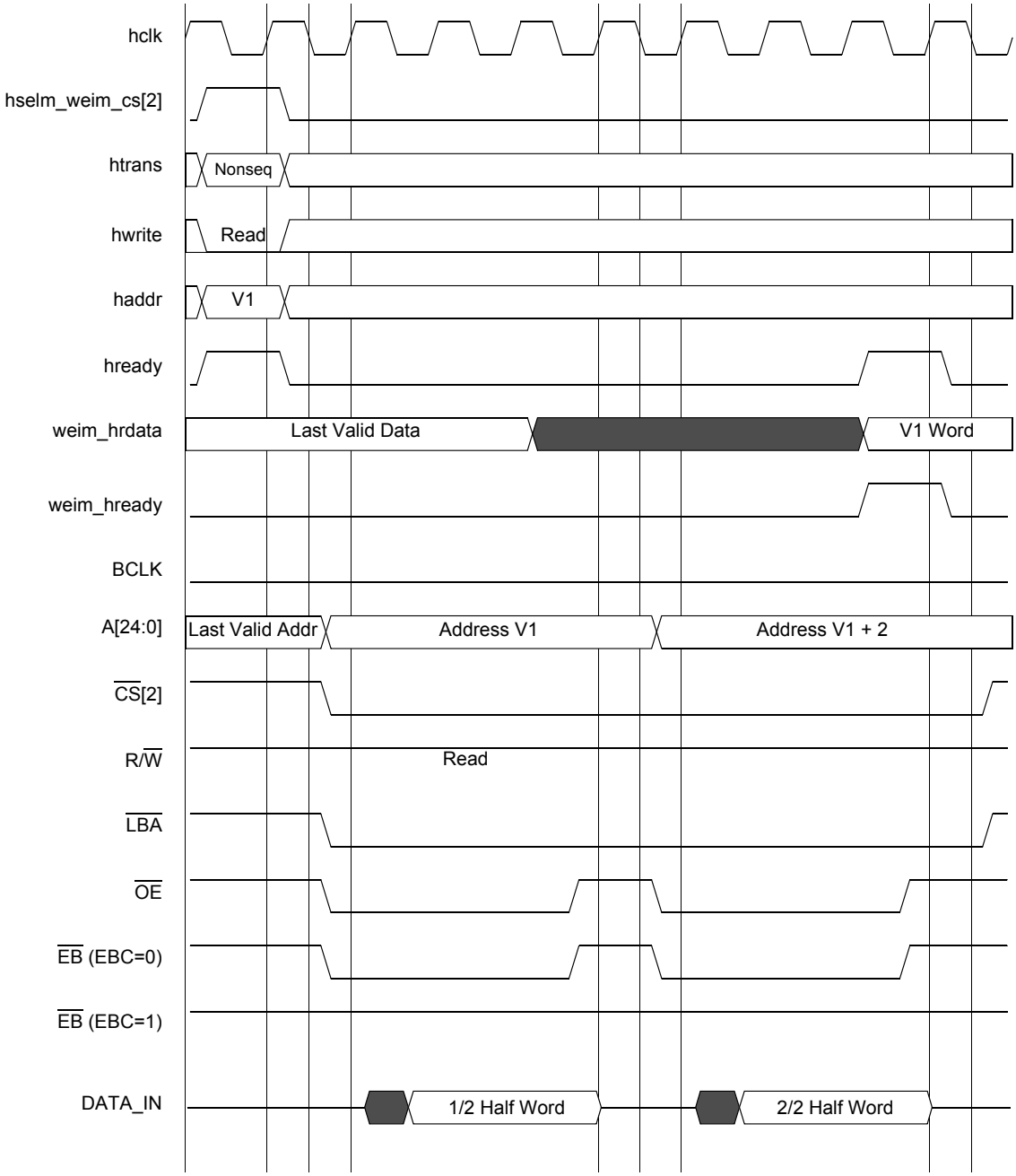


Figure 62. WSC = 3, OEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

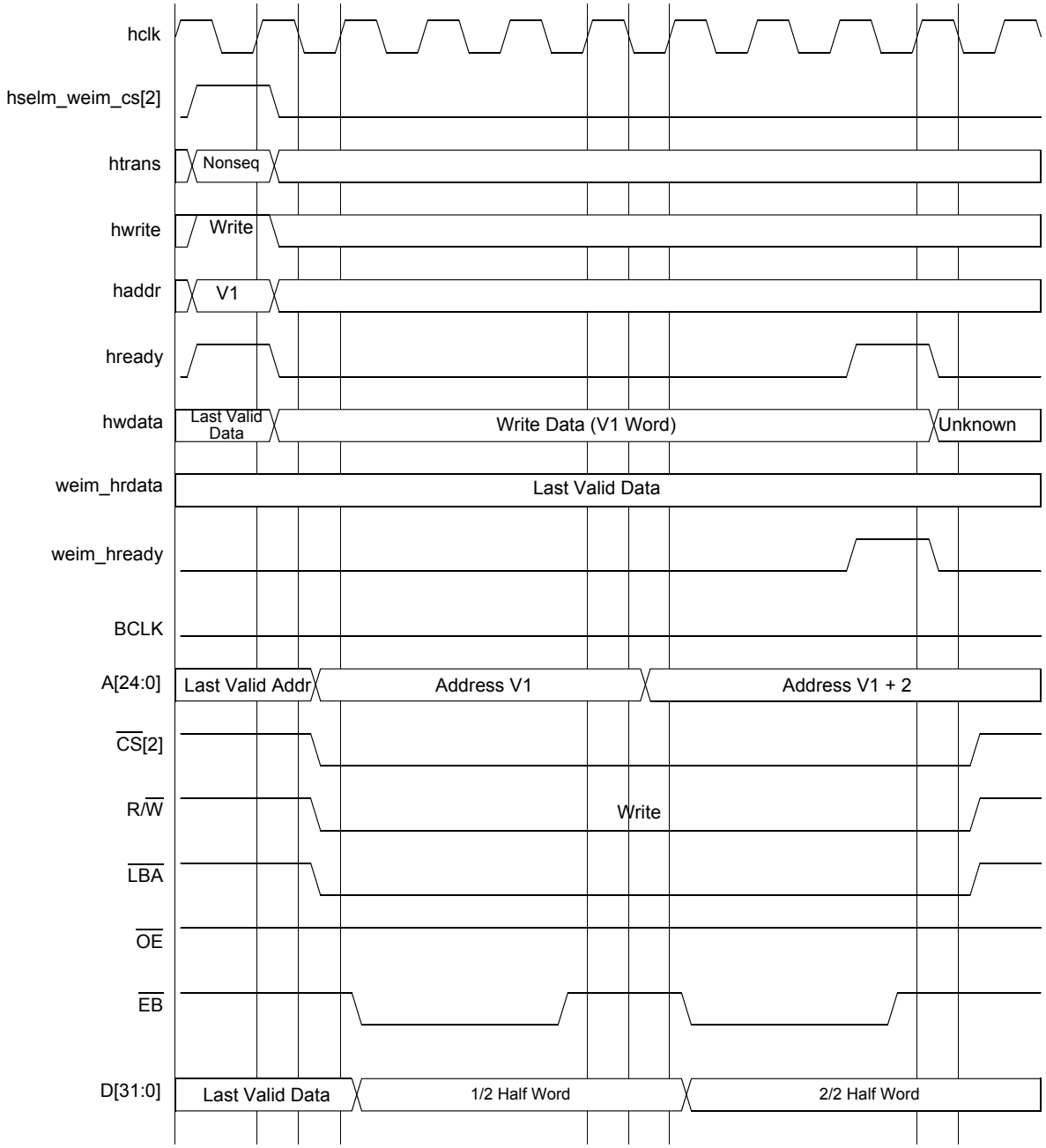


Figure 65. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

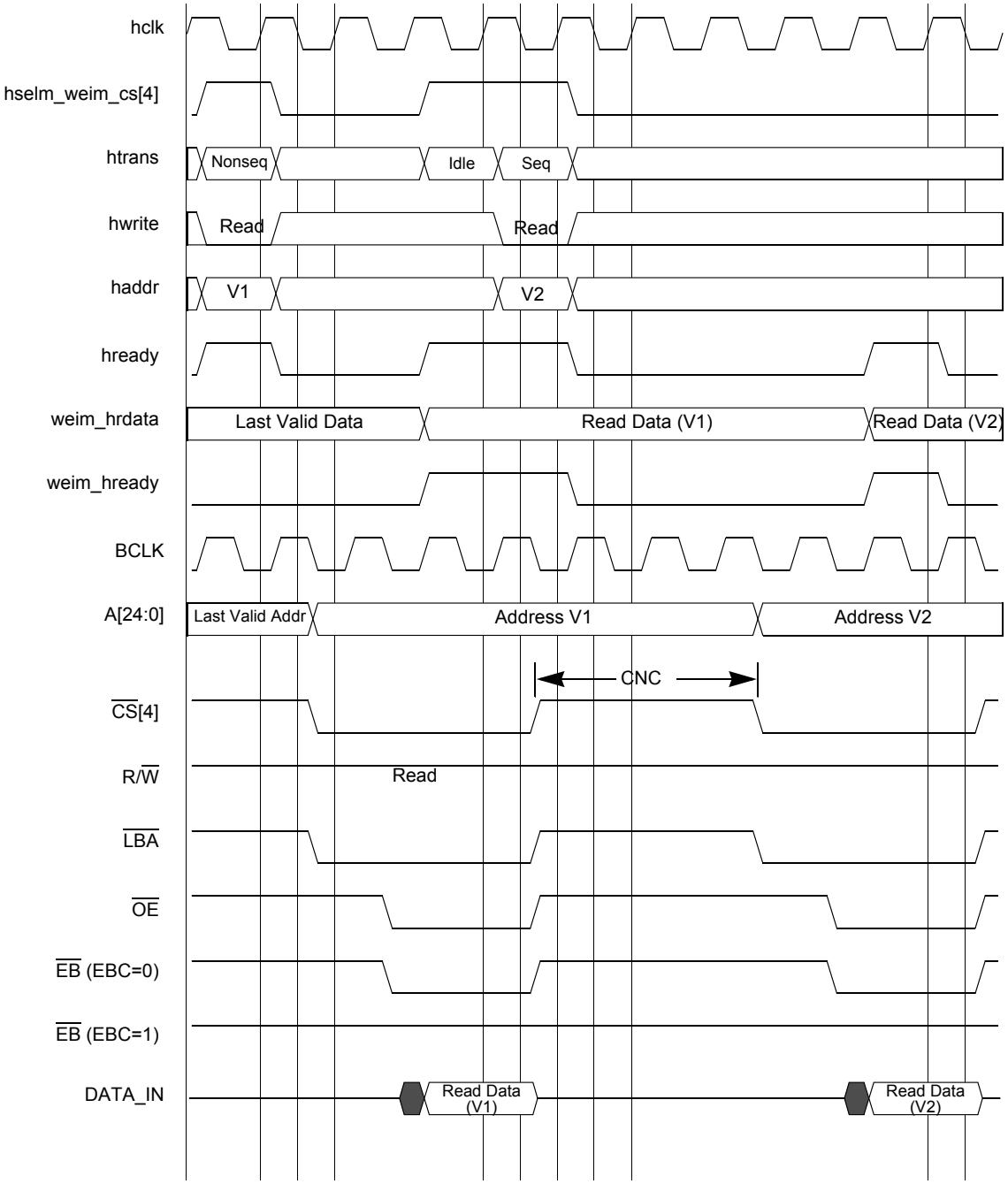


Figure 70. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

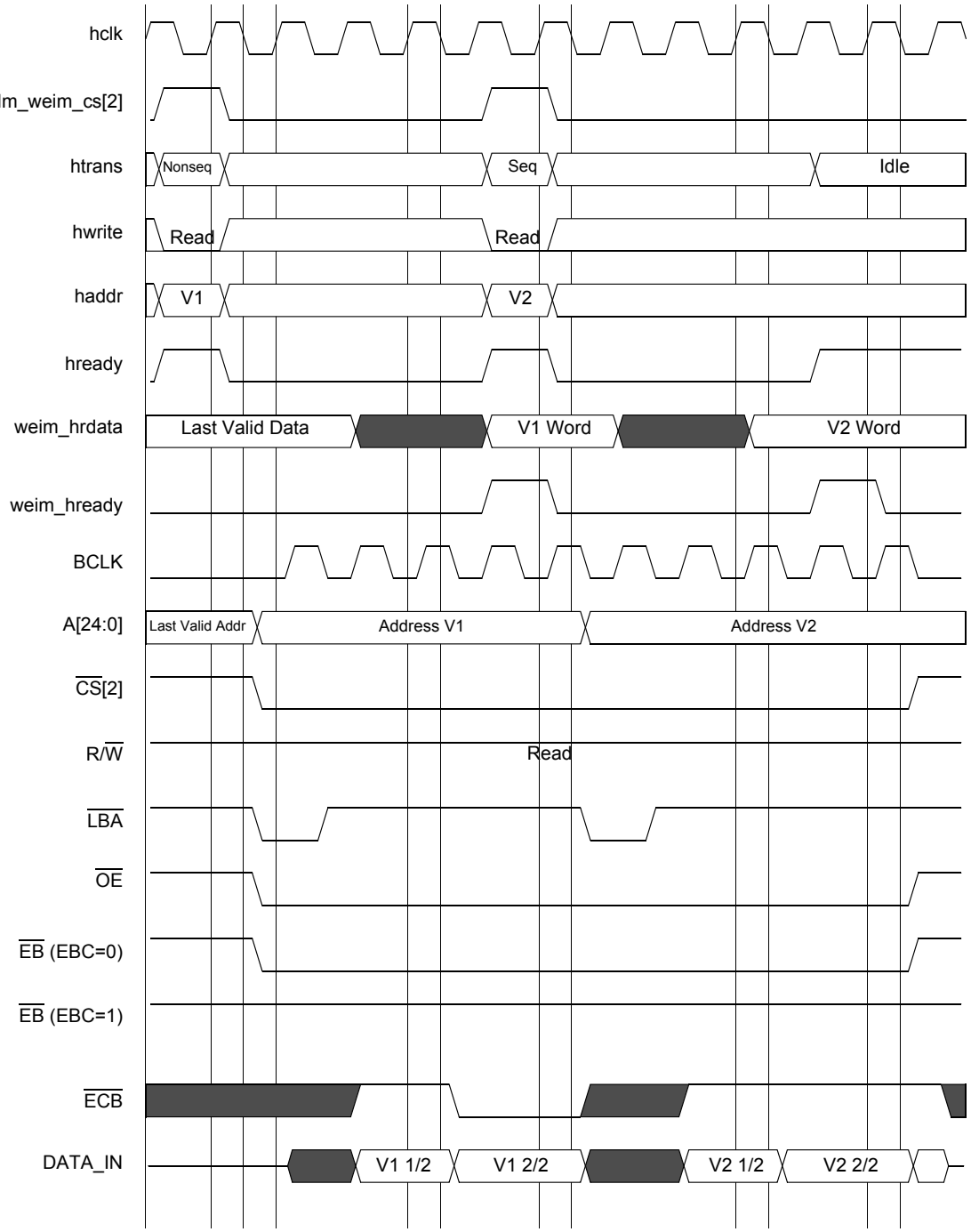


Figure 74. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

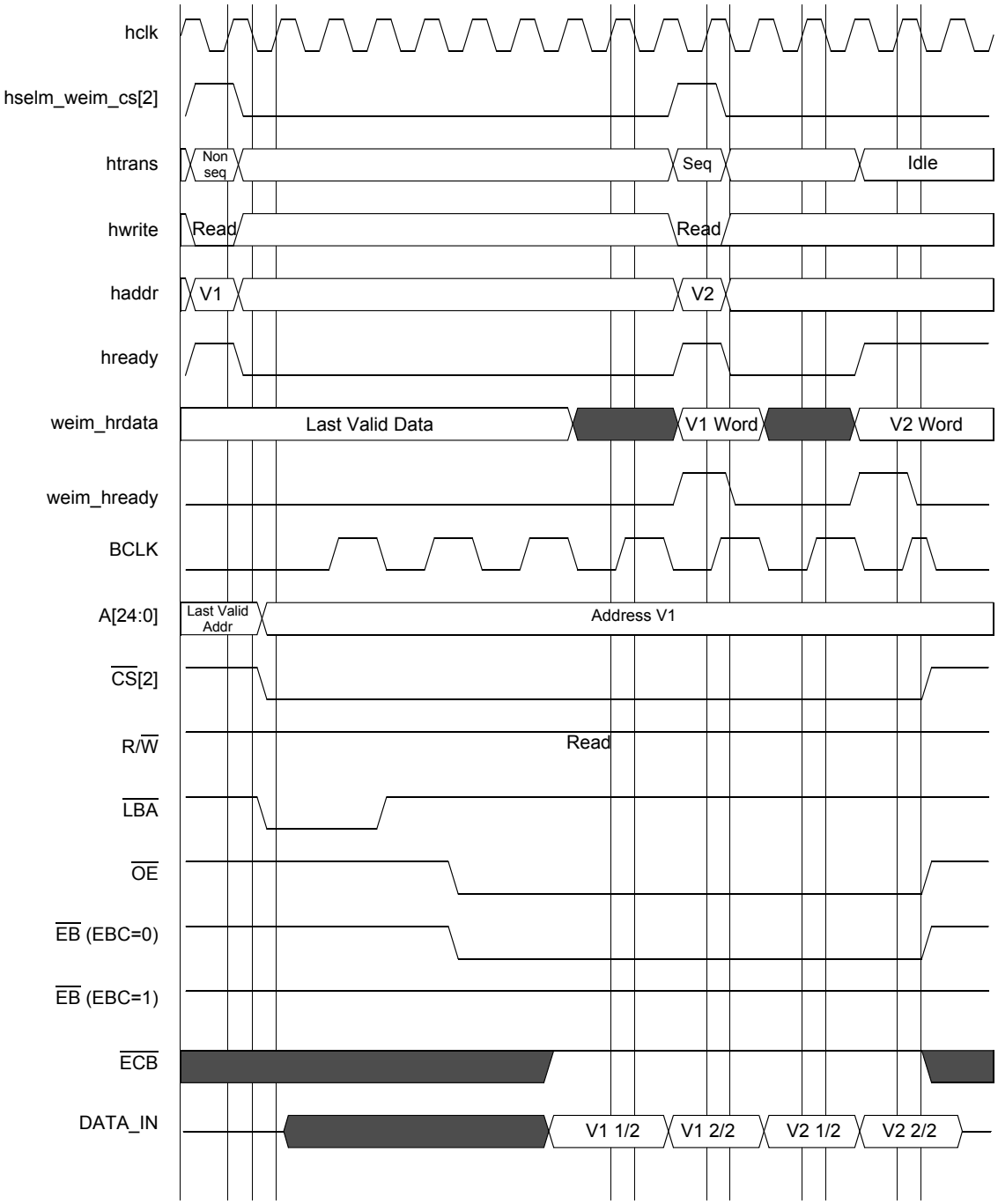


Figure 75. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

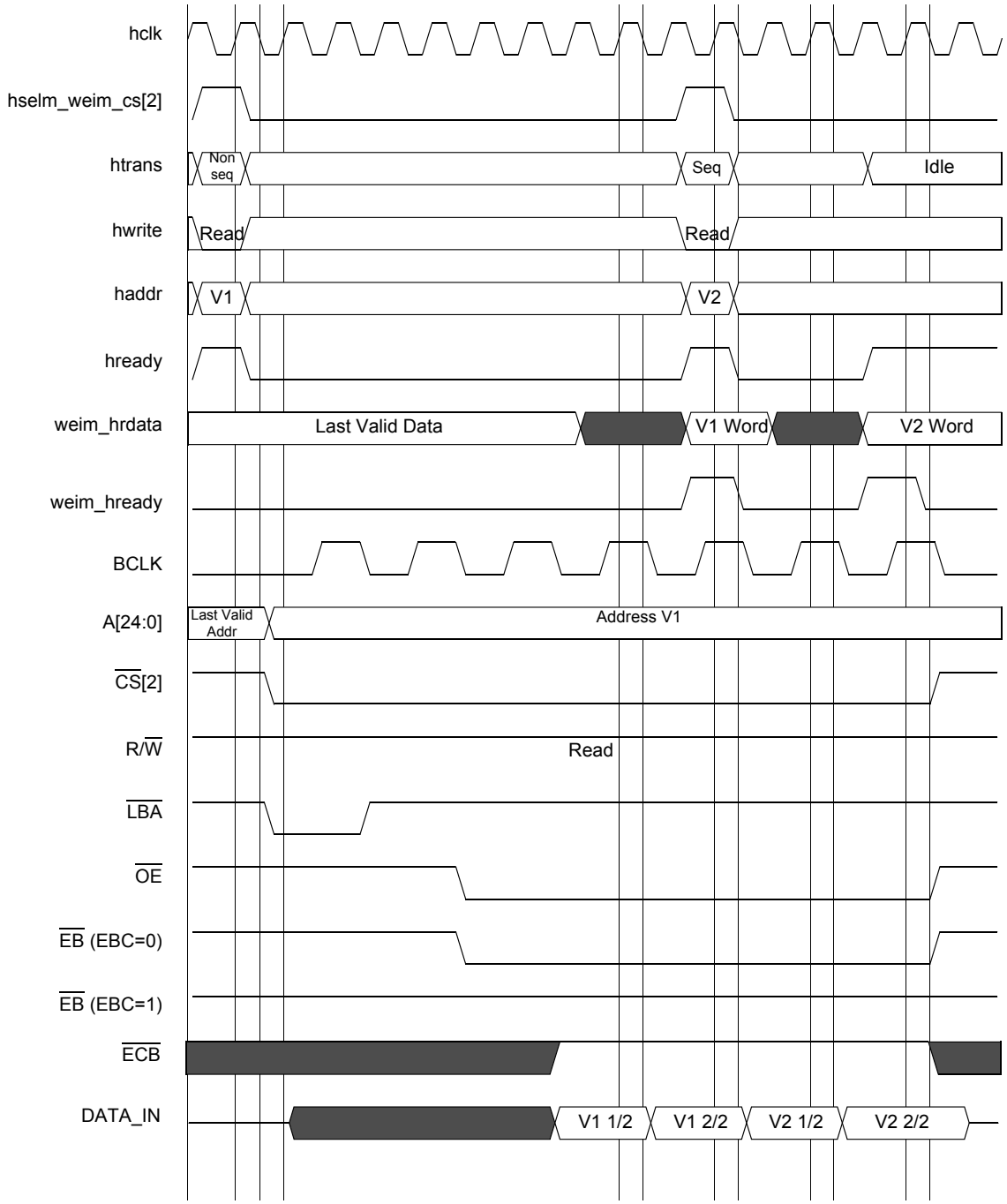


Figure 76. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

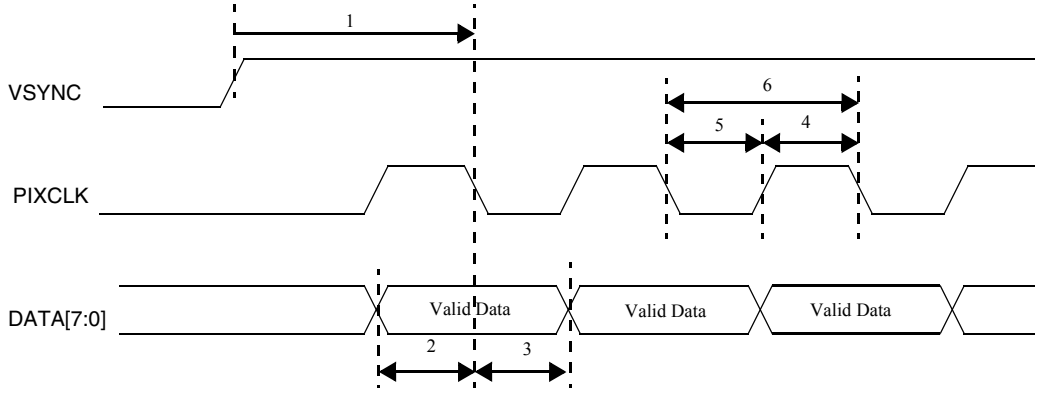


Figure 84. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 45. Non-Gated Clock Mode Parameters[1]

Number	Parameter	Minimum	Maximum	Unit
1	csi_vsync to csi_pixclk	9 * T_{HCLK}	–	ns
2	csi_d setup time	1	–	ns
3	csi_d hold time	1	–	ns
4	csi_pixclk high time	T_{HCLK}	–	ns
5	csi_pixclk low time	T_{HCLK}	–	ns
6	csi_pixclk frequency	0	HCLK / 2	MHz

1. HCLK = AHB System Clock, T_{HCLK} = Period of HCLK

3.22.3 Calculation of Pixel Clock Rise/Fall Time

The limitation on pixel clock rise time/fall time is not specified. It should be calculated from the hold time and setup time based on the following assumptions:

Rising-edge latch data

- max rise time allowed = (positive duty cycle - hold time)
- max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore:

- max rise time = (period / 2 - hold time)
- max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
≥ max rise time allowed = 5 - 1 = 4ns
negative duty cycle = 10 / 2 = 5ns
≥ max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

- max fall time allowed = (negative duty cycle - hold time)
- max rise time allowed = (positive duty cycle - setup time)

4 Pin Assignment and Package Information

Table 46. i.MX21 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	LD9	LD12	LD14	REV	HSYNC	OE_ ACD	SD2_D2	CSI_ D0	CSI_ PIXCLK	CSI_ VSYNC	USBH1_ FS	USBH1_ OE	USBG_ FS	TOUT	SAP_ TXDAT	SSI1_ CLK	SSI2_ RXDAT	SSI2_TXDAT	SSI3_ FS
B	LD7	LD5	LD11	LD16	PS	CON TRAST	SD2_D0	SD2_ CMD	CSI_ D4	CSI_D6	USB_ PWR	USBG_ SCL	USBG_ TXDM	SAP_ FS	SSI1_ FS	SSI2_ FS	SSI3_ TXDAT	I2C_DATA	CSPI2_ SS2
C	LD1	LD3	LD6	LD10	LD17	VSYNC	SD2_D3	CSI_ D1	CSI_ MCLK	CSI_ HSYNC	USB_ OC	USBH1_ RXDM	USBG_ RXDM	TIN	SSI1_ TXDAT	SSI3_ RXDAT	SSI3_ CLK	I2C_CLK	CSPI2_ SS1
D	LD2	LD0	LD13	CLS	QVDD	QVSS	SD2_D1	SD2_ CLK	CSI_ D2	CSI_D7	USBH1_ TXDM	USBH1_ RXDP	USBG_ ON	USBG_ RXDP	SAP_ RXDAT	SSI1_ RXDAT	SSI2_ CLK	CSPI2_SS0	CSPI2_ SCLK
E	LD8	LD4	LD15	SPL_ SPR												SAP_ CLK	CSPI2_ MISO	CSPI1_SS2	CSPI2_ MOSI
F	A24_ NFIO14	D31	A25_ NFIO15	LSCLK												CSPI1_ SS1	CSPI1_ MISO	KP_ROW0	CSPI1_ SS0
G	A22_ NFIO12	D29	A23_ NFIO13	D30			NVDD6	NVSS6	CSI_D3	USB_ BYP	USBH_ ON	USBG_ SDA	USBG_ TXDP			KP_ ROW1	KP_ ROW3	UART2_CTS	KP_ ROW4
H	A20	D27	A21_ NFIO11	D28			NVDD1	NVSS5	CSI_D5	CSPI1_ SCLK	CSPI1_ RDY	USBH1_ TXDP	USBG_ OE			TEST_ WB4	TEST_ WB2	TEST_WB3	PWMO
J	A19	A18	D25	D26			NVDD1	NVDD5	NVDD4	KP_ ROW5	KP_ ROW2	CSPI1_ MOSI	TEST_ WB0			UART2_ RTS	KP_COL1	KP_COL0	TEST_ WB1
K	A16	A17	D23	D24			NVSS1	NVSS4	QVDDX	UART1_ RXD	TDO	QVDD	QVSS			KP_ COL3	KP_COL5	KP_COL4	KP_ COL2
L	A14_ NFIO9	A15_ NFIO10	D21	D22			NVSS1	NVDD3	QVDD	QVSS	NFIO2	NFWP	UART1_ TXD			UART2_ TXD	UART3_ RTS	UART3_CTS	UART3_ TXD
M	D19	A13_ NFIO8	D20	D18			NVDD2	NVDD3	NVSS3	QVSS	NFIO7	NFRB	EXT_ 48M			UART2_ RXD	UART3_ RXD	UART1_RTS	UART1_ CTS
N	A11	A12	D17	D16			LBA	NVSS3	SDCKE0	NVSS1	NVSS1	NVDD1	NVDD1			SD1_ D0	TCK	SD1_D1	RTCK
P	A9	A10	D15	D14												SD1_ D2	SD1_ CMD	TDI	TMS
R	A7	A8	D13	D12												SD1_ CLK	EXT_ 266M	NVSS2	TRST
T	A5	A6	EB3	D10	CS3	CS1	BCLK	MA11	RAS	CAS	NFIO5	NFIO3	NFWE	RESET_ IN	NFCE	BOOT1	SD1_D3	CLKMODE1	CLK MODE0
U	D11	EB1	EB2	OE	CS4	D6	ECB	D3	MA10	PC_ PWRON	PF16	NFIO4	NFIO1	NFALE	NFCLE	POR	BOOT2	BOOT3	XTAL32K
V	A4	EB0	D9	D8	CS5	D5	CS0	RW	D1	JTAG_ CTRL	SDWE	CLKO	NFIO6	QVSS	RESET_ OUT	BOOT0	OSC26M_ TEST	VDDA	EXTAL 32K
W	A3	A2	D7	A1	CS2	A0	D4	D2	D0	SDCLK	SDCKE1	NFIO0	NFRE	QVDD	QVSS	EXTAL 26M	XTAL26M	QVDD	QVSS