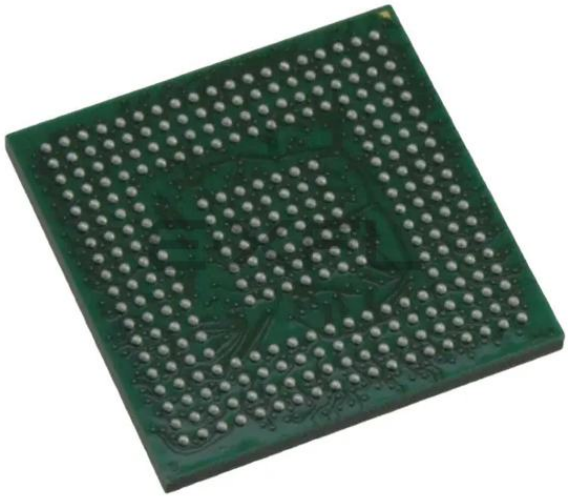

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	Yes
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	USB 1.x (2)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc94mx21dvkn3r2

For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

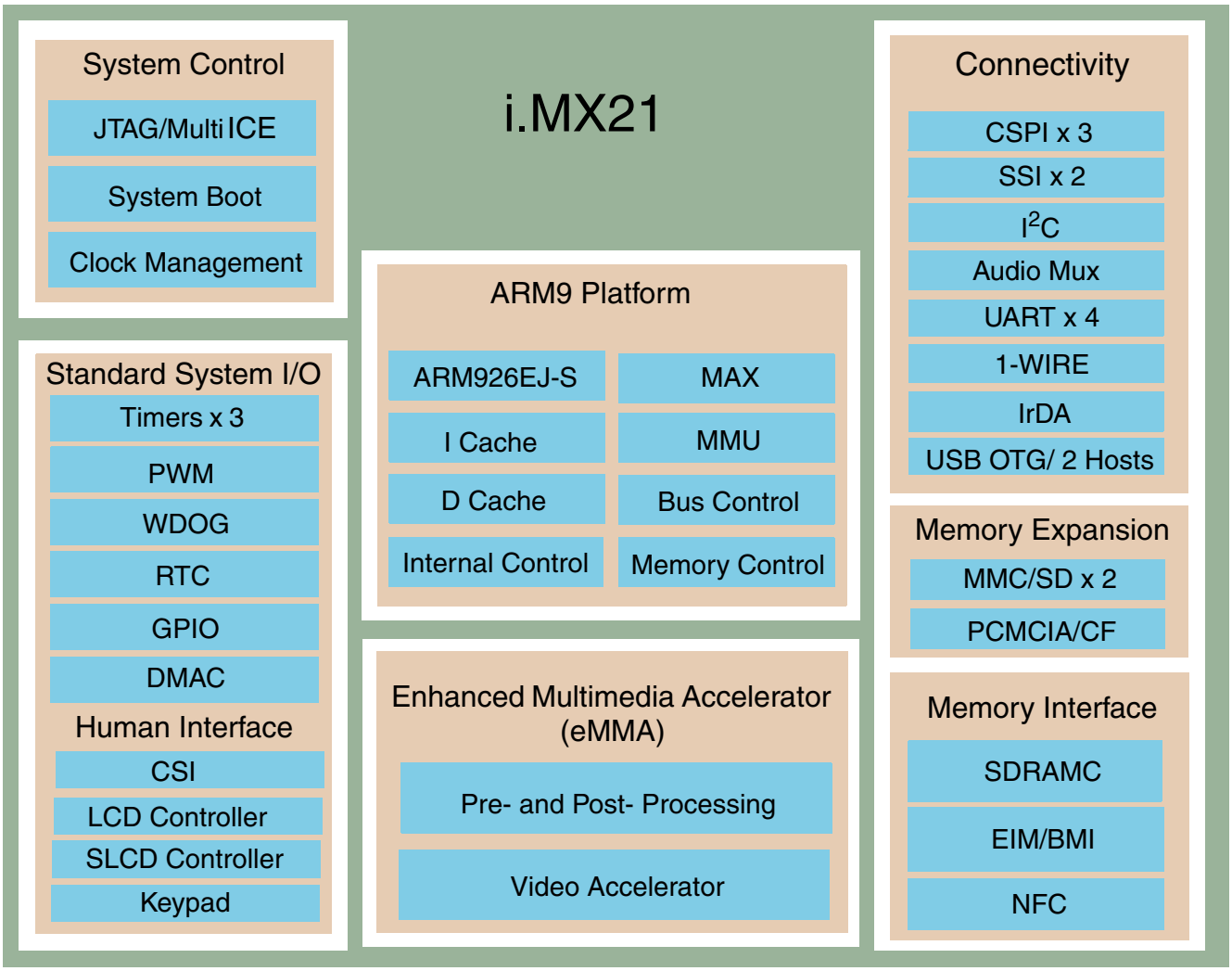


Figure 1. i.MX21 Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
TEST_WB[4:3]	These are special factory test signals. To ensure proper operation, leave these signals as no connects.
WKGD	Battery indicator input used to qualify the walk-up process. Also multiplexed with TIN.
JTAG For termination recommendations, see the Table "*JTAG pinouts*" in the *Multi-ICE® User Guide* from ARM® Limited.	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
TDO	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
JTAG_CTRL	JTAG Controller select signal—JTAG_CTRL is sampled during the rising edge of TRST. Must be pulled to logic high for proper JTAG interface to debugger. Pulling JTAG_CRTL low is for internal test purposes only.
RTCK	JTAG Return Clock used to enhance stability of JTAG debug interface devices. This signal is multiplexed with 1-Wire, therefore using 1-Wire renders RTCK unusable and vice versa.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [17:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off. LD[15:0] signals are multiplexed with SLCDC1_DAT[15:0] from SLCDC1 and BMI_D[15:0]. LD[17] signal is multiplexed with $\overline{\text{BMI\_WRITE}}$ of BMI. LD[16] is multiplexed with BMI_READ_REQ of BMI and $\overline{\text{EXT\_DMAGRANT}}$.
FLM_VSYNC (or simply referred to as VSYNC)	Frame Sync or Vsync—This signal also serves as the clock signal output for gate driver (dedicated signal SPS for Sharp panel HR-TFT). This signal is multiplexed with BMI_RXF_FULL and $\overline{\text{BMI\_WAIT}}$ of the BMI.
LP_HSYNC (or simply referred to as HSYNC)	Line Pulse or HSync
LSCLK	Shift Clock. This signal is multiplexed with the BMI_CLK_CS from BMI.
OE_ACD	Alternate Crystal Direction/Output Enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control. This signal is multiplexed with the $\overline{\text{BMI\_READ}}$ from BMI.
SPL_SPR	Sampling start signal for left and right scanning. This signal is multiplexed with the SLCDC1_CLK.
PS	Control signal output for source driver (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_CS.
CLS	Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_RS.
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal). This signal is multiplexed with SLCDC1_D0.

Table 2. i.MX21 Signal Descriptions (Continued)

Signal Name	Function/Notes
Smart LCD Controller	
SLCDC1_CLK	SLCDC Clock output signal. This signal is multiplexed and available at 2 alternate locations. These are SPL_SPR and SD2_CLK signals of LCDC and SD2, respectively.
SLCDC1_CS	SLCDC Chip Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are PS and SD2_CMD signals of LCDC and SD2, respectively.
SLCDC1_RS	SLCDC Register Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are CLS and SD2_D3 signals of LCDC and SD2, respectively.
SLCDC1_D0	SLCDC serial data output signal. This signal is multiplexed and available at 2 alternate signal locations. These are and REV and SD2_D2 signals of LCDC and SD2, respectively. This signal is inactive when a parallel data interface is used.
SLCDC1_DAT[15:0]	SLCDC Data output signals for connection to a parallel SLCD panel interface. These signals are multiplexed with LD[15:0] while an alternate 8-bit SLCD muxing is available on LD[15:8]. Further alternate muxing of these signals are available on some of the USB OTG and USBH1 signals.
SLCDC2_CLK	SLCDC Clock input signal for pass through to SLCD device. This signal is multiplexed with SSI3_CLK signal from SSI3.
SLCDC2_CS	SLCDC Chip Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_TXD signal from SSI3.
SLCDC2_RS	SLCDC Register Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_RXD signal from SSI3.
SLCDC2_D0	SLCD Data input signal for pass through to SLCD device. This signal is multiplexed with SSI3_FS signal from SSI3.
Bus Master Interface (BMI)	
BMI_D[15:0]	BMI bidirectional data bus. Bus width is programmable between 8-bit or 16-bit.These signals are multiplexed with LD[15:0] and SLCDC_DAT[15:0].
BMI_CLK_CS	BMI bidirectional clock or chip select signal.This signal is multiplexed with LSCLK of LCDC.
$\overline{\text{BMI\_WRITE}}$	BMI bidirectional signal to indicate read or write access. This is an input signal when the BMI is a slave and an output signal when BMI is the master of the interface. $\overline{\text{BMI\_WRITE}}$ is asserted for write and negated for read.This signal is muxed with LD[17] of LCDC.
$\overline{\text{BMI\_READ}}$	BMI output signal to enable data read from external slave device. This signal is not used and driven high when BMI is slave.This signal is multiplexed with CONTRAST signal of LCDC.
BMI_READ_REQ	BMI Read request output signal to external bus master. This signal is active when the data in the TXFIFO is larger or equal to the data transfer size of a single external BMI access.This signal is muxed with LD[16] of LCDC.
BMI_RXF_FULL	BMI Receive FIFO full active high output signal to reflect if the RxFIFO reaches water mark value.This signal is muxed with VSYNC of the LCDC.
$\overline{\text{BMI\_WAIT}}$	BMI Wait—Active low signal to wait for data ready (read cycle) or accepted (write_cycle). Also multiplexed with VSYNC.
External DMA	
$\overline{\text{EXT\_DMAREQ}}$	External DMA Request input signal. This signal is multiplexed with CSPI1_$\overline{\text{RDY}}$.
$\overline{\text{EXT\_DMAGRANT}}$	External DMA Grant output signal. This signal is multiplexed with LD[16] of LCDC and CSPI1_SS1 of CSPI1.

Table 11. Reset Module Timing Parameters

Ref No.	Parameter	1.8V ± 0.10V		3.0V ± 0.30V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	800	–	800	–	ms
2	Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7k to 32k-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14k to 32k-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET\_IN}}$	4	–	4	–	Cycles of CLK32
6	4k to 32k-cycle qualifier	4	4	4	4	Cycles of CLK32

3.7 External DMA Request and Grant

The External DMA request is an active low signal to be used by devices external to i.MX21 processor to request the DMAC for data transfer.

After assertion of External DMA request the DMA burst will start when the channel on which the External request is the source (as per the RSSR settings) becomes the current highest priority channel. The external device using the External DMA request should keep its request asserted until it is serviced by the DMAC. One External DMA request will initiate one DMA burst.

The output External Grant signal from the DMAC is an active-low signal.When the following conditions are true, the External DMA Grant signal is asserted with the initiation of the DMA burst.

- The DMA channel for which the DMA burst is ongoing has request source as external DMA Request (as per source select register setting).
- REN and CEN bit of this channel are set.
- External DMA Request is asserted.

After the grant is asserted, the External DMA request will not be sampled until completion of the DMA burst. As the external request is synchronized, the request synchronization will not be done during this period. The priority of the external request becomes low for the next consecutive burst, if another DMA request signal is asserted.

Worst case—that is, the smallest burst (1 byte read/write) timing diagrams are shown in Figure 4 and Figure 5. Minimum and maximum timings for the External request and External grant signals are present in Table 12.

Figure 4 shows the minimum time for which the External Grant signal remains asserted when an External DMA request is de-asserted immediately after sensing grant signal active.

can write data to BMI RxFIFO anytime as CPU or DMA can move data out from RxFIFO much faster than the BMI interface. Overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

3.8.1.1.1 MMD Read BMI Timing

Figure 6 shows the MMD read BMI timing when the MMD drives clock.

On each rising edge of BMI_CLK/CS BMI checks the $\overline{\text{BMI\_WRITE}}$ logic level to determine if the current cycle is a read cycle. It puts data into the data bus and enables the data out on the rising edge of BMI_CLK/CS if BMI_WRITE is logic high. The BMI_READ_REQ is negated one hclk cycle after the BMI_CLK/CS rising edge of last data read. The MMD cannot issues read command when BMI_READ_REQ is low (no data in TxFIFO).

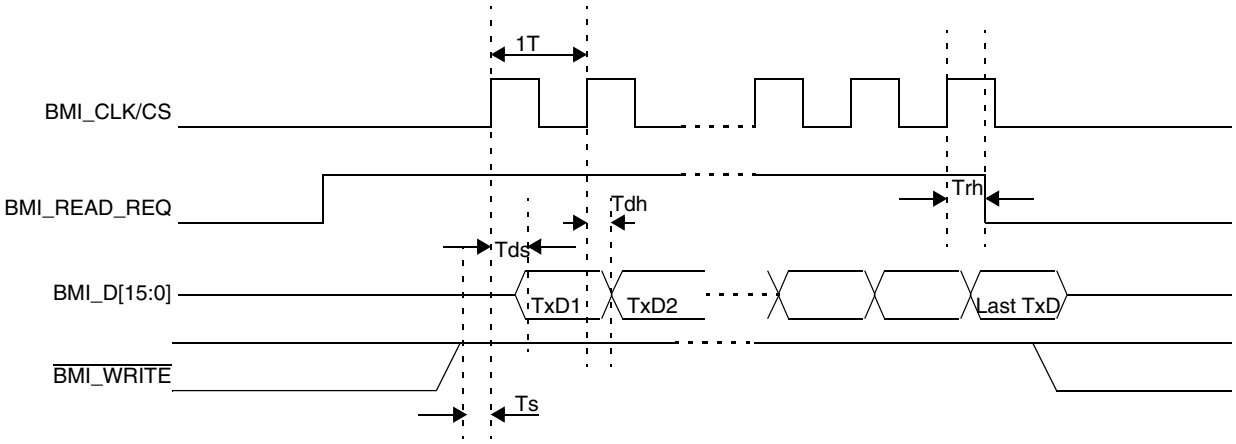


Figure 6. MMD (ATI) Drives Clock, MMD Read BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0,MMD_CLKOUT=0)

Table 13. MMD Read BMI Timing Table when MMD Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Clock period	1T	33.3	–	–	ns
$\overline{\text{write}}$ setup time	Ts	11	–	–	ns
read_req hold time	Trh	6	–	24	ns
transfer data setup time	Tds	6	–	14	ns
transfer data hold time	Tdh	6	-	14	ns

Note: All the timings assume that the hclk is running at 133 MHz.

Note: The MIN period of the 1T is assumed that MMD latch data at falling edge.

Note: If the MMD latch data at next rising edge, the ideally max clock can be as much as double, but because the BMI data pads are slow pads and it max frequency can only up to 18MHz, the max clock frequency can only up to 36 MHz.

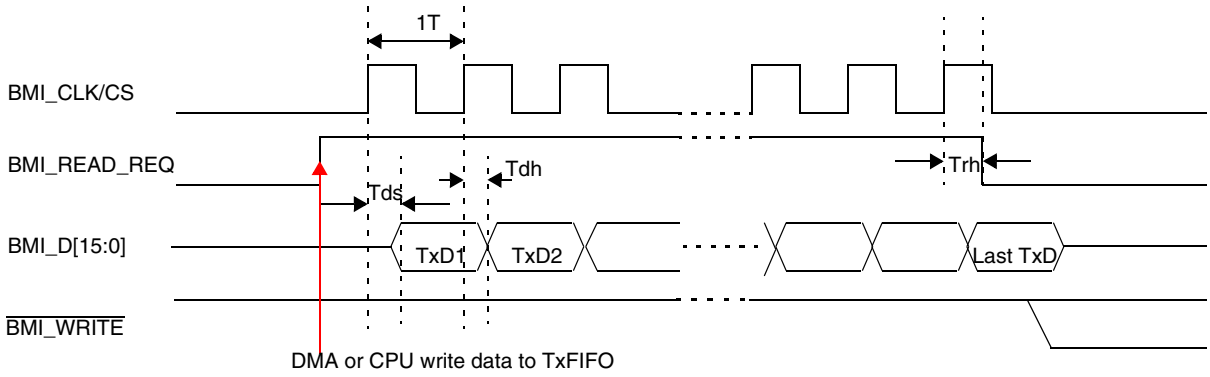


Figure 8. BMI Drives Clock, MMD Read BMI Timing (MASTER_MODE_SEL=0, MMD_MODE_SEL=1, MMD_CLKOUT=1)

Table 15. MMD Read BMI Timing Table when BMI Drives Clock

Item	Symbol	Minimum	Typical	Maximum	Unit
Transfer data setup time	Tds	2	–	8	ns
Transfer data hold time	Tdh	2	–	8	ns
Read_req hold time	Trh	2	–	18	ns

Note: In this mode, the max frequency of the BMI_CLK/CS can be up to 36MHz (double as max data pad speed).
Note: The BMI_CLK/CS can only be divided by 2,4,8,16 from HCLK.

3.8.1.4 MMD Write BMI Timing

Figure 9 shows the MMD write BMI timing when BMI drives BMI_CLK/CS.

When the $\overline{\text{BMI\_WRITE}}$ signal is asserted, the BMI can write a 1 to READ bit of control register to issue a WRITE cycle. This bit is cleared automatically when the WRITE operation is completed. In a WRITE burst the MMD will write COUNT+1 data to the BMI. The user can issue another WRITE operation if the MMD still has data to write after the first operation completed.

The BMI can latch the data either at falling edge or the next rising edge of the BMI_CLK/CS according to the DATA_LATCH bit. When the DATA_LATCH bit is set, the BMI latch data at the next rising edge and latch the last data using the internal clock.

$\overline{\text{BMI\_WRITE}}$ signal can not be negated when the WRITE operation is proceeding.

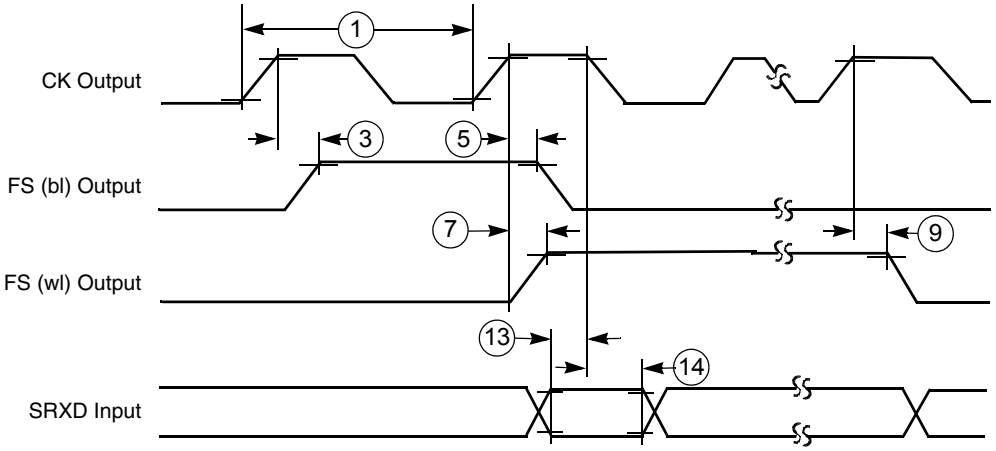
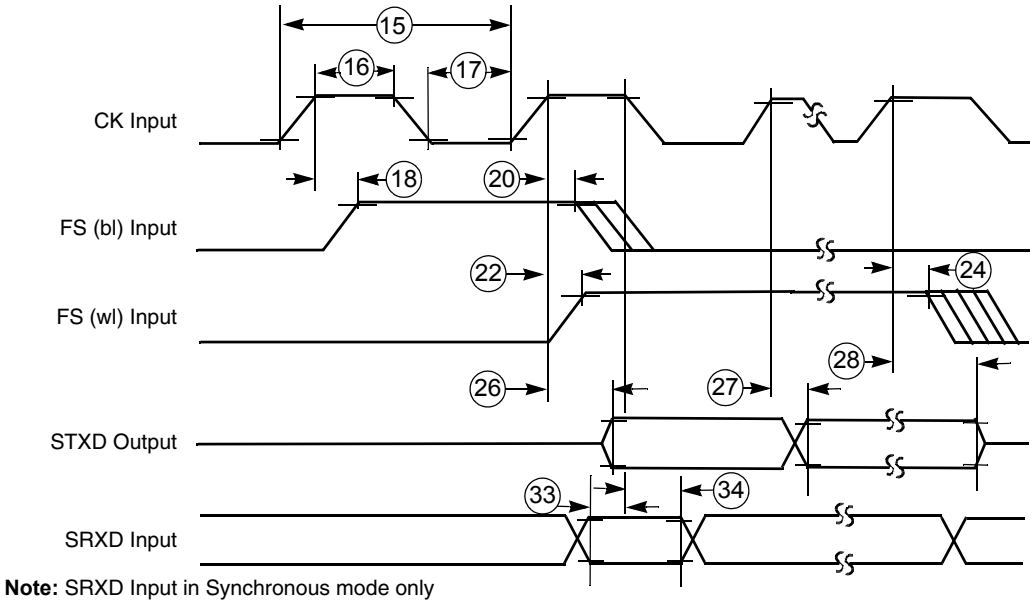


Figure 43. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 44. SSI Transmitter External Clock Timing Diagram

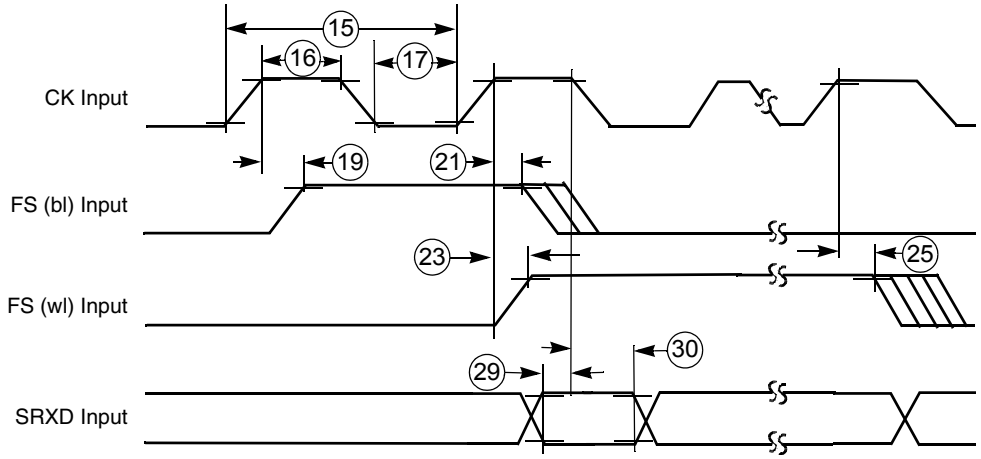


Figure 45. SSI Receiver External Clock Timing Diagram

Table 34. SSI to SSI1 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
20	(Tx) CK high to FS (bl) low	10.22	17.63	8.82	16.24	ns
21	(Rx) CK high to FS (bl) low	10.79	19.67	9.39	18.28	ns
22	(Tx) CK high to FS (wl) high	10.22	17.63	8.82	16.24	ns
23	(Rx) CK high to FS (wl) high	10.79	19.67	9.39	18.28	ns
24	(Tx) CK high to FS (wl) low	10.22	17.63	8.82	16.24	ns
25	(Rx) CK high to FS (wl) low	10.79	19.67	9.39	18.28	ns
26	(Tx) CK high to STXD valid from high impedance	10.05	15.75	8.66	14.36	ns
27a	(Tx) CK high to STXD high	10.00	15.63	8.61	14.24	ns
27b	(Tx) CK high to STXD low	10.00	15.63	8.61	14.24	ns
28	(Tx) CK high to STXD high impedance	10.05	15.75	8.66	14.36	ns
29	SRXD setup time before (Rx) CK low	0.78	–	0.47	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI1 Ports)						
31	SRXD setup before (Tx) CK falling	19.90	–	19.90	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI1 Ports)						
33	SRXD setup before (Tx) CK falling	2.59	–	2.28	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

Table 35. SSI to SSI2 Ports Timing Parameters

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (SSI2 Ports)						
1	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
2	(Tx) CK high to FS (bl) high	0.01	0.15	0.01	0.15	ns
3	(Rx) CK high to FS (bl) high	-0.21	0.05	-0.21	0.05	ns
4	(Tx) CK high to FS (bl) low	0.01	0.15	0.01	0.15	ns
5	(Rx) CK high to FS (bl) low	-0.21	0.05	-0.21	0.05	ns
6	(Tx) CK high to FS (wl) high	0.01	0.15	0.01	0.15	ns
7	(Rx) CK high to FS (wl) high	-0.21	0.05	-0.21	0.05	ns
8	(Tx) CK high to FS (wl) low	0.01	0.15	0.01	0.15	ns
9	(Rx) CK high to FS (wl) low	-0.21	0.05	-0.21	0.05	ns
10	(Tx) CK high to STXD valid from high impedance	0.34	0.72	0.34	0.72	ns

Table 35. SSI to SSI2 Ports Timing Parameters (Continued)

Ref No.	Parameter	1.8 V ± 0.1 V		3.0 V ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
11a	(Tx) CK high to STXD high	0.34	0.72	0.34	0.72	ns
11b	(Tx) CK high to STXD low	0.34	0.72	0.34	0.72	ns
12	(Tx) CK high to STXD high impedance	0.34	0.48	0.34	0.48	ns
13	SRXD setup time before (Rx) CK low	21.50	–	21.50	–	ns
14	SRXD hold time after (Rx) CK low	0	–	0	–	ns
External Clock Operation (SSI2 Ports)						
15	(Tx/Rx) CK clock period[1]	90.91	–	90.91	–	ns
16	(Tx/Rx) CK clock high period	36.36	–	36.36	–	ns
17	(Tx/Rx) CK clock low period	36.36	–	36.36	–	ns
18	(Tx) CK high to FS (bl) high	10.40	17.37	8.67	15.88	ns
19	(Rx) CK high to FS (bl) high	11.00	19.70	9.28	18.21	ns
20	(Tx) CK high to FS (bl) low	10.40	17.37	8.67	15.88	ns
21	(Rx) CK high to FS (bl) low	11.00	19.70	9.28	18.21	ns
22	(Tx) CK high to FS (wl) high	10.40	17.37	8.67	15.88	ns
23	(Rx) CK high to FS (wl) high	11.00	19.70	9.28	18.21	ns
24	(Tx) CK high to FS (wl) low	10.40	17.37	8.67	15.88	ns
25	(Rx) CK high to FS (wl) low	11.00	19.70	9.28	18.21	ns
26	(Tx) CK high to STXD valid from high impedance	9.59	17.08	7.86	15.59	ns
27a	(Tx) CK high to STXD high	9.59	17.08	7.86	15.59	ns
27b	(Tx) CK high to STXD low	9.59	17.08	7.86	15.59	ns
28	(Tx) CK high to STXD high impedance	9.59	16.84	7.86	15.35	ns
29	SRXD setup time before (Rx) CK low	2.52	–	2.52	–	ns
30	SRXD hole time after (Rx) CK low	0	–	0	–	ns
Synchronous Internal Clock Operation (SSI2 Ports)						
31	SRXD setup before (Tx) CK falling	20.78	–	20.78	–	ns
32	SRXD hold after (Tx) CK falling	0	–	0	–	ns
Synchronous External Clock Operation (SSI2 Ports)						
33	SRXD setup before (Tx) CK falling	4.42	–	4.42	–	ns
34	SRXD hold after (Tx) CK falling	0	–	0	–	ns

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

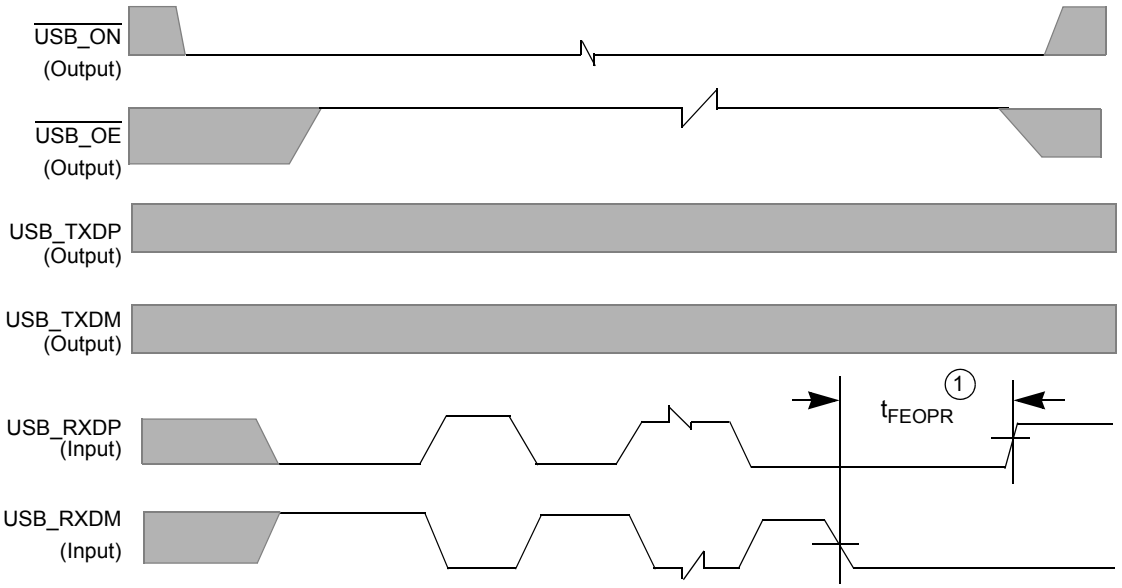


Figure 51. USB Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 40. USB Timing Parameters for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 V ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{FEOPR}; Receiver SE0 interval of EOP	82	–	ns

The USBOTG I^{2}C communication protocol consists of six components: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

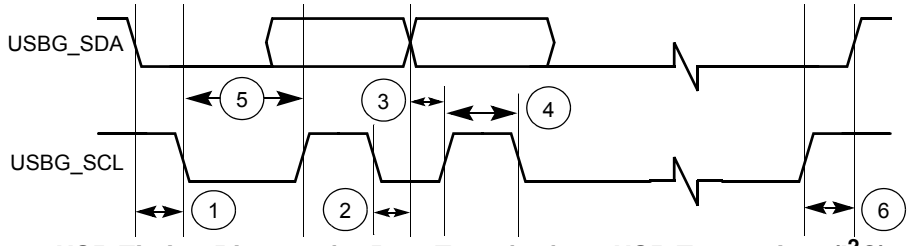


Figure 52. USB Timing Diagram for Data Transfer from USB Transceiver (I^{2}C)

Table 41. USB Timing Parameters for Data Transfer from USB Transceiver (I^{2}C)

Ref No.	Parameter	1.8 V ± 0.1 V		Unit
		Minimum	Maximum	
1	Hold time (repeated) START condition	188	–	ns
2	Data hold time	0	188	ns
3	Data setup time	88	–	ns
4	HIGH period of the SCL clock	500	–	ns
5	LOW period of the SCL clock	500	–	ns
6	Setup time for STOP condition	185	–	ns

Note: Signals listed with lower case letters are internal to the device.

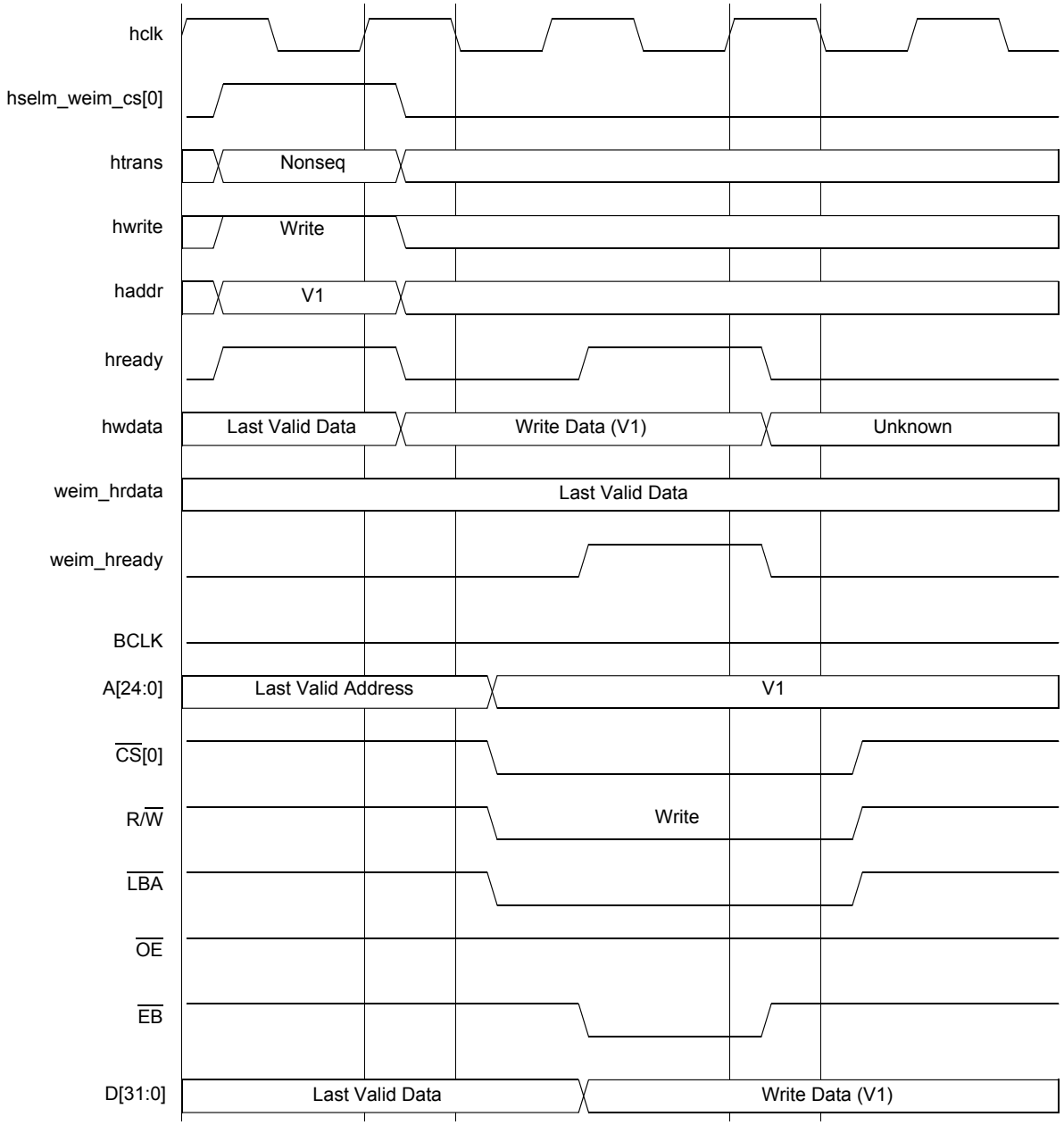


Figure 55. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

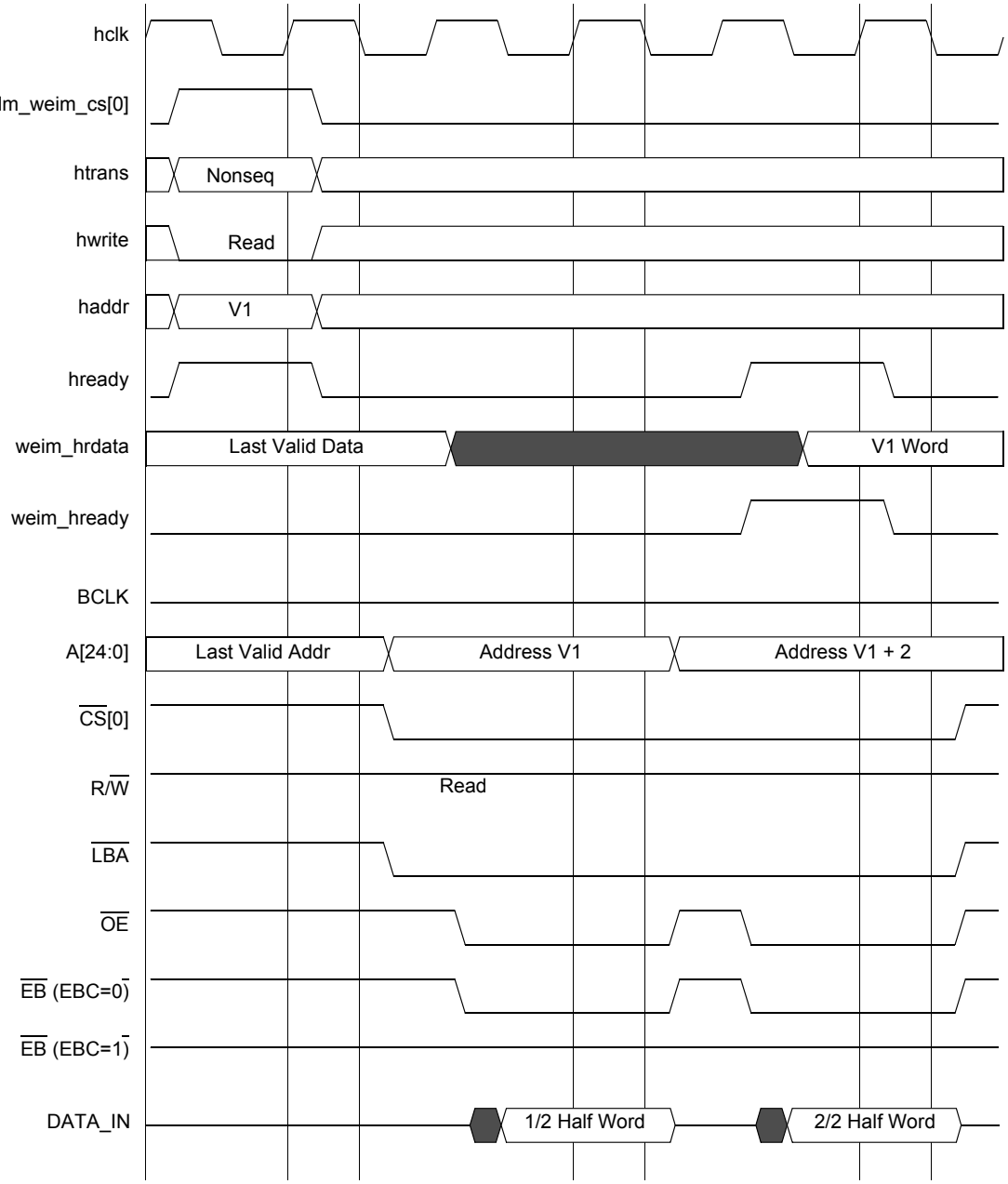


Figure 56. WSC = 1, OEA = 1, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

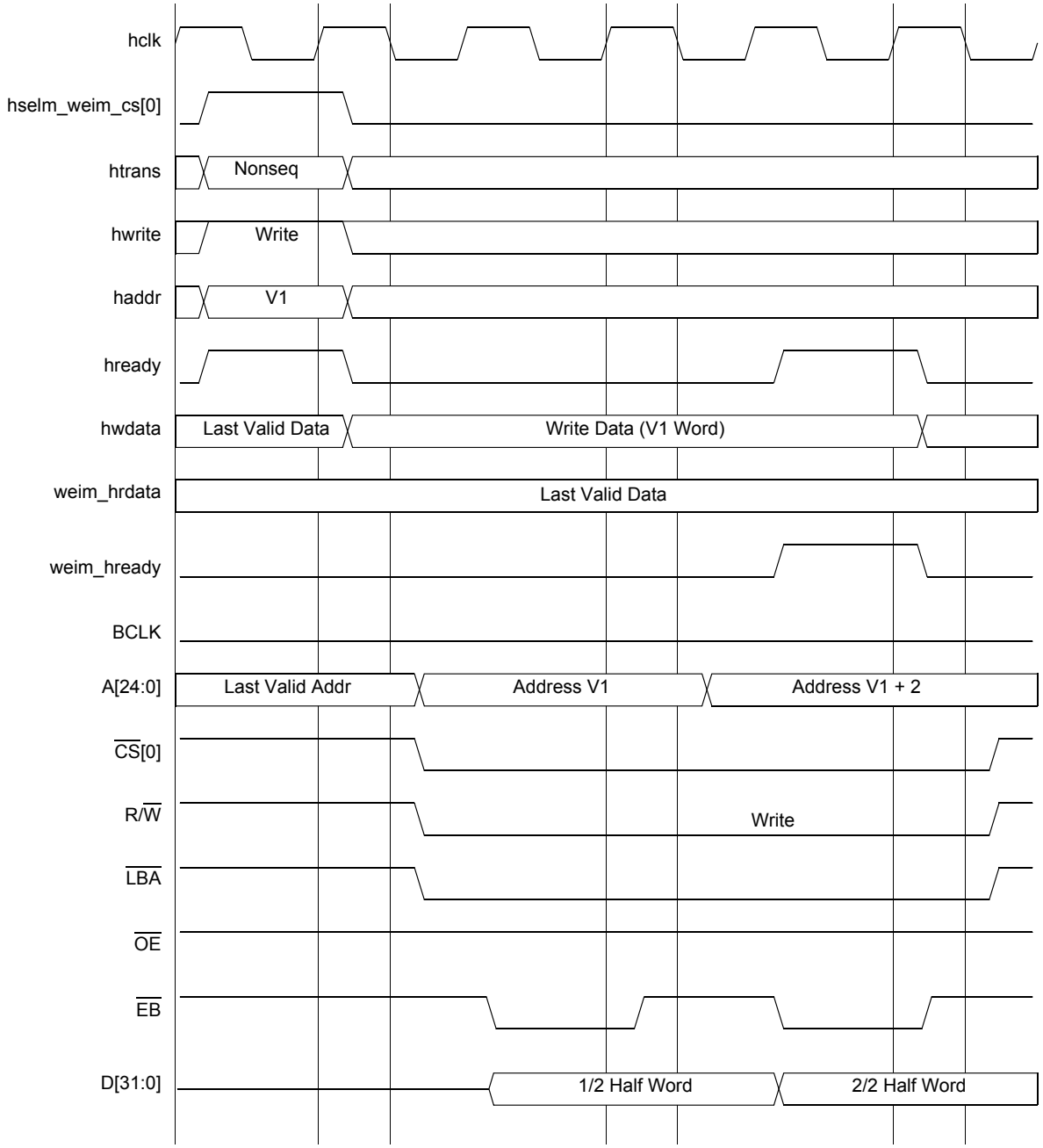


Figure 57. WSC = 1, WEA = 1, WEN = 1, A.WORD/E.HALF

Note: Signals listed with lower case letters are internal to the device.

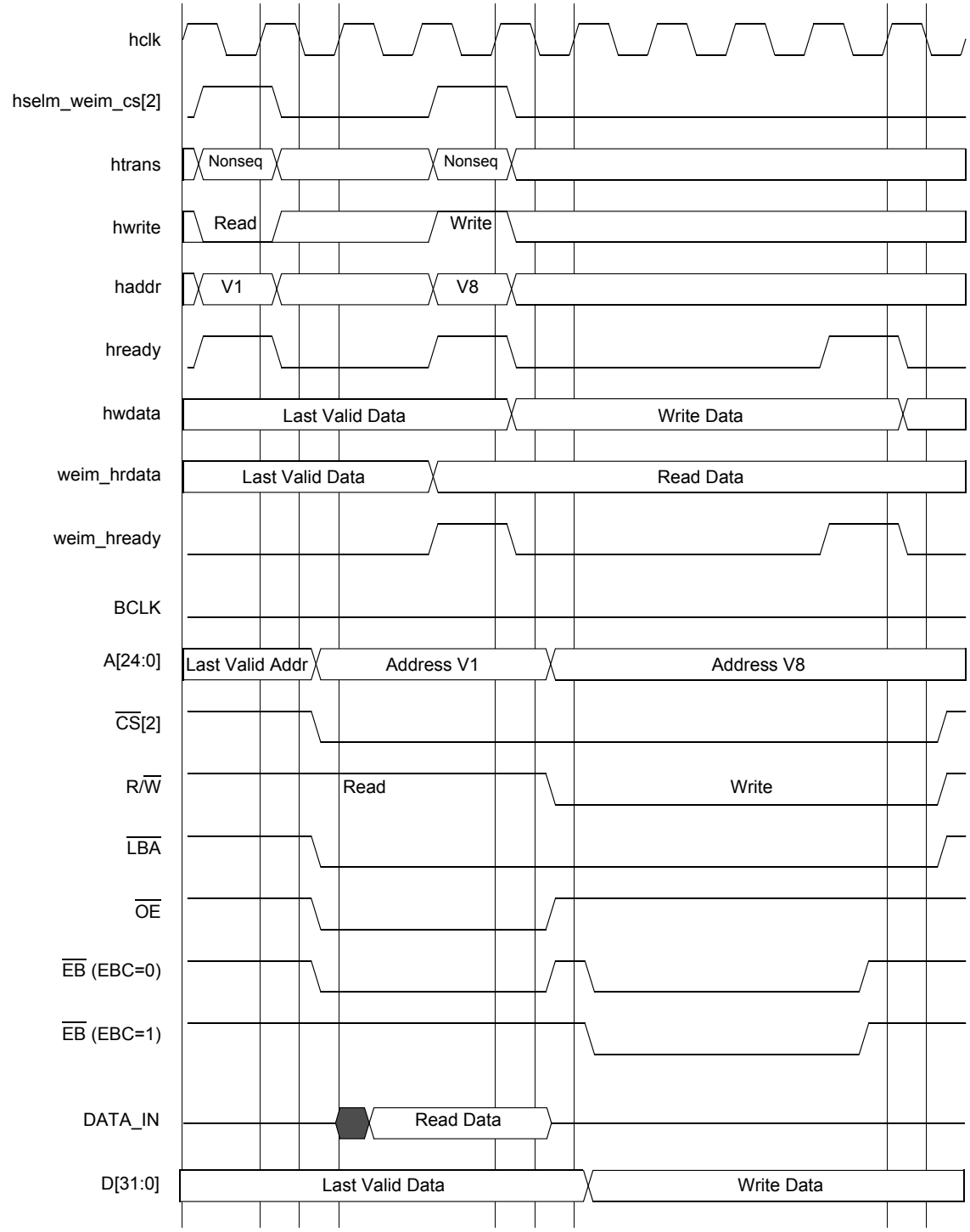


Figure 66. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

Note: Signals listed with lower case letters are internal to the device.

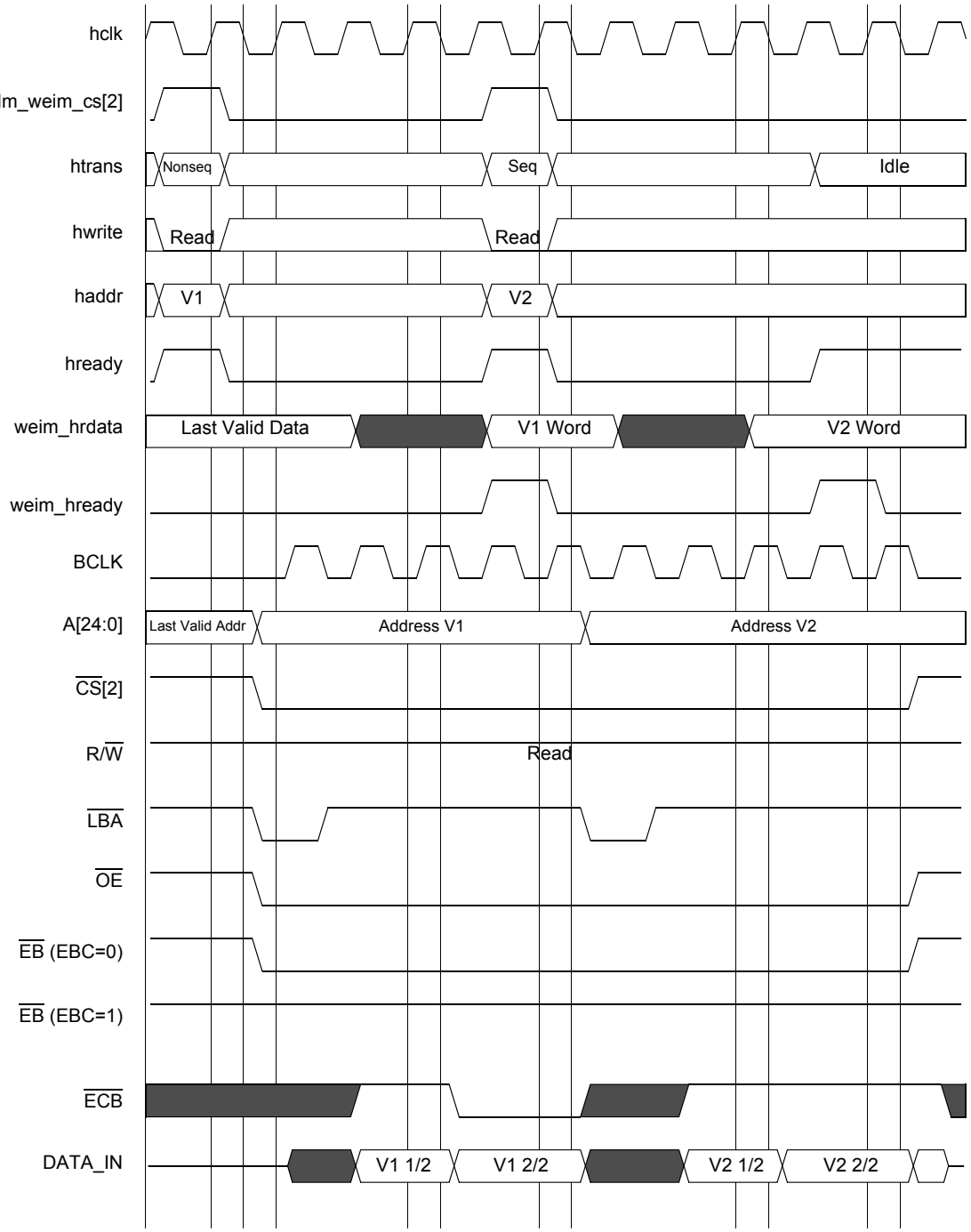


Figure 74. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

3.20 DTACK Mode Memory Access Timing Diagrams

When enabled, the DTACK input signal is used to externally terminate a data transfer. For DTACK enabled operations, a bus time-out monitor generates a bus error when an external bus cycle is not terminated by the DTACK input signal after 1024 HCLK clock cycles have elapsed, where HCLK is the internal system clock driven from the PLL module. For a 133 MHz HCLK setting, this time equates to 7.7 µs. Refer to the Section 3.5, "DPLL Timing Specifications" for more information on how to generate different HCLK frequencies.

There are two modes of operation for the DTACK input signal: rising edge detection or level sensitive detection with a programmable insensitivity time. DTACK is only used during external asynchronous data transfers, thus the SYNC bit in the chip select control registers must be cleared.

During edge detection mode, the EIM will terminate an external data transfer following the detection of the DTACK signal's rising edge, so long as it occurs within the 1024 HCLK cycle time. Edge detection mode is used for devices that follow the PCMCIA standard. Note that DTACK rising edge detection mode can only be used for $\overline{CS}$[5] operations. To configure $\overline{CS}$[5] for DTACK rising edge detection, the following bits must be programmed in the Chip Select 5 Control Register and EIM Configuration Register:

- WSC bit field set to 0x3F and CSA (or CSN) set to 1 or greater in the Chip Select 5 Control Register
- AGE bit set in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device. The requirement of setting CSA or CSN is required to allow the EIM to wait for the rising edge of DTACK during back-to-back external transfers, such as during DMA transfers or an internal 32-bit access through an external 16-bit data port.

During level sensitive detection, the EIM will first hold off sampling the DTACK signal for at least 2 HCLK cycles, and up to 5 HCLK cycles as programmed by the DCT bits in the Chip Select Control Register. After this insensitivity time, the EIM will sample DTACK and if it detects that DTACK is logic high, it will continue the data transfer at the programmed number of wait states. However, if the EIM detects that DTACK is logic low, it will wait until DTACK goes to logic high to continue the access, so long as this occurs within the 1024 HCLK cycle time. If at anytime during an external data transfer DTACK goes to logic low, the EIM will wait until DTACK returns to logic high to resume the data transfer. Level detection is often used for asynchronous devices such graphic controller chips. Level detection may be used with any chip select except CS[4] as it is multiplexed with the DTACK signal. To configure a chip select for DTACK level sensitive detection, the following bits must be programmed in the Chip Select Control Register and EIM Configuration Register:

- EW bit set, WSC set to > 1, and CSN set to < 3 in the Chip Select Control Register
- BCD/DCT set to desired "insensitivity time" in the Chip Select Control Register. The "insensitivity time" is dictated by the external device's timing requirements.
- AGE bit cleared in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device.

The waveforms in the following section provide examples of the DTACK signal operation.

3.20.1 DTACK Example Waveforms: Internal ARM AHB Word Accesses to Word-Width (32-bit) Memory

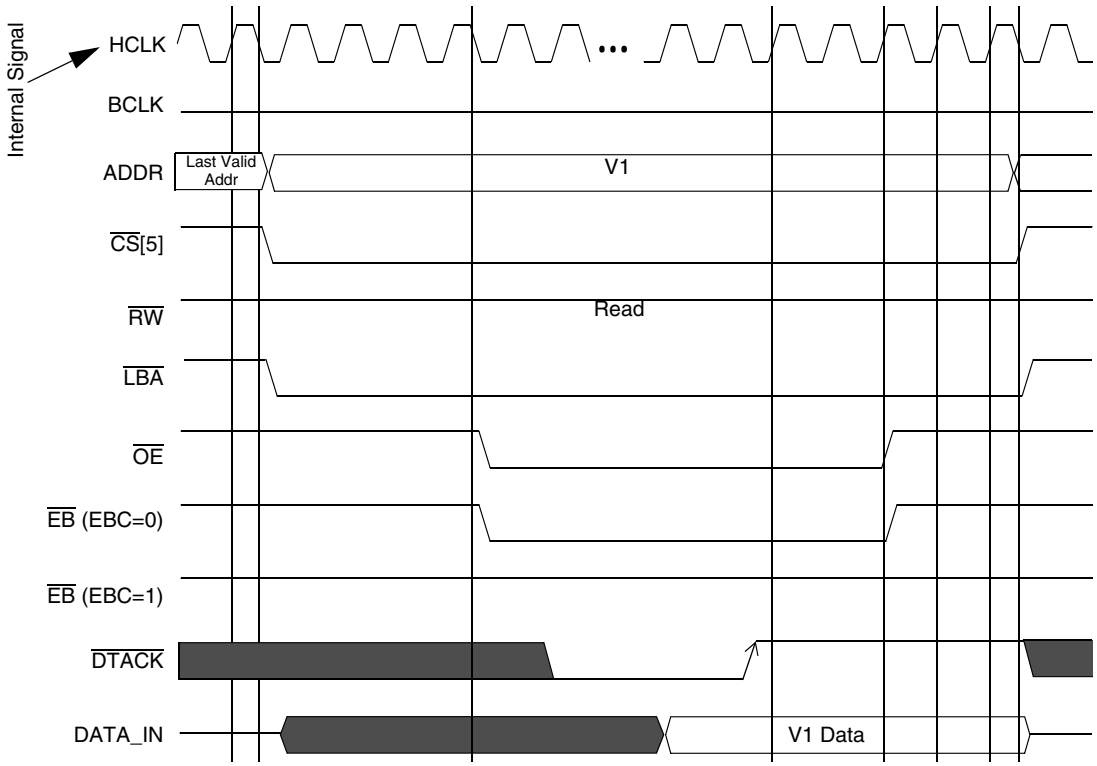


Figure 77. DTACK Edge Triggered Read Access, WSC=3F, OEA=8, OEN=5, AGE=1.

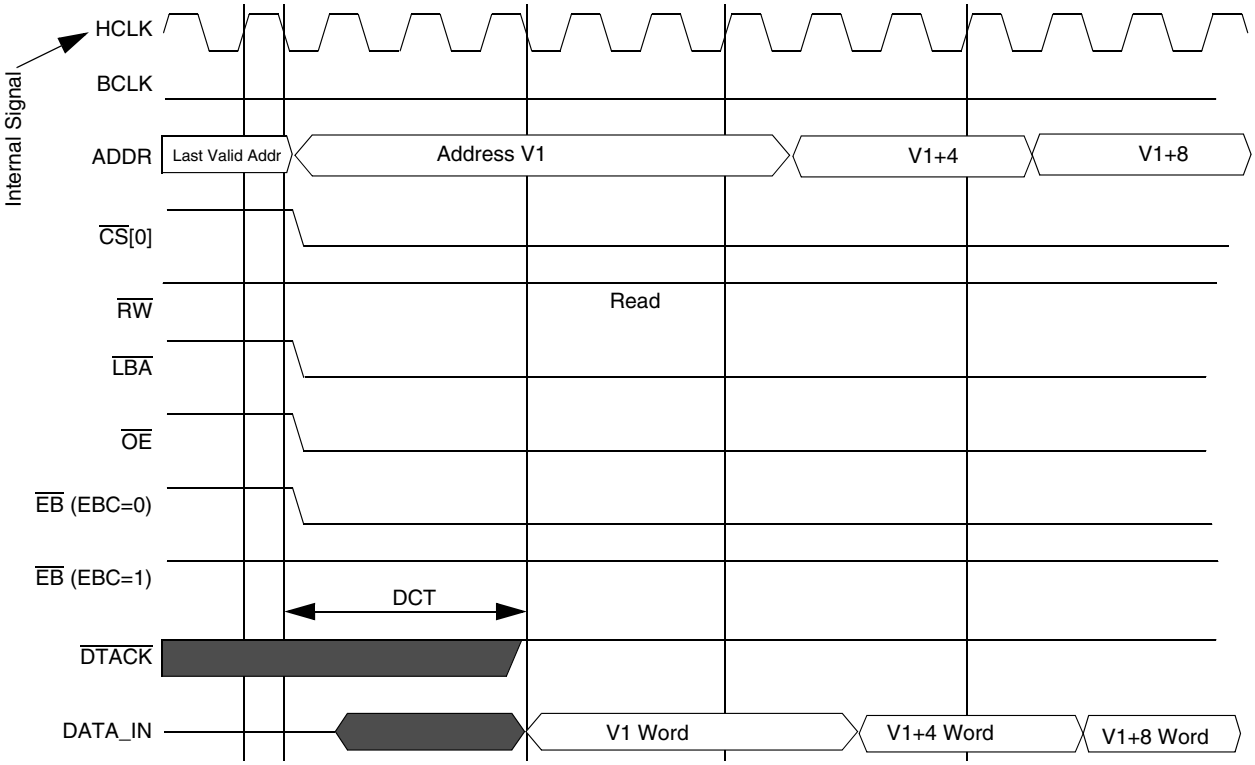


Figure 78. DTACK Level Sensitive Sequential Read Accesses, WSC=2, EW=1, DCT=1, AGE=0 (Example of DTACK Remaining High)

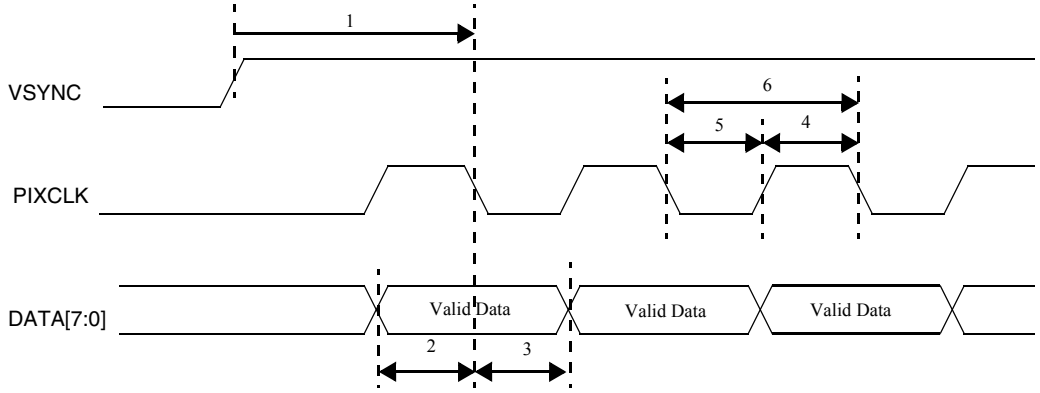


Figure 84. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge

Table 45. Non-Gated Clock Mode Parameters[1]

Number	Parameter	Minimum	Maximum	Unit
1	csi_vsync to csi_pixclk	9 * T_{HCLK}	–	ns
2	csi_d setup time	1	–	ns
3	csi_d hold time	1	–	ns
4	csi_pixclk high time	T_{HCLK}	–	ns
5	csi_pixclk low time	T_{HCLK}	–	ns
6	csi_pixclk frequency	0	HCLK / 2	MHz

1. HCLK = AHB System Clock, T_{HCLK} = Period of HCLK

3.22.3 Calculation of Pixel Clock Rise/Fall Time

The limitation on pixel clock rise time/fall time is not specified. It should be calculated from the hold time and setup time based on the following assumptions:

Rising-edge latch data

- max rise time allowed = (positive duty cycle - hold time)
- max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore:

- max rise time = (period / 2 - hold time)
- max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

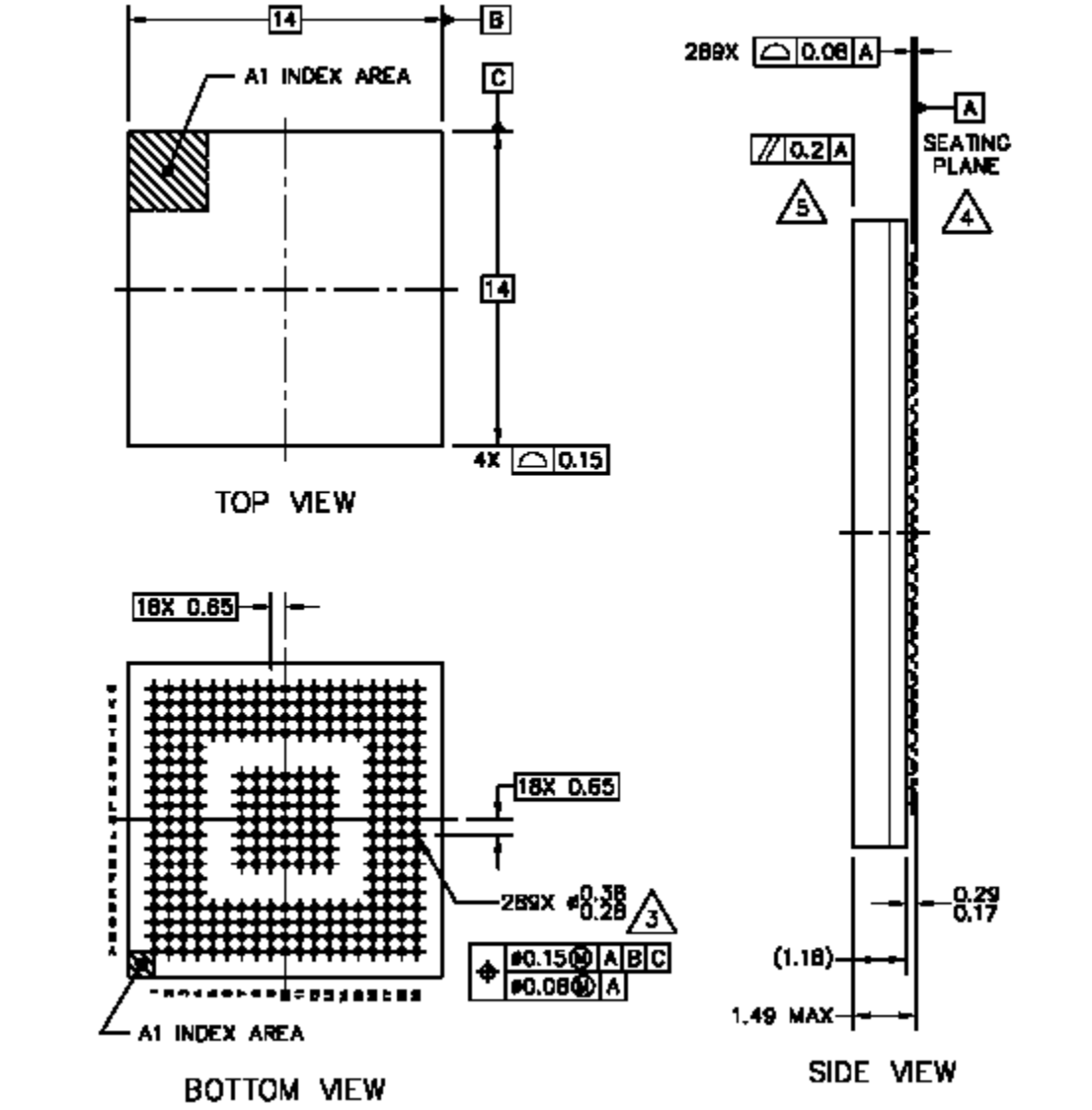
positive duty cycle = 10 / 2 = 5ns
≥ max rise time allowed = 5 - 1 = 4ns
negative duty cycle = 10 / 2 = 5ns
≥ max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

- max fall time allowed = (negative duty cycle - hold time)
- max rise time allowed = (positive duty cycle - setup time)

4.1 MAPBGA Package Dimensions

Figure 85 illustrates the MAPBGA 14 mm × 14 mm × 1.41 mm package, which has 0.65 mm ball pitch.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 85. i.MX21 MAPBGA Mechanical Drawing