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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Dual-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5743rk1mlq5

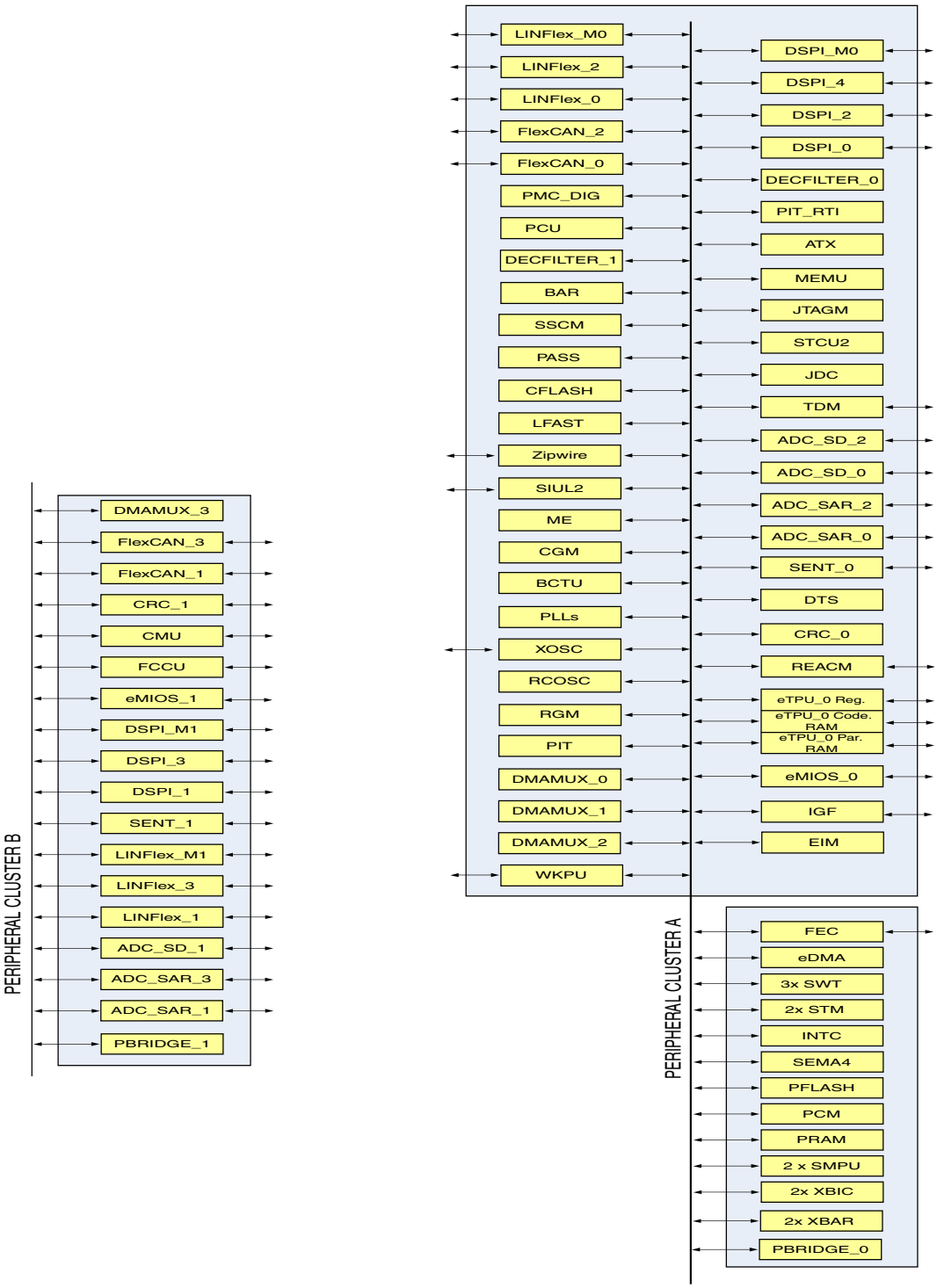

Figure 2. Peripherals allocation

2 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

Table 1. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
I_{INJA}	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXSEG}[10, 11]	Maximum current per I/O segment	—	–120	120	mA
T_{STG}	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	yrs
T_{SDR}	Maximum solder temperature[12] Pb-free package	—	—	260	°C
MSL	Moisture sensitivity level[13]	—	—	3	—

1. Voltage is referenced to V_{SS} unless otherwise noted.
2. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in note -1 and note -1.
3. Allowed 1.375 – 1.45 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in note -1.
4. 1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J = 150 °C.
5. Allowed 5.5 – 6.0 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time at or below 5.0 V +10%.
6. Allowed 3.6 – 4.5 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time at or below 3.3 V +10%. This is an internally regulated supply. Values given are for reference only.
7. The maximum input voltage on an I/O pin tracks with the associated I/P supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
8. Relative value can be exceeded, if design measures are taken to ensure injection current limitation (parameters I_{INJD} and I_{INJA}).
9. $V_{DD\_HV\_IO}$/$V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FEC}$, $V_{DD\_HV\_IO\_MSC}$.
10. Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
11. The average current values given in the "I/O pad current specifications" section should be used to calculate total I/O segment current.
12. Solder profile per IPC/JEDEC J-STD-020D.
13. Moisture sensitivity per JEDEC test method A112.

4 Electromagnetic Compatibility (EMC)

EMC measurements to IC-level IEC standards are available from Freescale on request.

5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 15. XOSC External Oscillator electrical specifications (continued)

Symbol	Parameter	Conditions		Value		Unit
				Min	Max	
			f_{XTAL} ≤ 40 MHz	12	43	
V_{EXTAL}	Oscillation Amplitude on the EXTAL pin after startup[7]	T_J = –40 °C to 150 °C		0.5	1.6	V
I_{XTAL}	XTAL current[7,8]	T_J = –40 °C to 150 °C		—	14	mA

1. The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40MHZ.
2. This value is determined by the crystal manufacturer and board design.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
5. This parameter is guaranteed by design rather than 100% tested.
6. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance. The capacitance on “EXTAL” and “XTAL” by internal capacitance array is controlled by the XOSC LOAD CAP SEL field of the UTEST Miscellaneous DCF client. See the DCF Records chapter of the Reference Manual.
7. Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid overdriving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
8. IXTAL is the oscillator bias current out on the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2-3 mA range and is dependant on the load and series resistance of the crystal. Test circuit is shown in the figure below.

Table 16. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance on EXTAL (C_{EXTAL})/XTAL (C_{XTAL}) [1,2] (pF)
00000	1.0
00001	2.0
00010	2.9
00011	3.8
00100	4.8
00101	5.7
00110	6.6
00111	7.5
01000	8.5
01001	9.4
01010	10.3
01011	11.2
01100	12.2
01101	13.1
01110	14.0

Table continues on the next page...

11.2 SAR ADC

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

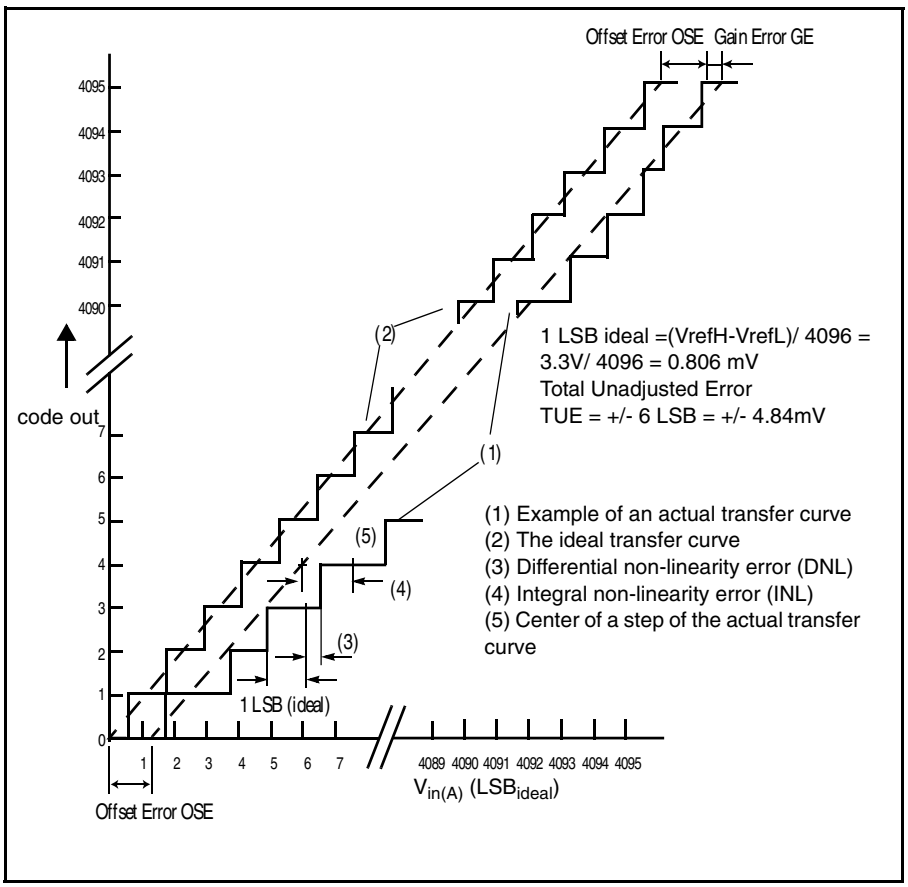

Figure 10. ADC characteristics and error definitions

11.2.1 Input equivalent circuit and ADC conversion characteristics

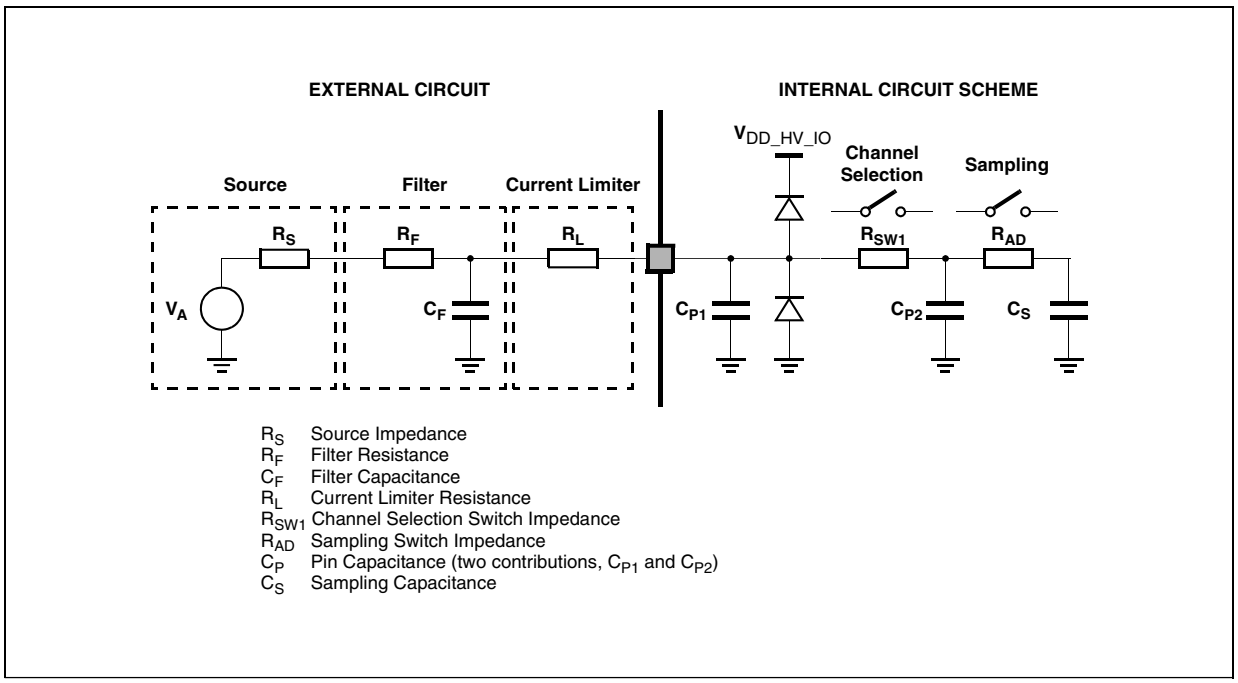

Figure 11. Input equivalent circuit

Table 19. ADC conversion characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK} [2]	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[3] frequency.)	—	20	—	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[4]	—	250	—	—	ns
t_{conv}	Conversion time[5]	80 MHz	700	—	—	ns
C_S [6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS[7]	Offset error	—	–6	—	6	LSB
GNE[7]	Gain error	—	–6	—	6	LSB
Input (double ADC channel)	Max leakage	150 °C	—	—	300	nA

Table continues on the next page...

Table 19. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	V_{REF} = 3.3 V, Fin ≤ 125 kHz	66	—	—	dB
SNR	Signal-to-noise ratio	V_{REF} = 5.0 V, Fin ≤ 125 kHz	68	—	—	dB
THD	Total harmonic distortion	@ 125 kHz	65	70	—	dB
ENOB[8]	Effective number of bits	Fin < 125 kHz	10.5	—	—	bits
SINAD	Signal-to-noise and distortion	Fin < 125 kHz	(6.02*ENOB)+1.76			dB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ	Without current injection	–6	—	6	LSB
$TUE_{IS1WWINJ}$	Total unadjusted error for IS1WWINJ	Without current injection	–6	—	6	LSB
I_{DD_VDDA}	Maximum operating current on VDDA	Tj = 150C VDD_LV_COR = 1.32 V	—	3.7	5	mA
I_{DD_VDDR}	Maximum operating current on VREF	Tj = 150C VDD_LV_COR = 1.32 V	—	150	600	µA
V_{BG_REF}, [9]	Band gap reference for self test	Trimmed, INPSAMP=0xFF	1.164	—[10]	1.236	V

1. $V_{DD\_HV\_IO}$ = 3.3 V -5%,+10%, T_J = –40 to +150 °C, unless otherwise specified, and analog input voltage from V_{AGND} to V_{AREF}
2. SAR ADC performance is not guaranteed when IRC is used as clock source for PLL0 to generate SAR ADC clock.
3. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
5. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
6. See the above figure.
7. Subject to change with additional -40°C characterization on final silicon version.
8. Below 4.5V, ENOB - 9.5b, THD- 60dB at Fin= 125KHz
9. Band gap reference only applies to Cut 2 silicon.
10. Minimum and maximum values are typical +/-3%

NOTE

- For spec complaint operation, do not expose clock sources, including crystal oscillator, IRC, PLL0, and PLL1 on the CLKOUT pads while the SAR ADC is converting.
- The ADC performance specifications are not guaranteed if two or more ADCs simultaneously sample the same shared channel.

11.3 S/D ADC

The SD ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{DIFF150}$	Signal to Noise Distortion Ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 1 $T_J < 150$ °C	72	—	—	dB
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 $T_J < 150$ °C	72	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 $T_J < 150$ °C	69	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 $T_J < 150$ °C	68.8	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 $T_J < 150$ °C	64.8	—	—	
$SINAD_{DIFF333}$	Signal to Noise Distortion Ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 $T_J < 150$ °C	66	—	—	dB
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 $T_J < 150$ °C	66	—	—	
		$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_SD} =$ $V_{DD\_HV\_ADV\_SD}$	63	—	—	

Table continues on the next page...

Table 25. LFAST PLL electrical characteristics (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Nominal	Max	
		Long term, f_{RF_REF} = 10 MHz	–500	—	500	ps
ΔPER_{EYE}	Output Eye Jitter (peak to peak)[3]	—	—	550	—	ps

1. The 640 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 26 MHz reference, the VCO frequency is 624 MHz.
2. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
3. Measured at the transmitter output across a 100 Ohm termination resistor on a device evaluation board. Refer to the figure below.

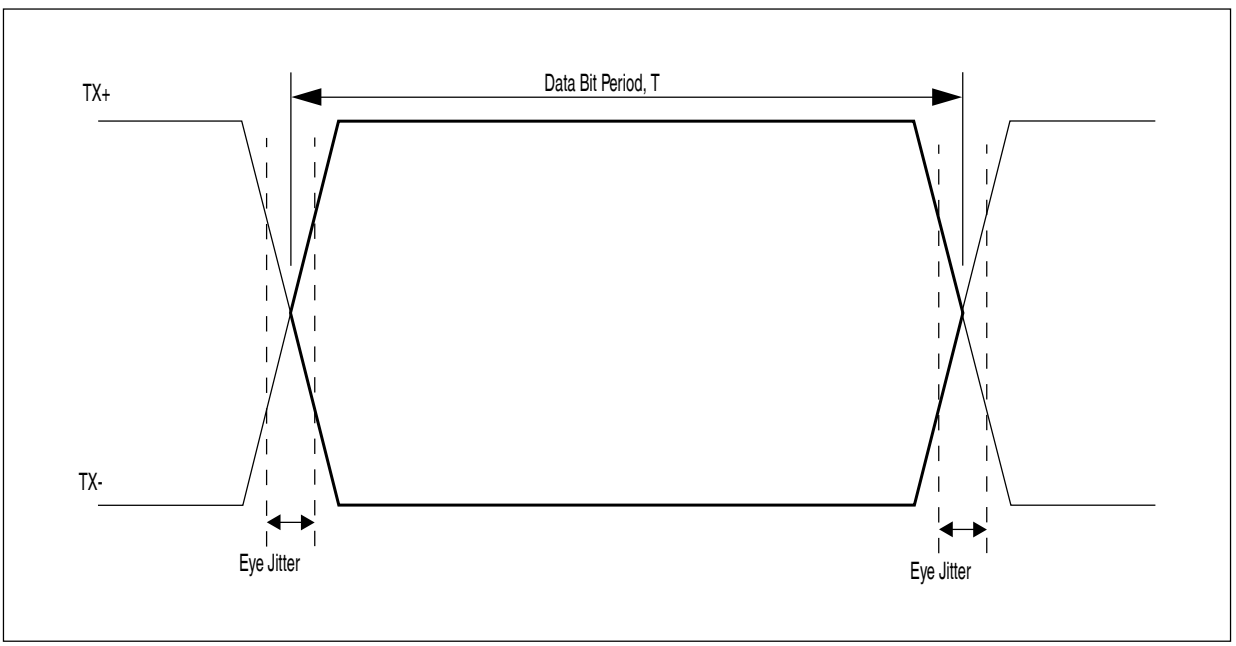

Figure 16. LFAST output 'eye' diagram

15 Aurora LVDS electrical characteristics

The following table describes the Aurora LVDS electrical characteristics.

All Aurora electrical characteristics are valid from -40 °C to 150 °C.

All specifications valid for maximum transmit data rate F_{TX}.

16.1.4 Regulator example for the 2SCR574d transistor

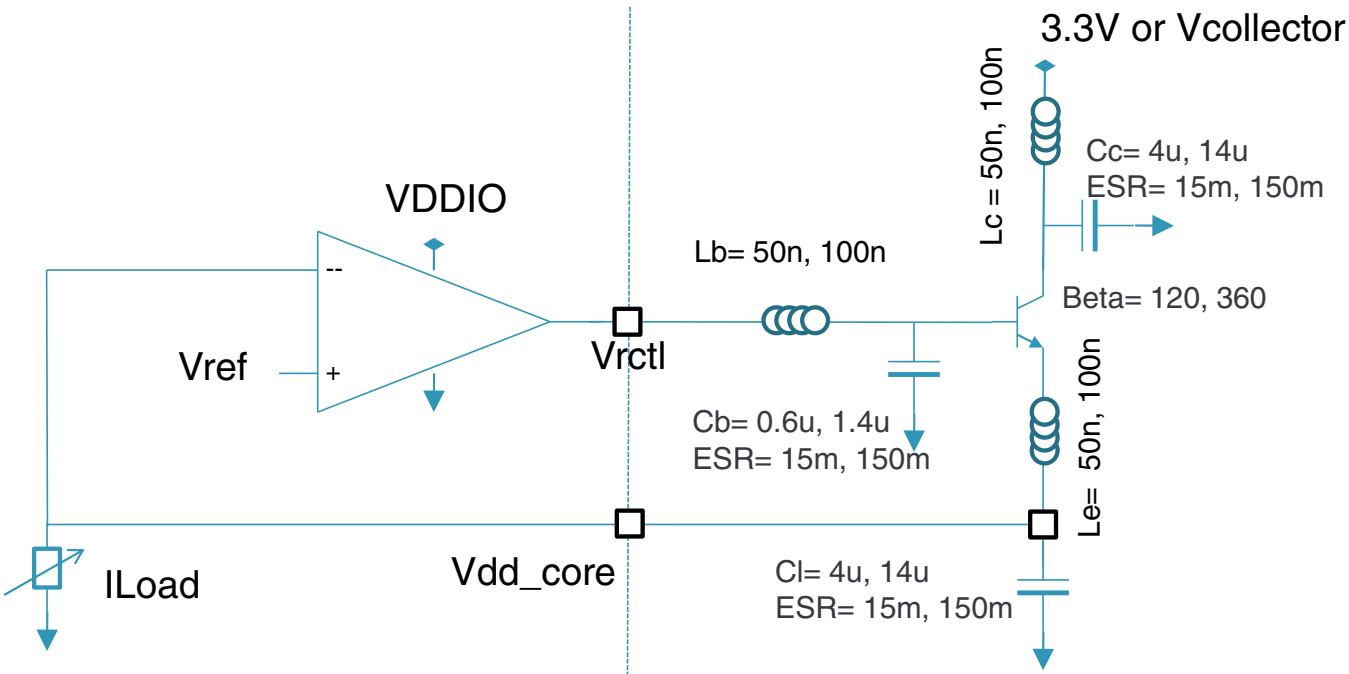

Figure 19. Regulator example

16.1.5 Device voltage monitoring

The LVD/HVDs for the device and their levels are given in the following table. Voltage monitoring threshold definition is provided in the following figure.

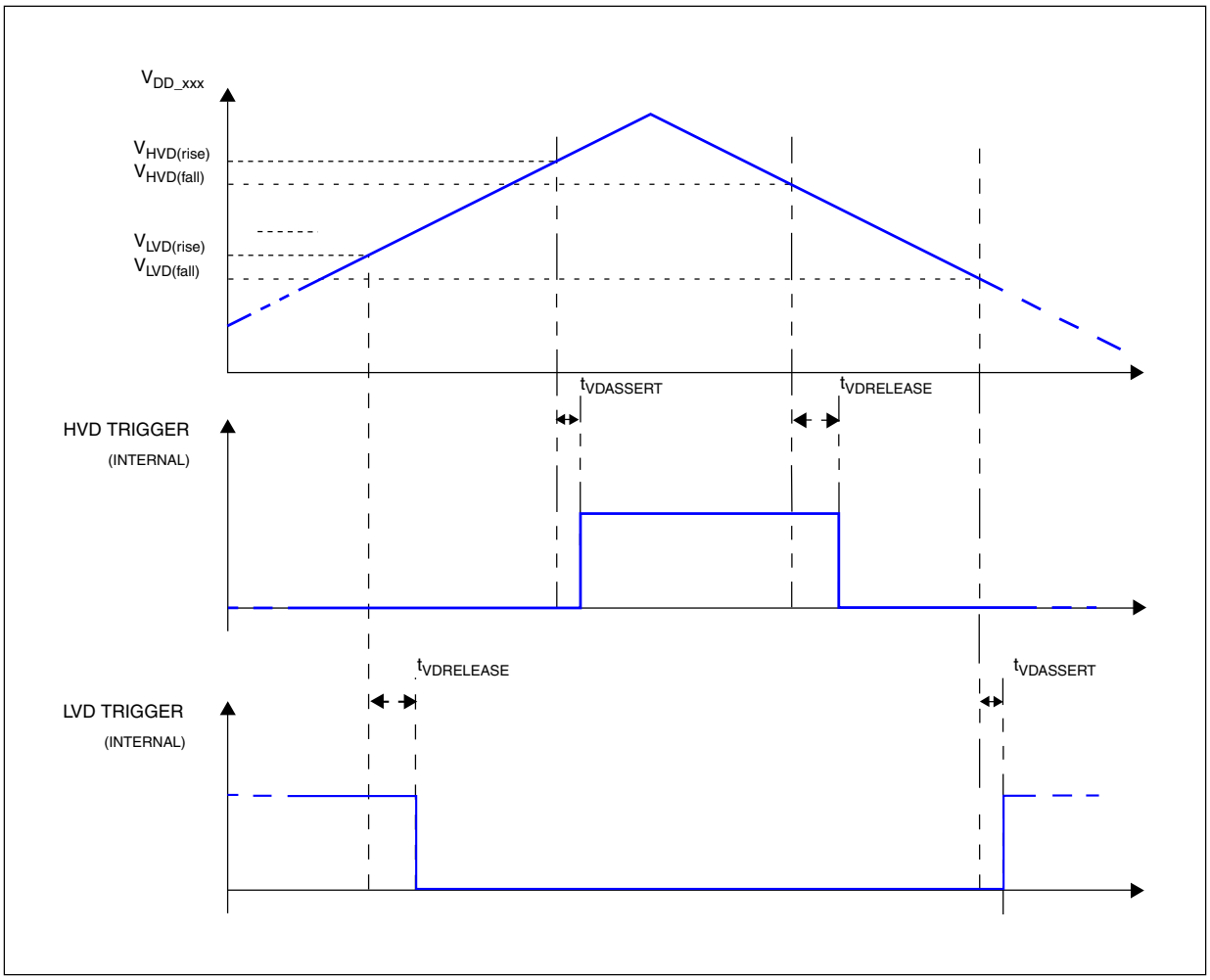

Figure 20. Voltage monitor threshold definition

For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by multiplying the supply current by 0.5 ohm.

LVD is released after $t_{VDRELEASE}$ temporization when upper threshold is crossed, LVD is asserted $t_{VDASSERT}$ after detection when lower threshold is crossed.

HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed.

Table 29. Voltage monitor electrical characteristics

Symbol	Parameter	Conditions	Configuration			Value			Unit
			Trim bits	Mask Opt.	Pow. Up	Min	Typ	Max	
POR085_c[1]	LV internal supply power on reset	Rising voltage (power up)	N/A	No	Enab.	870	920	970	mV
		Falling voltage (power down)				850	900	950	

Table continues on the next page...

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

18.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

The values presented in these sections are target values. A complete performance characterization of the pads (in all configuration combinations) is required before the final specifications can be released.

18.2.1.1 DSPI CMOS master mode – classic timing

All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

NOTE

In Table 40, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 40. DSPI CMOS master classic timing (full duplex and output only) - MTFE = 0, CPHA = 0 or 1

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	
			Medium	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	SCK and PCS drive strength				
			Very strong	25 pF	(N^3 x t_{SYS}, 4) - 16	—	ns
			Strong	50 pF	(N^3 x t_{SYS}, 4) - 16	—	
			Medium	50 pF	(N^3 x t_{SYS}, 4) - 16	—	
			PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N^3 x t_{SYS}, 4) - 29	—	
3	t_{ASC}	After SCK delay	SCK and PCS drive strength				
			Very strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}4) - 35	—	ns
			Strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, 4) - 35	—	
			Medium	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, 4) - 35	—	
			PCS medium and SCK strong	PCS = 0 pF	(M^5 x t_{SYS}, 4) - 35	—	

Table continues on the next page...

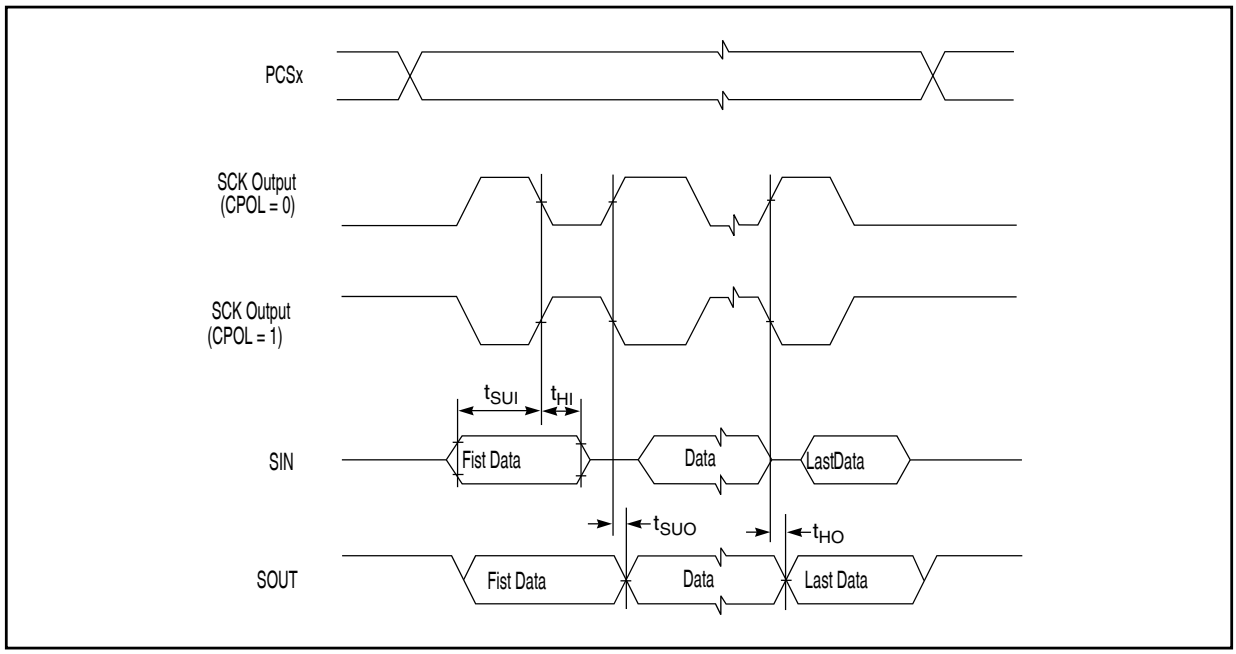

Figure 31. DSPI CMOS master mode – classic timing, CPHA = 1

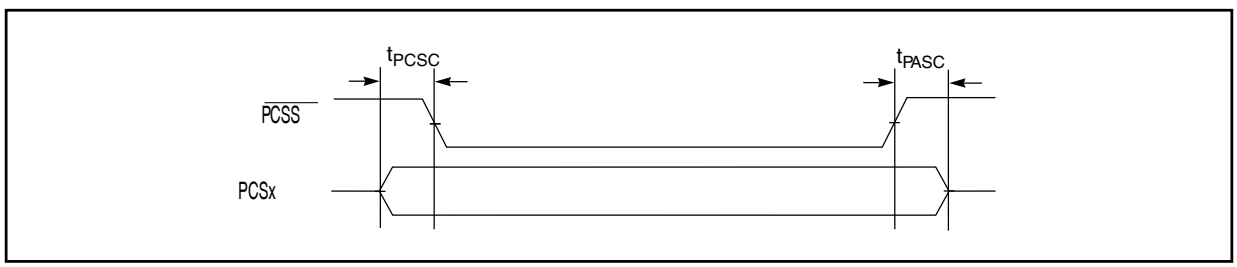

Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

18.2.1.2 DSPI CMOS master mode – modified timing

All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

NOTE

In Table 41, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 41. DSPI CMOS master modified timing (full duplex and output only) - MTFE = 1, CPHA = 0 or 1

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	

Table continues on the next page...

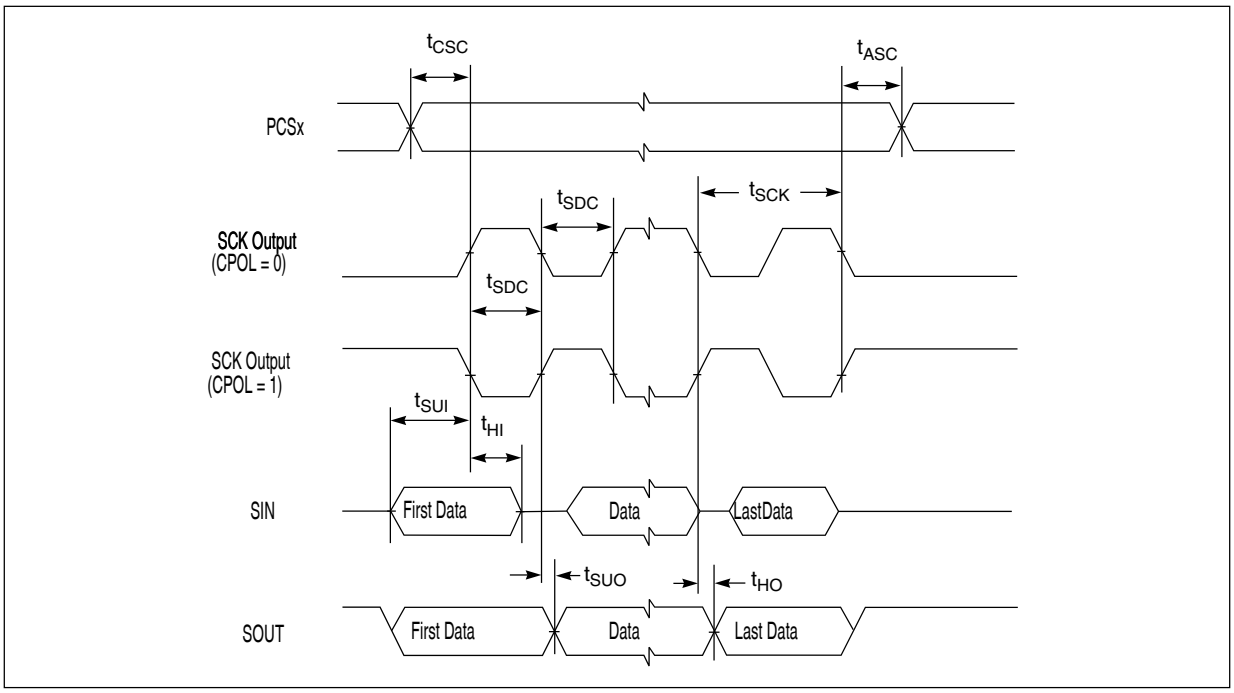

Figure 36. DSPI LVDS master mode – modified timing, CPHA = 0

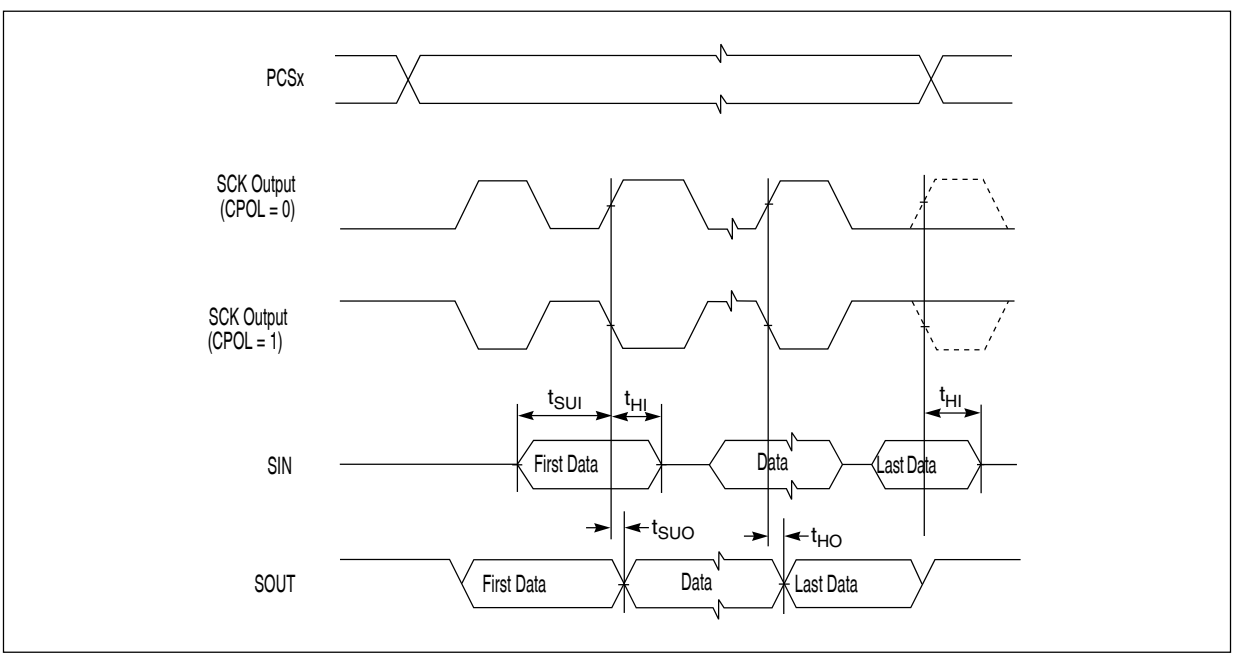

Figure 37. DSPI LVDS master mode – modified timing, CPHA = 1

18.2.1.4 DSPI master mode – output only

For Table 43 :

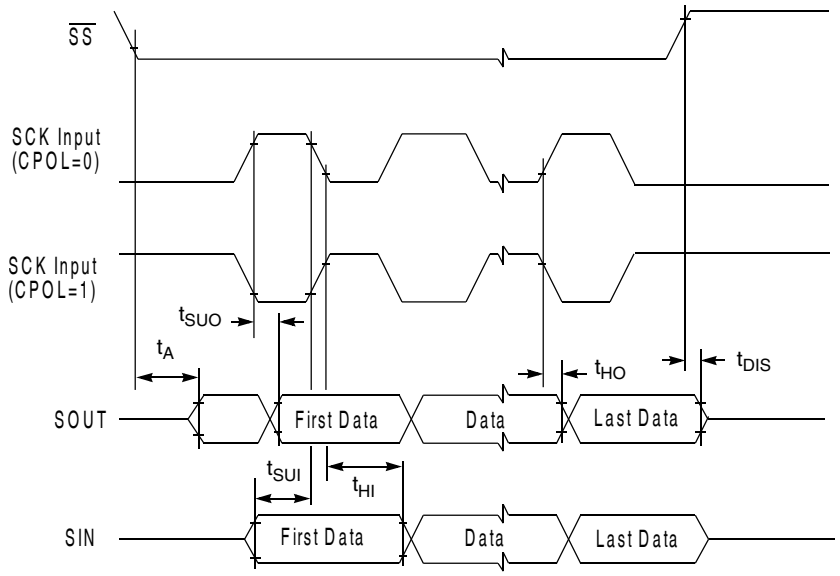

Figure 40. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1

18.3 FEC timing

The FEC supports the 10/100 Mbps MII, 10/100 Mbps MII-lite, and the 10 Mbps-only 7-wire interface.

18.3.1 MII-lite receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

All timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels.

Table 46. MII-lite receive signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

If you want the drawing for this package	Then use this document number
LQFP 144 PD	98ASS23177W
LQFP 176 PD	98ASS23479W
MAPBGA 252 PD	98ASA00468D
MAPBGA 292 ED	98ASA00261D

20 Thermal characteristics

The following tables describe the thermal characteristics of the device.

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

Table 56. Thermal characteristics for the 144-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	41.3	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	33.0	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32.4	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	26.7	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	21.5	°C/W
Junction to Case [5]	—	$R_{\theta JC}$	7.0	°C/W
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	0.25	°C/W
Junction to Package Lead[7]	Natural Convection	Ψ_{JB}	16.5	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 57. Thermal characteristics for the 176-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	49.9	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	33.8	°C/W

Table continues on the next page...

7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 59. Thermal characteristics for the 252-pin MAPBGA package 16 removed balls: 12 central, 4 corner peripheral

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	23.8	°C/W
Junction to Board[4]	Four layer board (2s2p)	$R_{\theta JB}$	15.9	°C/W
Junction to Package Lead[5]	Natural Convection	Ψ_{JB}	4.8	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

20.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21 Ordering information

Table 60. Ordering information

Part Number	Device Type	Flash/SRAM	Emulation RAM	Package	Frequency
SPC5746RK1MMT5	Sample PD[1]	4M / 256 KB	-	252 MAPBGA	200 MHz
SPC5745RK1MLU3	Sample PD	3M / 192 KB	-	176 LQFP	150 MHz
SPC5743RK1MLQ5	Sample PD	2M / 128 KB	-	144 LQFP	200 MHz
PPC5746R2K1MMZ5A	Sample ED[2]	4M / 256 KB	1 MB	292 MAPBGA	200 MHz

1. "PD" refers to a production device, orderable in quantity.
2. “ED" refers to an emulation device, orderable in limited quantities. An emulation device (ED) is for use during system development only and is not to be used in production. An ED is a Production PD chip combined with a companion chip to form an Emulation and Debug Device (ED) and includes additional RAM memory and debug features. EDs are provided

"as is" without warranty of any kind. In the event of a suspected ED failure, Freescale agrees to exchange the suspected failing ED from the customer at no additional charge, however Freescale will not analyze ED returns.

22 Revision history

Table 61. Revision history

Revision	Date	Description of changes
1	05/2013	Initial release.

2	12/2014	Overall:
		• Editorial changes.
		• Removed the Classification columns in spec tables and removed statements that values need to be characterized.
		• In footnotes changed cross references to figures to static text.
		
		In section Block diagram :
		• In Figure 1, changed "AIPS Bridge 0/1" to "AIPS PBridge_0/1".
		• In Figure 2 :
		  • Changed figure title (was "Peripherals block diagram").
		  • Changed "BAF" to "BAR".
		  • Added PBRIDGE_1, EIM, XBAR, and PBRIDGE_0.
		
		In section Introduction, removed section "Parameter classification".
		
		In section Absolute maximum ratings, Table 1 :
		• VDD_HV_IO_FEC spec: removed row for "Using Ethernet Reference to VSS" condition.
		• Corrected "VIDD_HV_IO_MSC" to "VDD_HV_IO_MSC".
		• Add parameter IIOMAX.
		• Deleted IMAXSEG parameter.
		
		In section Operating conditions :
		• Deleted sentence "The ranges in this table are design targets...".
		• Added a NOTE that all power supplies need to be powered up.
		• In Table 3 :
		  • Removed VDD_HV_FLA.
		  • Changed minimum voltage of VDD_HV_ADV_SD.
		  • Modified footnote for S/D ADC supply voltage.
		  • Modified footnote for SAR ADC supply voltage.
		  • Modified VRAMP spec to two separate specs for "VRAMP_VDD_LV" and "VRAMP_VDD_HV_IO_MAIN, VRAMP_VDD_HV_PMC".
		
		In section DC electrical specifications :
		• Removed the statement that the ranges are design targets.
		• In Table 5 :
		  • Modified I_{DD_LV} to show specs depending on device model. Modified footnote.
		  • Removed the "PMC only" row of the IDD_HV_PMC "internal core reg bypassed" spec.
		  • Removed IDD_MAIN_CORE_AC.
		  • Removed IDD_LKSTP_AC.
		  • Changed I_{DDSTBY_ON} value at 40 °C.
		  • Changed I_{DDSTBY_REG} parameter to "32 KB RAM Standby Regulator Current" (was "Standby Leakage Current"); changed condition to "V_{DDSTBY} @1.2 V to 5.9 V, Tj = 150C" (was "V_{DDSTBY} @1.3 V...")
		  • Removed IDDOFF.
		  • Added IDD_BD_STBY.
		  • Added IVDDA.

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes
		In section Ordering information table "Ordering Information", changed Part Numbers for the 176 LQFP PD and the ED.

5	10/2016	Editorial updates.
		
		In section Operating conditions table "Device operating conditions" added foootnote to $V_{DD\_HV\_IO\_JTAG}$.
		
		In section Input pad specifications table "I/O input DC electrical characteristics" for I_{LKG} added condition "$V_{SS} < V_{IN} < V_{DD\_HV\_IO*}$"
		
		In section ADC input description table "Analog Input Leakage and Pull-Up/Down DC electrical characteristics" for ILK_AD added conditions "$V_{SS\_HV\_ADV\_SAR} < V_{IN} < V_{DD\_HV\_ADV\_SAR}$" and "$V_{SS\_HV\_ADV\_SD} < V_{IN} < V_{DD\_HV\_ADV\_SD}$".
		
		In section Recommended power transistors table "Recommended operating characteristics" for I_{CMaxDC} changed the parameter from "Minimum peak collector current" to "Maximum DC collector current".
		
		In section SAR ADC table "ADC conversion characteristics":
		• Removed the condition for t_{sample}.
		• Removed the Min and added the formula (6.02*ENOB) + 1.76 for SINAD.
		• Changed the Min value from 650 to 700 for t_{conv}.
		
		In section S/D ADC table "SDn ADC electrical specification":
		• Removed Z_{IN} specification
		• Added Z_{DIFF}, Z_{CM}, and ΔV_{INTCM} specifications
		• For R_{BIAS}:
		  • Changed Parameter description from "Bias resistance" to "Bare bias resistance"
		  • Changed Min from 100 kΩ to 110 kΩ
		  • Changed Typ from 125 kΩ to 144 kΩ
		  • Changed Max from 160 kΩ to 180 kΩ
		
		In section Flash memory AC timing specifications table "Flash memory AC timing specifications" for t_{psus}:
		• Changed Typical from 7 µs plus four system clock periods to 9.4 µs plus four system clock periods
		• Changed Max from 9.1 µs plus four system clock periods to 11.5 µs plus four system clock periods

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Document Number MPC5746R
Revision 5, 10/2016