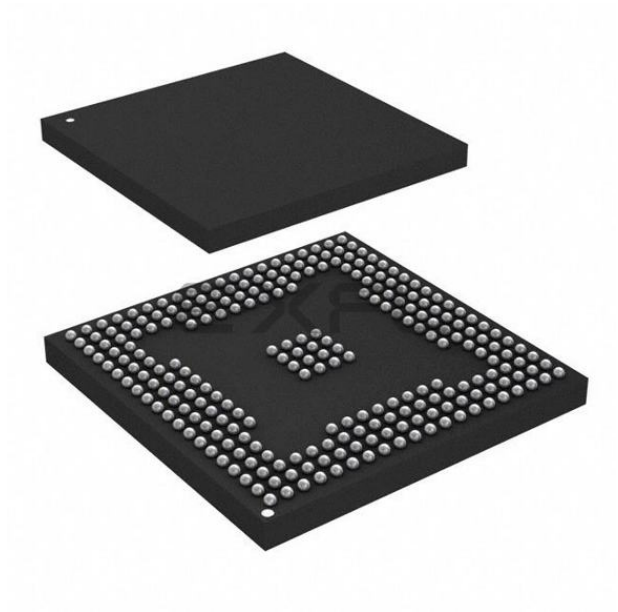

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Tri-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	252-LFBGA
Supplier Device Package	252-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746rk1mmt5

1.1 Block diagram

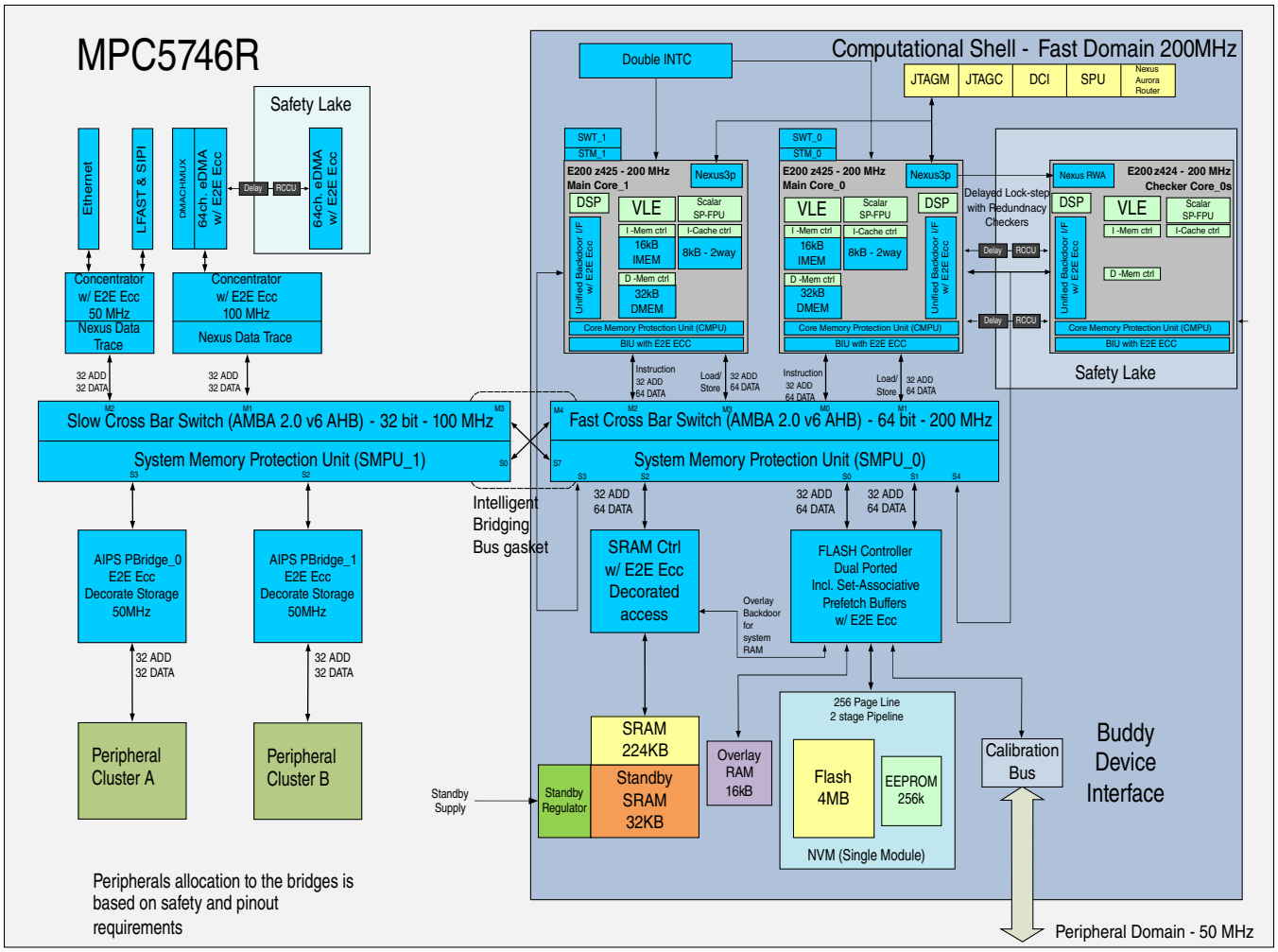


Figure 1. Core block diagram

Table 10. I/O current consumption at VDD_HV_IO = 3.6 V (continued)

Cell	VDD_HV_IO (V)	Load (pF)	Period1 (ns)	MSCR[OERC]	Idde AVG (mA)	Idde RMS (mA)
		200	130		3	9
		50	150	00	1.6	4
		200	200		4	11

Table 11. I/O current consumption at VDD_HV_IO = 5.5 V

Cell	VDD_HV_IO (V)	Load (pF)	Period1 (ns)	MSCR[OERC]	Idde AVG (mA)	Idde RMS (mA)
pad_sr_hv	5.5	25	9	11	37	83
		50	10.2		42	89
		200	26		46	92
		25	10.5	10	25	53
		50	16		21	44
		200	44		26	49
		50	54	01	6	14
		200	80		15	35
		50	80	00	4	9
		200	130		9	22

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{MAXSEG} value given in the table "Absolute maximum ratings".

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{MAXSEG} value given in the table "Device operating conditions".

Note

The MPC5746R I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel workbook file attached to the Reference Manual.

9 Reset pad (PORST, RESET) electrical characteristics

The device implements a dedicated bidirectional reset pin (PORST).

11.2 SAR ADC

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

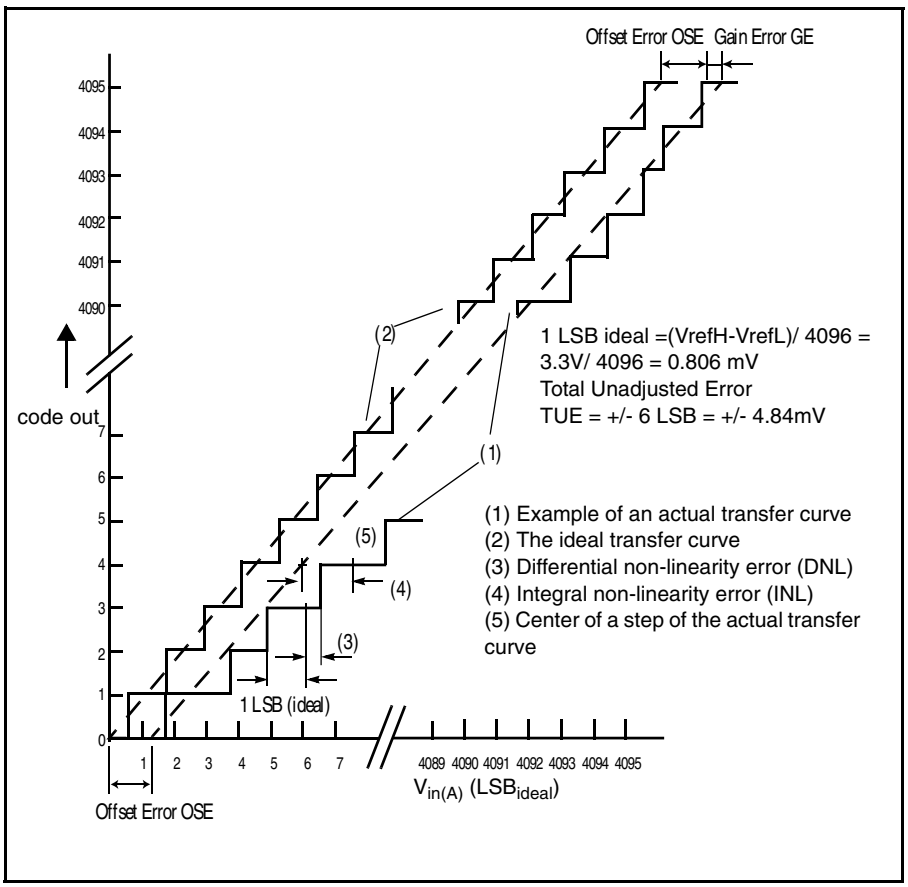


Figure 10. ADC characteristics and error definitions

Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

Table 20. SDn ADC electrical specification

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	$V_{DD\_HV\_ADV\_SD}$	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended. $V_{INM} = V_{SS\_HV\_ADR\_SD}$	$V_{DD\_HV\_ADR\_SD}$/GAIN			V
		Single ended. $V_{INM} = 0.5*V_{DD\_HV\_ADR\_SD}$ GAIN = 1	$\pm 0.5*V_{DD\_HV\_ADR\_SD}$			
		Single ended. $V_{INM} = 0.5*V_{DD\_HV\_ADR\_SD}$ GAIN = 2,4,8,16	$\pm V_{DD\_HV\_ADR\_SD}$/GAIN			
		Differential $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$\pm V_{DD\_HV\_ADR\_SD}$/GAIN			
f_{ADCD_M}	S/D clock frequency	$T_J < 150$ °C	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	$T_J < 150$ °C	—	—	333	ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	S/D register resolution	2's complement notation	16[4]			bit
GAIN	ADC gain	Defined through ADC_SD[PGA] register. Only integer power of 2 are valid gain.	1	—	16	—
$\lvert\delta_{GAIN}\rvert$	Absolute value of the ADC gain error[5]	Before calibration (applies to gain settings =1)	—	—	1	%
		After calibration[6] $\Delta V_{DD\_HV\_ADR\_SD} < 5\%$ $\Delta V_{DD\_HV\_ADV\_SD} < 10\%$ $T_J < 50$ °C	—	—	0.1	%
		After calibration[6] $\Delta V_{DD\_HV\_ADR\_SD} < 5\%$ $\Delta V_{DD\_HV\_ADV\_SD} < 10\%$ $T_J < 150$ °C	—	—	0.2	%
V_{OFFSET}	Conversion offset	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	20	mV
		After calibration[6]	—	—	5	mV
$SNR_{DIFF150}$,[7]	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_SD} < 5.5$[7] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$	78	—	—	dB

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		GAIN = 1 T_J < 150 °C				
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	75	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	72	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	69	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	65	—	—	
$SNR_{DIFF333}$[7]	Signal to noise ratio in differential mode 333 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	72	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	69	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	66	—	—	

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	63	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	60	—	—	
SNR_{SE150}[7]	Signal to noise ratio in single ended mode 150 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	72	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	69	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	66	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	63	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_DS}$ = $V^{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	55	—	—	

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_{S_D}	S/D ADC sampling capacitance after sampling switch[14]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least 1 ADCD enabled	—	—	3.5	mA
I_{ADV_D}	ADCD supply consumption	ADCD enabled	—	2.5	8	mA
ΣI_{ADR_D}	Reference current for one SDADC	ADCD enabled	—	10	50	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be 'clipped'.
2. VINP is the input voltage applied to the positive terminal of the SD ADC.
3. VINM is the input voltage applied to the negative terminal of the SD ADC.
4. For Gain=16, SDADC Resolution is 15 bit.
5. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{DD\_HV\_ADR\_SD}$ for differential "differential mode" and single ended mode with negative input=$0.5*V_{DD\_HV\_ADR\_SD}$ ". Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0". Both Offset and Gain Calibration is guaranteed for +/-5% variation of $V_{DD\_HV\_ADR\_SD}$, +/-10% variation of $V_{DD\_HV\_ADV\_SD}$, +/-50 C temperature variation.
7. S/D ADC is functional in the range $3.6V < V_{DD\_HV\_ADV\_SD} < 4.5V$ and $3.0V < V_{DD\_HV\_ADR\_SD} < 4.5$ V, SNR paramter degrades by 9 dB.
8. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
9. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
10. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
11. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
12. The ±1% passband ripple specification is equivalent to 20 * log10 (0.99) = 0.873 dB.
13. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the following formula: REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator, and fPBRIDGEx_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
14. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

12 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 21. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
—	Junction temperature monitoring range	—	–40	—	150	°C
T_{SENS}	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	Accuracy	—	–7	—	7	°C

13 LVDS fast asynchronous serial transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to both the LFAST and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

13.1 LFAST interface timing diagrams

Table 22. LVDS pad startup and receiver electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{PD2NM_TX}	Transmitter startup time (power down to normal mode)[1]	—	—	0.4	0.55	µs
t_{SM2NM_TX}	Transmitter startup time (sleep mode to normal mode)[2]	Not applicable to the MSC/ DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	Receiver startup time (power down to normal mode)[3]	—	—	20	40	ns
t_{PD2SM_RX}	Receiver startup time (power down to sleep mode)[4]	Not applicable to the MSC/ DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER						
V_{ICOM}	Common mode voltage	—	0.15[5]	—	1.6[6]	V
$\lvert\Delta_{VI}\rvert$	Differential input voltage	—	100	—	—	mV
V_{HYS}	Input hysteresis	—	25	—	—	mV
R_{IN}	Terminating resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	80	100	120	Ω
		$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	80	115	150	Ω
C_{IN}	Differential input capacitance[7]	—	—	3.5	6.0	pF
I_{LVDS_RX}	Receiver DC current consumption	Enabled	—	—	0.5	mA

1. Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods. The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values.
2. Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode. All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from -40 °C to 150 °C.
3. Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.
4. Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.
5. Absolute min = 0.15 V – (285 mV/2) = 0 V
6. Absolute max = 1.6 V + (285 mV/2) = 1.743 V
7. Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 23. LFAST transmitter electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{DATA}	Data rate	—	—	—	320	Mbps
V_{OS}	Common mode voltage	—	1.08	—	1.32	V
$\lvert V_{OD}\rvert$	Differential output voltage swing (terminated)[1, 2]	—	100	200	285	mV
t_{TR}	Rise/Fall time (10%–90% of swing) [3, 4]	—	0.26	—	1.5	ns

Table continues on the next page...

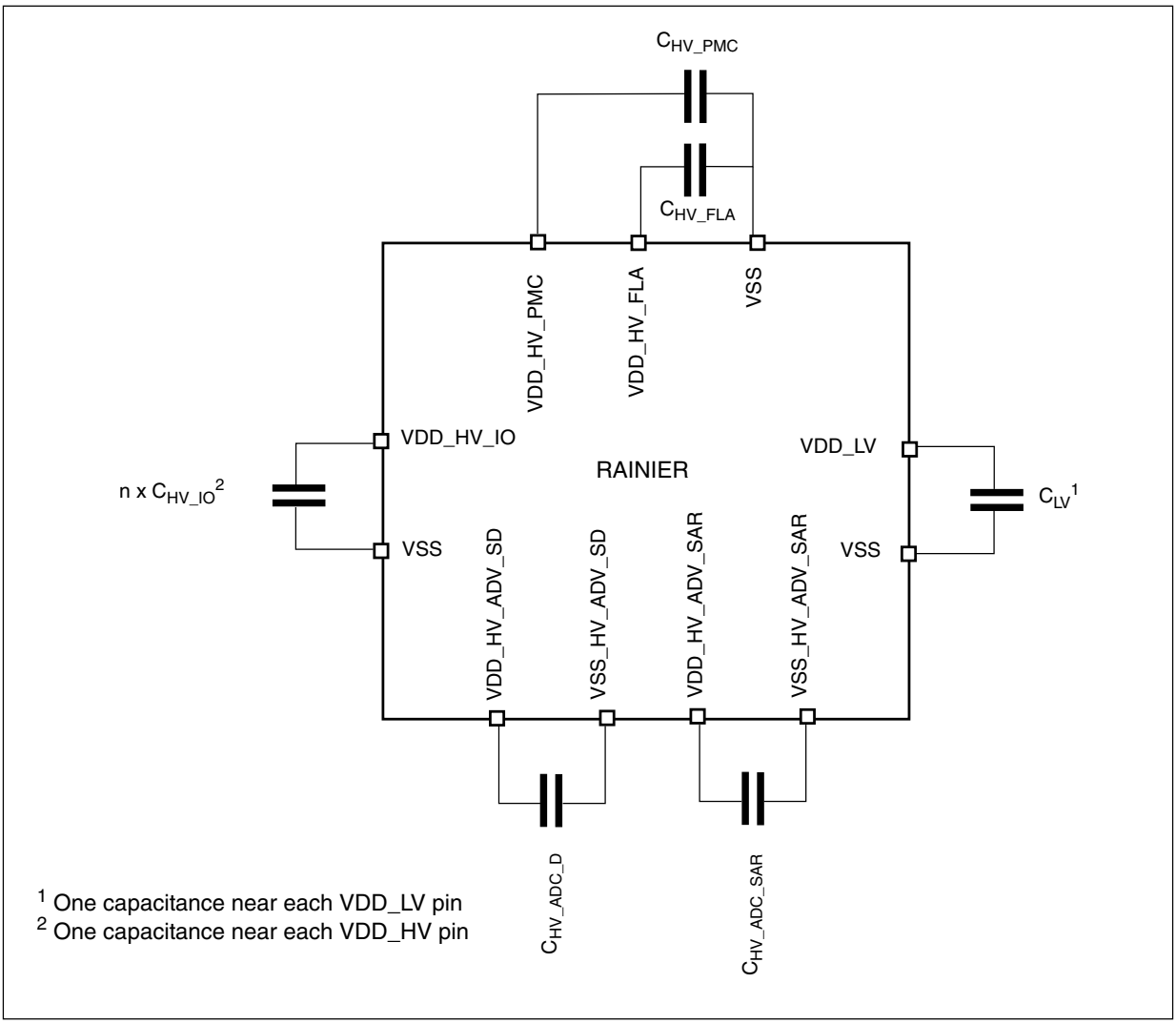


Figure 17. Recommended supply pin circuits

The following table describes the supply stability capacitances required on the device for proper operation.

Table 28. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD_LV} external bulk capacitance[2, 3]	—	4.7	—	—	µF
C_{HV_PMC}	Minimum $V_{DD\_HV\_PMC}$ external bulk capacitance [2, 4]	—	4.7	—	—	µF
C_{HV_IO}	Minimum VDD_HV_IO external capacitance[2]	—	4.7	—	—	µF
C_{HV_FLA}	Minimum $V_{DD\_HV\_FLA}$ external capacitance[5]	—	2.0			µF
$C_{HV\_ADC\_SAR}$	Minimum $V_{DD\_HV\_ADV\_SAR}$ external capacitance[6]		10	—	—	µF

Table continues on the next page...

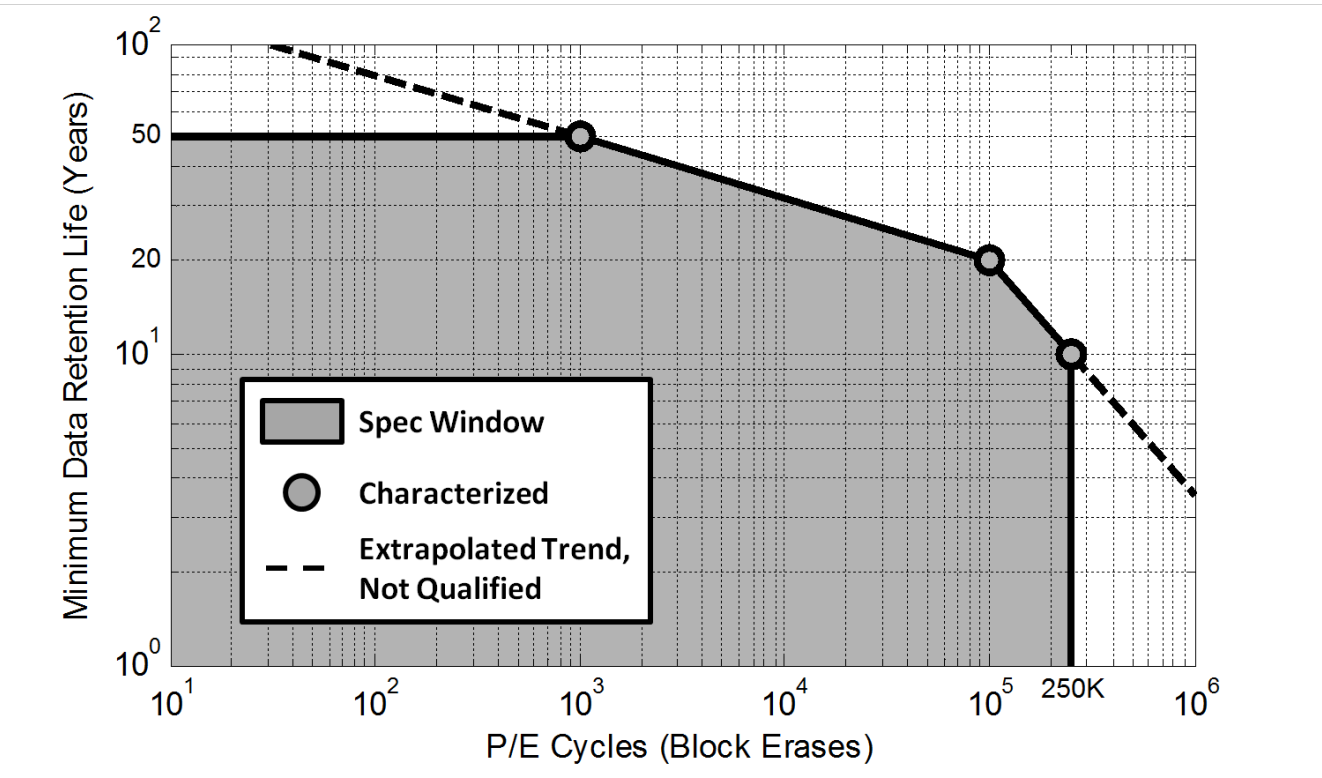
Table 32. Flash memory module life specifications (continued)

Symbol	Characteristic	Conditions	Min	Typical	Units
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

17.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



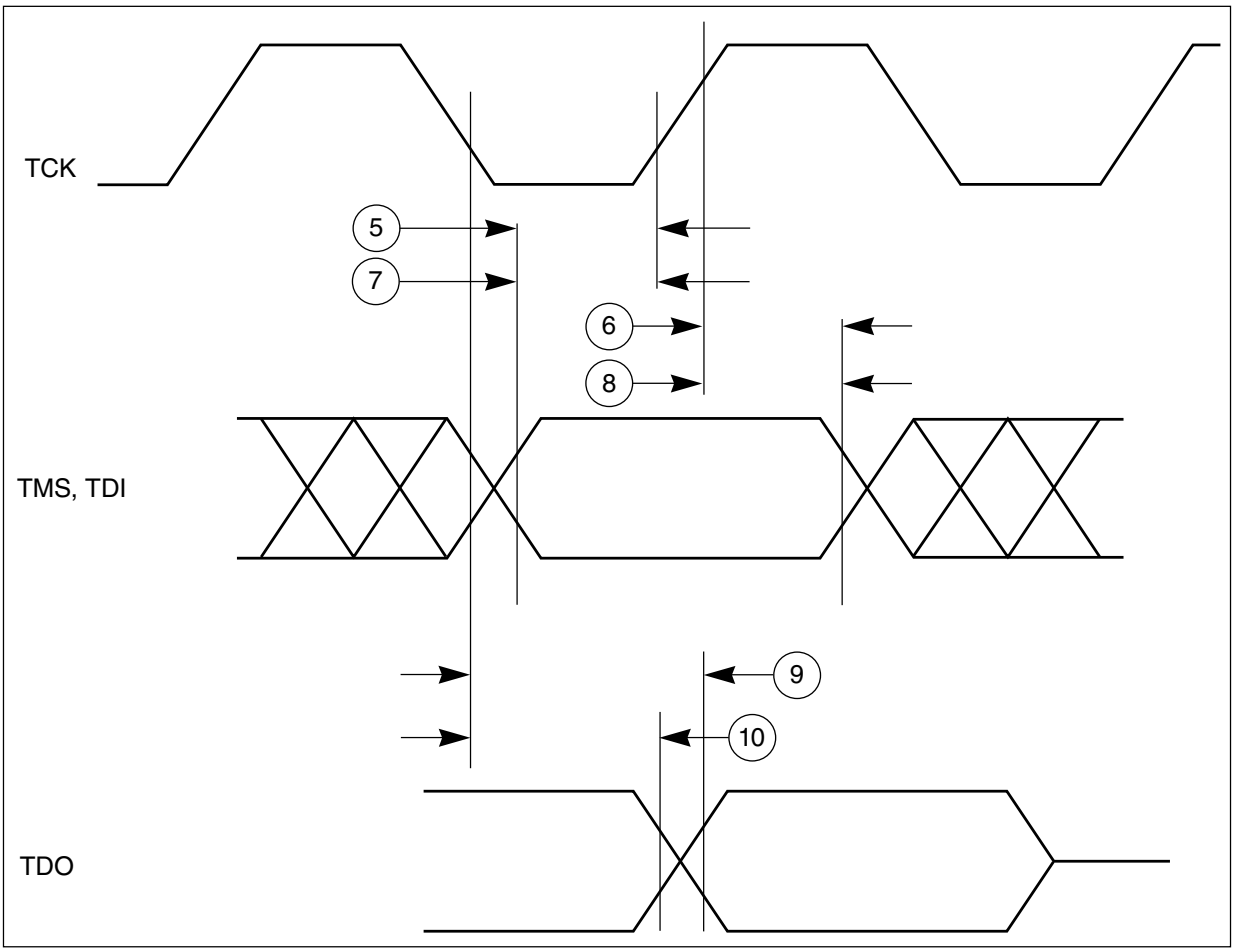


Figure 28. Nexus TDI, TMS, TDO timing

18.1.3 Aurora LVDS interface timing

Table 37. Aurora LVDS interface timing specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
Data Rate					
—	Data rate	—		1250	Mbps
STARTUP					
t_{STRT_BIAS}	Bias startup time[1]	—	—	5	µs
t_{STRT_TX}	Transmitter startup time[2]	—	—	5	µs
t_{STRT_RX}	Receiver startup time[3]	—	—	4	µs

1. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
2. Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3. Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

18.1.3.1 Aurora debug port timing

Table 38. Aurora debug port timing

#	Symbol	Parameter		Value		Unit
				Min	Max	
1	t_{REFCLK}	Reference clock frequency		625	1200	MHz
1a	t_{MCYC}	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	Reference clock duty cycle		45	55	%
3	J_{RC}	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	Reference clock stability		50	—	PPM
5	BER	Bit error rate		—	10^{-12}	—
6	J_D	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	Transmit lane total jitter		—	0.35	OUI
8	S_O	Differential output skew		—	20	ps
9	S_{MO}	Lane to lane output skew		—	1000	ps
10	OUI	Aurora lane unit interval[1]	625 Mbps	1600	1600	ps
			1.25Gbps	800	800	ps

1. ± 100 PPM

Table 40. DSPI CMOS master classic timing (full duplex and output only) - MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
				SCK = 50 pF			
4	t_{SDC}	SCK duty cycle[6]	SCK drive strength				
			Very strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	
			Medium	0 to 50 pF	$^1/_2t_{SCK}$ - 5	$^1/_2t_{SCK}$ + 5	
PCS strobe timing							
5	t_{PCSC}	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
			Strong	25 pF	13.0	—	ns
6	t_{PASC}	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
			Strong	25 pF	13.0	—	ns
SIN setup time							
7	t_{SUI}	SIN setup time to SCK[8]	SCK drive strength				
			Very strong	25 pF	25.0	—	ns
			Strong	50 pF	31.0	—	
			Medium	50 pF	52.0	—	
SIN hold time							
8	t_{HI}	SIN hold time from SCK[8]	SCK drive strength				
			Very strong	0 pF	-1.0	—	ns
			Strong	0 pF	-1.0	—	
			Medium	0 pF	-1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK[9]	SOUT and SCK drive strength				
			Very strong	25 pF	—	7.0	ns
			Strong	50 pF	—	8.0	
			Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK[9]	SOUT and SCK drive strength				
			Very strong	25 pF	-7.7	—	ns
			Strong	50 pF	-11.0	—	
			Medium	50 pF	-15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

Table 44. DSPI CMOS master timing - output only - timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	ns
			Medium	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[3]	SCK and PCS drive strength				
			Very strong	25 pF	7	—	ns
			Strong	50 pF	8	—	ns
			Medium	50 pF	16	—	ns
			PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	PCS hold after SCK[3]	SCK and PCS drive strength				
			Very strong	PCS = 0 pF SCK = 50 pF	-14	—	ns
			Strong	PCS = 0 pF SCK = 50 pF	-14	—	ns
			Medium	PCS = 0 pF SCK = 50 pF	-33	—	ns
			PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	-35	—	ns
4	t_{SDC}	SCK duty cycle[4]	SCK drive strength				
			Very strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Strong	0 to 50 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
			Medium	0 to 50 pF	$^1/_2t_{SCK}$ - 5	$^1/_2t_{SCK}$ + 5	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[5]	SOUT and SCK drive strength				
			Very strong	25 pF	—	7.0	ns
			Strong	50 pF	—	8.0	ns
			Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[5]	SOUT and SCK drive strength				
			Very strong	25 pF	-7.7	—	ns
			Strong	50 pF	-11.0	—	ns
			Medium	50 pF	-15.0	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

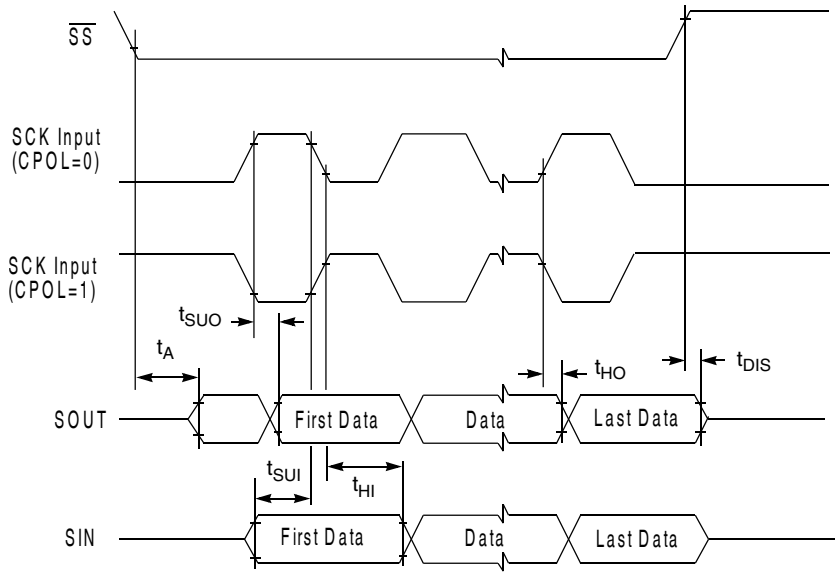


Figure 40. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1

18.3 FEC timing

The FEC supports the 10/100 Mbps MII, 10/100 Mbps MII-lite, and the 10 Mbps-only 7-wire interface.

18.3.1 MII-lite receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

All timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels.

Table 46. MII-lite receive signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

If you want the drawing for this package	Then use this document number
LQFP 144 PD	98ASS23177W
LQFP 176 PD	98ASS23479W
MAPBGA 252 PD	98ASA00468D
MAPBGA 292 ED	98ASA00261D

20 Thermal characteristics

The following tables describe the thermal characteristics of the device.

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

Table 56. Thermal characteristics for the 144-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	41.3	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	33.0	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	32.4	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	26.7	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	21.5	°C/W
Junction to Case [5]	—	$R_{\theta JC}$	7.0	°C/W
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	0.25	°C/W
Junction to Package Lead[7]	Natural Convection	Ψ_{JB}	16.5	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 57. Thermal characteristics for the 176-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	49.9	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	33.8	°C/W

Table continues on the next page...

Table 61. Revision history

Revision	Date	Description of changes

		In section Input pad specifications :
		• In Table 7 :
		  • Added footnote that supported input levels vary according to pad types.
		  • Corrected VILTTL Min and Max values.
		  • Corrected VIHAUTO, VILCMOS_H and VILCMOS Min value.
		• In Table 8 :
		  • Modified |IWPU| Min values for condition Vin = VIH = 0.65 * VDD_HV_IO.
		  • Modified |IWPD| Min values for condition Vin = VIL = 0.35 * VDD_HV_IO.
		• Removed the "Analog Input Leakeage and Pull-Up/Down DC electrical characteristics" table and the preceding introductory paragraph to be moved to the ADC input description section.
		
		In section Output pad specifications, Table 9, changed VOH and VOL specs to two separate specs for 3V pads and 5V pads respectively. Corrected VOH Min and VOL Max values.
		
		In section I/O pad current specifications :
		• Added I/O Current Consumption tables.
		• Modified NOTE on Excel file attached to the Reference Manual.
		
		Added section Reset pad (PORST, RESET) electrical characteristics.
		
		In section Oscillator and FMPLL :
		• In Table 13, removed PLL0_PHI0 single period jitter row.
		• In Table 15 :
		  • Modified footnote for CS_EXTAL and CS_XTAL.
		  • Modified gm (Oscillator Transconductance) spec.
		  • Removed VHYS.
		
		In section ADC modules, revised the subsection structure and titles:
		• Added section ADC input description with content moved from the "Input pad specifications" section.
		• Section "Input impedance and ADC accuracy" renamed to Input equivalent circuit and ADC conversion characteristics with all content except Figure 11 and Table 19 removed.
		• Removed erroneous section "SAR ADC electrical specification".
		
		In section SAR ADC, Table 19 :
		• Added footnote ("SAR ADC performance is not guaranteed...") to f_{CK} symbol.
		• Changed t_{sample} specification min value to 250 ns (was 275).
		• Added footnote to OFS and GNE. Changed OFS and GNE min and max values.
		• Removed "Input (singe ADC channel)".
		• Removed injection row for "Input (double ADC channel)".
		• SNR, THD, SINAD, and ENOB specifications: changed frequency condition to 50 kHz (was 125 kHz).
		• Changed SNR Min values.
		• Added footnote to ENOB.
		• Added I_{DD_VDDA}, I_{DD_VDDR}, and V_{BG_REF} parameters.
		
		In section S/D ADC, Table 20 :
		• For V_{IN_PK2PK} parameter second and third rows, changed V_{SS} in Conditions to V_{DD}.
		• For f_{ADCD_M} specification, removed sampling frequency footnote from parameter.
		• Added footnote to RESOLUTION value.
		• For $\|\delta_{GAIN}\|$ specification added footnote to parameter and added new row with more detailed "After calibration" conditions.
		• Moved footnote "S/D ADC is functional in the range..." from the Z_{IN} to the SNR parameters.
		• Changed all instances of “4.0 < VDD_HV_ADV_SD < 5.5” in the Conditions column to “4.5 < VDD_HV_ADV_SD < 5.5”. Modified voltage range in its footnote.
		• Changed SNR_{SE150}, GAIN = 16 condition min value to 55 dB (was 60).
		• Changed $SINAD_{SE150}$, GAIN = 16 condition min value to 54 dB (was 59).

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes
		• Removed parenthetical phrase from table title. • Made overall updates to spec values. • Removed footnote 7. In section Flash memory Array Integrity and Margin Read specifications, Table 31 : • Removed parenthetical phrase from table title. • Made overall updates to spec values. In section Flash memory module life specifications, Table 32, removed parenthetical phrase from table title. In section Flash memory AC timing specifications, Table 33, removed parenthetical phrase from table title. Added section Flash read wait state and address pipeline control settings. In section Power management integration, Table 28, changed the footnotes for t_{TCYC} Min values to have the same footnote number as they were identical. In section DSPI timing with CMOS and LVDS, Table 39, LVDS (Master mode) specification: changed Max usuable frequency to 40 MHz (was 33 MHz). In section DSPI CMOS master mode – classic timing : • Added NOTE. • In Table 40, changed PCS strobe timing values. In section DSPI CMOS master mode – modified timing : • Added NOTE. • In Table 41, changed PCS strobe timing values. In section DSPI LVDS master mode – modified timing, Table 42, changed significant digits for some values. In section DSPI master mode – output only : • Modified format paragraphs leading the tables. Removed NOTE. • In Table 43, changed the t_{CSV} strong drive value and t_{HO} LVDS value. • In Table 44, changed significant digits for some values. In section FEC timing, corrected the title of MII-lite and RMII serial management channel timing subsections. In section MII-lite transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK), Table 47, modified footnote for output parameters. In section RMII serial management channel timing (MDIO and MDC), added Note on reference for timing specifications. In section RMII transmit signal timing (TXD[1:0], TX_EN), Table 52, modified R6 max value. In section UART timings, Table 53, removed 100 MHz specification. "Package drawings" section renamed to Obtaining package dimensions, with package drawing document numbers to search at the Freescale website. Drawings removed from this document. In section Thermal characteristics : • Added table for 144 LQFP. • Moved table for 176 LQFP before 252 MAPBGA and updated table. • Replaced table for 252 MAPBGA with two separate tables for package with full solder balls and package with 16 removed balls. In section Ordering information, replaced the table.
3	09/2015	On the cover page:

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes

		• Added NOTE "For spec complaint operation, do not expose clock sources, including crystal oscillator, IRC, PLL0, and PLL1 on the CLKOUT pads while the SAR ADC is converting."
		• Added NOTE: "The ADC performance specifications are not guaranteed if two or more ADCs simultaneously sample the same shared channel".
		
		In section S/D ADC :
		• In Table 20 :
		  • For $THD_{DIFF333}$ GAIN = 16, updated Min value.
		  • For I_{ADV_D}, updated Max value.
		
		In section LFAST and MSC /DSPI LVDS interface electrical characteristics :
		• After table Table 24 added NOTE "For optimum LVDS performance, it is recommended to set the neighbouring GPIO pads to use Weak Drive".
		
		In section Device voltage monitoring :
		• In Table 29 :
		  • For LVD_core_hot, LVD_HV, and LVD_IO specs, removed the untrimmed Rising voltage and Falling voltage rows.
		  • For LVD_core_hot, changed Mask Opt. value to "No".
		
		In section Regulator example for the 2SCR574d transistor, figure "Regulator example", changed “5V or Vcollector” to “3.3V or Vcollector”.
		
		In section DSPI CMOS master mode – classic timing, Table 40 :
		• Changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		• In tSUI and tHI specs' footnote, removed reference to "Automotive" thresholds.
		
		In section DSPI CMOS master mode – modified timing, Table 41 :
		• Changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		• In tSUI and tHI specs' footnote, removed reference to "Automotive" thresholds.
		
		In section DSPI master mode – output only, Table 44, changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		
		Added section eMIOS timing.
		
		In section Ordering information, Table 60 :
		• Updated Part Numbers.
		• Updated Emulation device footnote.

4	03/2016	In section Block diagram, Figure 2 : • "DECIM" changed to "DECFILTER". • "SIPI" changed to "Zipwire". • I/O lines added to Zipwire, SIUL2, REACM, eTPU, eMIOS, IGF, and XOSC. In section Absolute maximum ratings table "Absolute maximum ratings", removed I_{IOMAX} spec and added I_{MAXSEG} spec. In section Operating conditions table "Device operating conditions": • For the FEC I/O supply voltage, MSC I/O supply voltage, and JTAG I/O supply voltage specs, removed the LVD enabled/disabled distinction. • Added footnote to I_{MAXSEG}. In section I/O pad current specifications : • Modified the descriptions in the two paragraphs after the tables. • Removed the third paragraph after the tables and the first Note. Added section DSPI CMOS slave mode.

Table continues on the next page...