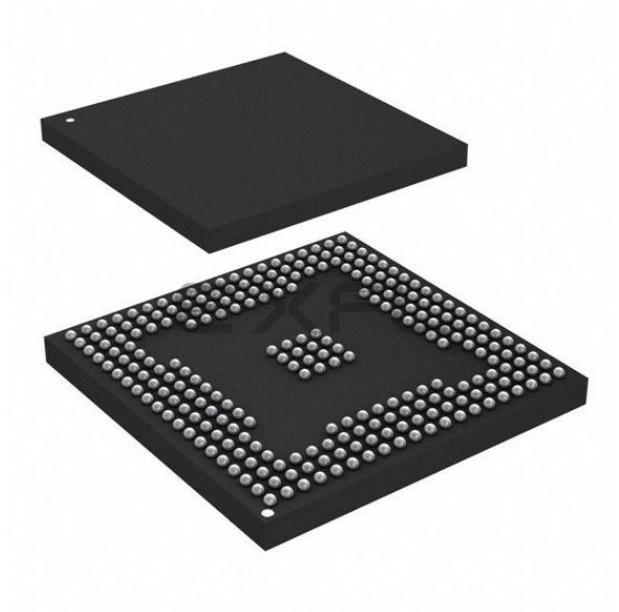

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Tri-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	-
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 12b SAR, 16b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	252-LFBGA
Supplier Device Package	252-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5746rk1mmt5r

1.1 Block diagram

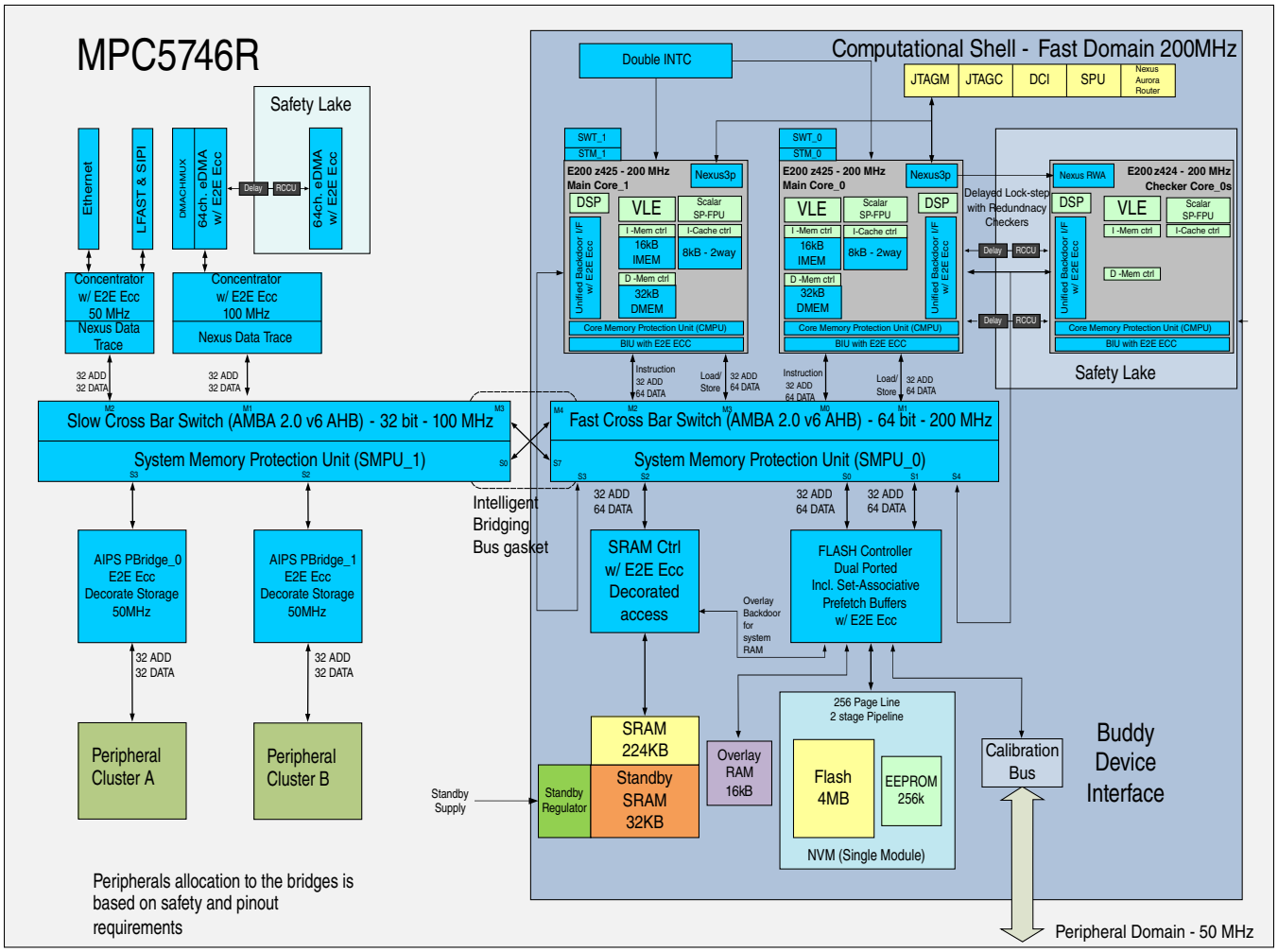

Figure 1. Core block diagram

3 Absolute maximum ratings

Functional operating conditions are given in the DC electrical specifications. Absolute maximum voltages are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond listed maxima may affect device reliability or cause permanent damage to the device.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
Cycle	Lifetime power cycles	—		1000k	—
V_{DD_LV}	1.2 V core supply voltage [2, 3, 4]	—	–0.3	1.5	V
$V_{DD\_LV\_BD}$	Emulation module voltage[2, 3, 4]	—	–0.3	1.5	V
$V_{DD\_HV\_IO\_MAIN}$	I/O supply voltage[5]	—	–0.3	6.0	V
$V_{DD\_HV\_IO\_JTAG}$	Crystal oscillator and JTAG supply	Reference to V_{SS}	–0.3	6.0	V
$V_{DD\_HV\_IO\_FEC}$	FEC supply voltage	Not using Ethernet Reference to V_{SS}	–0.3	6.0	V
$V_{DD\_HV\_IO\_MSC}$	MSC supply voltage	Reference to V_{SS}	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	Power Management Controller supply voltage [6]	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$	Decoupling pin for flash regulator[6]	—	–0.3	—	V
V_{DDSTBY}	RAM standby supply voltage[6]	—	–0.3	6.0	V
$V_{SS\_HV\_ADV\_SD}$	S/D ADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{SS\_HV\_ADV\_SAR}$	SAR ADC ground voltage	Reference to V_{SS}	–0.3	0.3	V
$V_{DD\_HV\_ADV\_SAR}$	SAR ADC supply voltage	Reference to $V_{SS\_HV\_ADV\_SAR}$	–0.3	6.0	V
$V_{DD\_HV\_ADV\_SD}$	S/D ADC supply voltage	Reference to $V_{SS\_HV\_ADV\_SD}$	–0.3	6.0	V
$V_{SS\_HV\_ADR\_SD}$	S/D ADC ground reference	Reference to V_{SS}	–0.3	0.3	V
$V_{SS\_HV\_ADR\_SAR}$	SAR ADC ground reference	Reference to V_{SS}	–0.3	0.3	V
$V_{DD\_HV\_ADR\_SAR}$	SAR ADC alternate reference	Reference to $V_{SS\_HV\_ADR\_SAR}$	–0.3	6.0	V
$V_{DD\_HV\_ADR\_SD}$	S/D ADC alternate reference	Reference to $V_{SS\_HV\_ADR\_SD}$	–0.3	6.0	V
$V_{DD\_LV\_BD}$ - V_{DD_LV}	Emulation module supply differential to 1.2 V core supply	—	–0.3	1.5	V
$V_{SS} – V_{SS\_HV\_ADR\_SAR}$	$V_{SS\_HV\_ADR\_SAR}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADR\_SD}$	$V_{SS\_HV\_ADR\_SD}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADV\_SAR}$	$V_{SS\_HV\_ADV\_SAR}$ differential voltage	—	–0.3	0.3	V
$V_{SS} – V_{SS\_HV\_ADV\_SD}$	$V_{SS\_HV\_ADV\_SD}$ differential voltage	—	–0.3	0.3	V
V_{IN}	I/O input voltage range[7]	—	–0.3	6.0	V
		Relative to $V_{SS\_HV\_IO}$, [8, 9]	–0.3	—	
		Relative to $V_{DD\_HV\_IO}$[8, 9]	—	0.3	
I_{INJD}	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA

Table continues on the next page...

Table 1. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions[1]	Value		Unit
			Min	Max	
I_{INJA}	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXSEG}[10, 11]	Maximum current per I/O segment	—	–120	120	mA
T_{STG}	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	yrs
T_{SDR}	Maximum solder temperature[12] Pb-free package	—	—	260	°C
MSL	Moisture sensitivity level[13]	—	—	3	—

1. Voltage is referenced to V_{SS} unless otherwise noted.
2. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in note -1 and note -1.
3. Allowed 1.375 – 1.45 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in note -1.
4. 1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J = 150 °C.
5. Allowed 5.5 – 6.0 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time at or below 5.0 V +10%.
6. Allowed 3.6 – 4.5 V for 10 hours cumulative time at maximum T_J = 150 °C, remaining time at or below 3.3 V +10%. This is an internally regulated supply. Values given are for reference only.
7. The maximum input voltage on an I/O pin tracks with the associated I/P supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
8. Relative value can be exceeded, if design measures are taken to ensure injection current limitation (parameters I_{INJD} and I_{INJA}).
9. $V_{DD\_HV\_IO}$/$V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FEC}$, $V_{DD\_HV\_IO\_MSC}$.
10. Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.
11. The average current values given in the "I/O pad current specifications" section should be used to calculate total I/O segment current.
12. Solder profile per IPC/JEDEC J-STD-020D.
13. Moisture sensitivity per JEDEC test method A112.

4 Electromagnetic Compatibility (EMC)

EMC measurements to IC-level IEC standards are available from Freescale on request.

5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

7 DC electrical specifications

The following table describes the DC electrical specifications.

Table 5. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD_LV}	Maximum operating current on the V_{DD_LV} supply [1]	MPC5746R/ MPC5745R	—	—	700	mA
		MPC5743R/ MPC5742R	—	—	610	
$I_{DD\_LV\_PE}$	Operating current on the V_{DD_LV} supply for flash program/erase	—	—	—	40	mA
$I_{DD\_HV\_PMC}$	Operating current on the $V_{DD\_HV\_PMC}$ supply[2]	Flash read	—	—	40	mA
		Flash P/E	—	—	70	
		PMC only	—	—	35	
	Operating current on the $V_{DD\_HV\_PMC}$ supply (internal core reg bypassed)	Flash read	—	—	10	mA
		Flash P/E	—	—	40	
$I_{VRCCTRL}$	Core regulator DC current output on VRC_CTRL pin	—	—	—	25	mA
I_{DDSTBY_ON}	32 KB RAM Standby Leakage Current (standby regulator on, RAM not operational)[3, 4, 5]	V_{DDSTBY} @1.3 V to 5.9 V, T_J = 150 °C	—	—	575	µA
		V_{DDSTBY} @1.3 V to 5.9 V, T_A = 40 °C	—	—	55	
		V_{DDSTBY} @1.3 V to 5.9 V, T_A = 85 °C	—	—	65	
I_{DDSTBY_REG}	32 KB RAM Standby Regulator Current [6]	V_{DDSTBY} @1.2 V to 5.9 V, Tj = 150 °C	—	—	50	µA
$I_{DD\_LV\_BD}$	BD Debug/Emulation low voltage supply operating current[7]	T_J = 150 °C $V_{DD\_LV\_BD}$ = 1.32 V	—	—	250	mA
$I_{DD\_HV\_IO\_BD}$	Debug/Emulation high voltage supply operating current (Aurora + JTAG/ LFAST)	T_J = 150 °C	—	—	130	mA
I_{BG}	Bandgap reference current consumption		—	—	600	µA
$I_{DD\_BD\_STBY}$	BD Debug/Emulation low voltage supply standby current	T_J = 150 °C $V_{DD\_LV\_BD}$ = 1.32 V	—	—	120	mA
I_{VDDA}	VDDA supply current		—	16	25	mA

1. Value is derived from a typical application at 200MHz, Core 0 Data and Instruction Cache On, Core 1 in Lockstep mode, typical usage for SARADC, SDADC, DMA, eTPU, eMIOS, CAN, MSC, SPI, SENT, PIT, and Flash reads.

Table 9. GPIO pad output buffer electrical characteristics (continued)

Symbol	Parameter	Conditions		Value [1], [2]			Unit
				Min	Typ	Max	
		MSCR[OERC] = 00, IOL = 6mA					
		3.0V < VDD_HV_IO < 3.6V MSCR[OERC] = 11, IOL = 24mA MSCR[OERC] = 10, IOL = 12mA MSCR[OERC] = 01, IOL = 9mA MSCR[OERC] = 00, IOL = 6mA		—	—	0.2 * VDD_HV_IO	
tR_F	GPIO pad output transition time (rise/fall)	MSCR[OERC] = 11	CL = 25pF	—	—	1.5	ns
			CL = 50pF	—	—	3	
		MSCR[OERC] = 10	CL = 50pF	—	—	6.5	
		MSCR[OERC] = 01	CL = 50pF	—	—	25	
		MSCR[OERC] = 00	CL = 50pF	—	—	40	
tPD	GPIO pad output propagation delay time	MSCR[OERC] = 11	CL = 25pF	—	—	6	ns
			CL = 50pF	—	—	7.5	
		MSCR[OERC] = 10	CL = 50pF	—	—	11.5	
		MSCR[OERC] = 01	CL = 50pF	—	—	45	
		MSCR[OERC] = 00	CL = 50pF	—	—	75	
$\lvert t_{SKEW\_W} \rvert$	Difference between rise and fall time	-		—	—	10	%

1. All GPIO pad output specifications are valid for 3.0V < VDD_HV_IO < 5.5V, except where explicitly stated.
2. All values need to be confirmed during device validation.

8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a VDD_HV_IO/VSS_HV_IO supply pair.

The following tables provides I/O consumption figures.

Table 10. I/O current consumption at VDD_HV_IO = 3.6 V

Cell	VDD_HV_IO (V)	Load (pF)	Period1 (ns)	MSCR[OERC]	Idde AVG (mA)	Idde RMS (mA)
pad_sr_hv	3.63	25	12	11	13	37
		50	15		16	36
		200	39		20	44
		25	16	10	8	20
		50	23		9	21
		200	66		12	37
		50	90	01	1.4	4

Table continues on the next page...

2. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.25V (+/-5%) with frequency below PLL bandwidth (40 KHz) will be filtered.

Table 14. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.762	—	200	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
$\lvert\Delta_{PLL1PHI0SPJ}\rvert$	PLL1_PHI0 single period peak to peak jitter	$f_{PLL1PHI0}$ = 200 MHz, 6-sigma pk-pk	—	—	500[2]	ps
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator is used in functional mode.
2. 1.25V +/-5%, application noise below 40kHz at V_{DD_LV} pin - no frequency modulation

All oscillator specifications are valid for $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V to 5.5 V.

Table 15. XOSC External Oscillator electrical specifications

Symbol	Parameter	Conditions		Value		Unit
				Min	Max	
f_{XTAL}	Crystal Frequency Range[1]	—		4	8	MHz
		—		>8	20	
		16MHz < freq < 40MHz (at present, freq = 20M and 40M have been validated, but still needs to be carried out for freq = 16MHz)		>20	40	
t_{cst}	Crystal start-up time[2, 3]	T_J = 150 °C, 20 MHz ≤ f ≤ 40 MHz		—	5	ms
t_{rec}	Crystal recovery time[4]	—		—	0.5	ms
V_{IHEXT}	EXTAL input high voltage[5] (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (External Reference)	V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[6]	BGA		4.75	5.25	pF
		QFP		5.25	5.75	
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[6]	BGA		4.75	5.25	pF
		QFP		5.25	5.75	
g_m	Oscillator Transconductance	T_J = -40 °C to 150 °C	f_{XTAL} ≤ 8 MHz	3	13	mA/V
			f_{XTAL} ≤ 20 MHz	9	35	

Table continues on the next page...

Table 16. Selectable load capacitance (continued)

load_cap_sel[4:0] from DCF record	Capacitance on EXTAL (C_{EXTAL})/XTAL (C_{XTAL}) [1, 2] (pF)
01111	15.0
10000-11111	N/A

1. Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.
2. Values in this table do not include the internal stray capacitances C_{xtal}/C_{extal}.

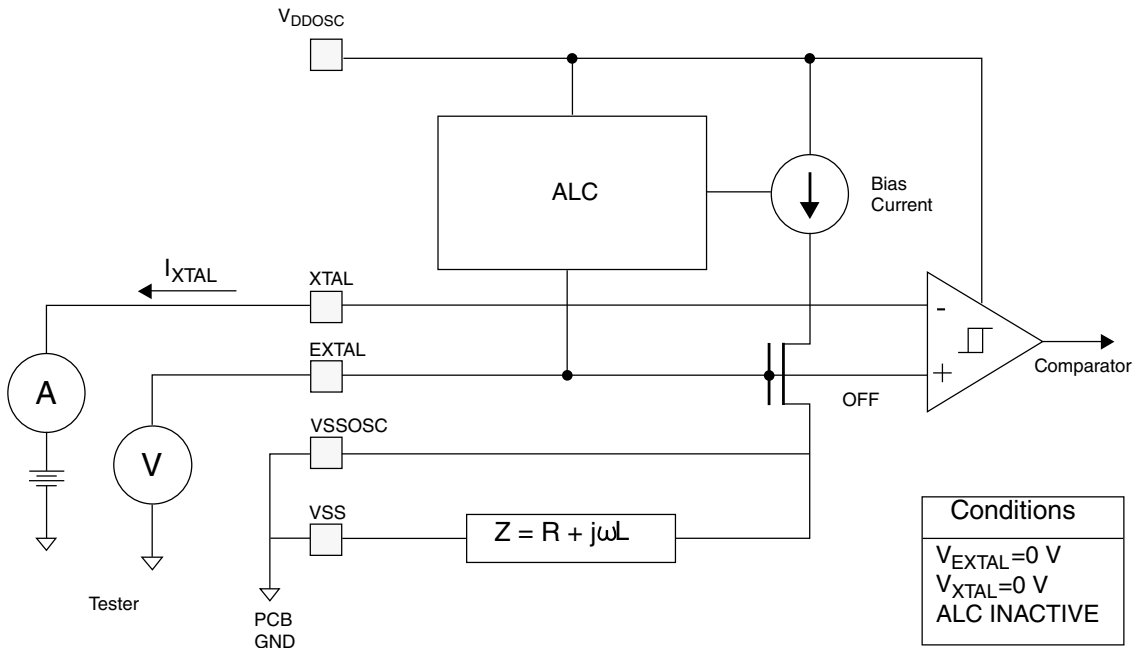

Figure 9. Test circuit

Table 17. Internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRCOSC target frequency	—	—	16	—	MHz
δf_{var_noT}	IRC frequency variation without temperature compensation	T < 150 °C	–8	—	8	%
δf_{var_T}	IRC frequency variation with temperature compensation	T < 150 °C	–3	—	3	%
δf_{var_SW}	IRC software trimming accuracy	Trimming temperature	–1	—	1	%
δf_{TRIM}	IRC software trimming step	—	—	+40/-48	—	kHz
T_{start_noT}	Startup time to reach within fvar_noT	Factory trimming already applied	—	—	5	µs
T_{start_T}	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
		GAIN = 4 T_J < 150 °C				
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	80	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 16 T_J < 150 °C	77	—	—	
THD_{SE150}	Total Harmonic Distortion in single ended mode 150 ksps output rate	4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 1 T_J < 150 °C	68	—	—	dB
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 2 T_J < 150 °C	68	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 4 T_J < 150 °C	68	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_SD}$ = $V_{DD\_HV\_ADV\_SD}$ GAIN = 8 T_J < 150 °C	68	—	—	
		4.5 < $V_{DD\_HV\_ADV\_SD}$ < 5.5[7] $V_{DD\_HV\_ADR\_DS}$ = $V^{DD\_HV\_ADV\_SD}$ G_{AIN} = 16 T_J < 150 °C	68	—	—	

Table continues on the next page...

Table 20. SDn ADC electrical specification (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_{S_D}	S/D ADC sampling capacitance after sampling switch[14]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
		GAIN = 16	—	—	600	fF
I_{BIAS}	Bias consumption	At least 1 ADCD enabled	—	—	3.5	mA
I_{ADV_D}	ADCD supply consumption	ADCD enabled	—	2.5	8	mA
ΣI_{ADR_D}	Reference current for one SDADC	ADCD enabled	—	10	50	µA

1. For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be 'clipped'.
2. VINP is the input voltage applied to the positive terminal of the SD ADC.
3. VINM is the input voltage applied to the negative terminal of the SD ADC.
4. For Gain=16, SDADC Resolution is 15 bit.
5. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.
6. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to $0.5*V_{DD\_HV\_ADR\_SD}$ for differential "differential mode" and single ended mode with negative input=$0.5*V_{DD\_HV\_ADR\_SD}$ ". Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0". Both Offset and Gain Calibration is guaranteed for +/-5% variation of $V_{DD\_HV\_ADR\_SD}$, +/-10% variation of $V_{DD\_HV\_ADV\_SD}$, +/-50 C temperature variation.
7. S/D ADC is functional in the range $3.6V < V_{DD\_HV\_ADV\_SD} < 4.5V$ and $3.0V < V_{DD\_HV\_ADR\_SD} < 4.5$ V, SNR paramter degrades by 9 dB.
8. Input impedance in differential mode $Z_{IN} = Z_{DIFF}$
9. Input impedance given at f_{ADCD_M} = 16 MHz. Impedance is inversely proportional to SDADC clock frequency. Z_{DIFF} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{DIFF}, Z_{CM} (f_{ADCD_M}) = (16 MHz / f_{ADCD_M}) * Z_{CM}.
10. Input impedance in single-ended mode $Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM})$
11. V_{INTCM} is the Common Mode input reference voltage for the SDADC. It has a nominal value of $(V_{RH\_SD} - V_{RL\_SD}) / 2$.
12. The ±1% passband ripple specification is equivalent to 20 * log10 (0.99) = 0.873 dB.
13. Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the following formula: REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator, and fPBRIDGEx_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing. Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.
14. This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

12 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

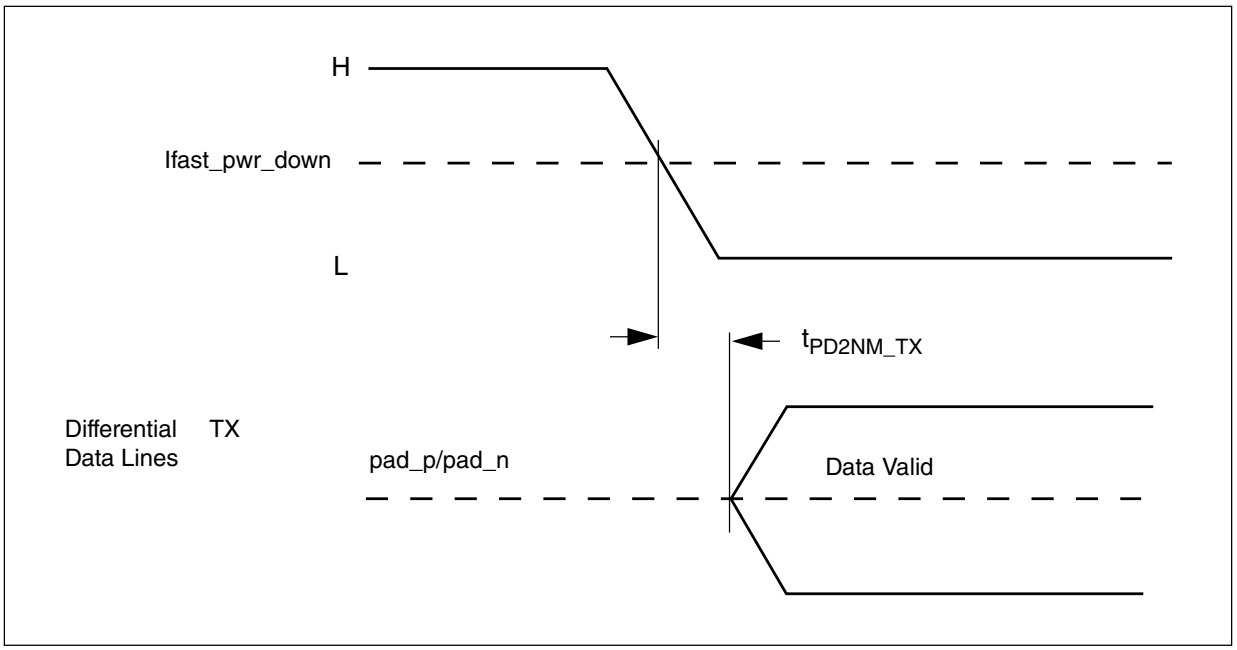

Figure 13. Power-down exit time

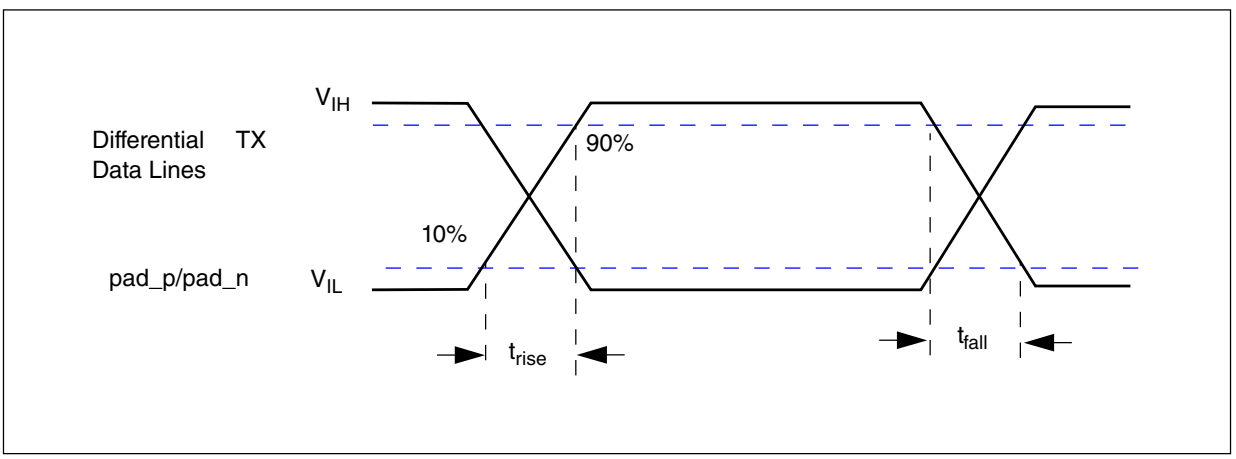

Figure 14. Rise/fall time

13.2 LFAST and MSC /DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

The LVDS pad electrical characteristics in this table apply to both the LFAST and High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.

All LVDS pad electrical characteristics are valid from -40 °C to 150 °C.

The following table describes the characteristics of the power transistors.

Table 27. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Maximum DC collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_C	Minimum voltage at transistor collector	2.5	V

16.1.2 Power management integration

In order to ensure correct functionality of the device, it is recommended to follow the integration scheme shown below.

5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

17.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

17.3 Flash memory module life specifications

Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years

Table continues on the next page...

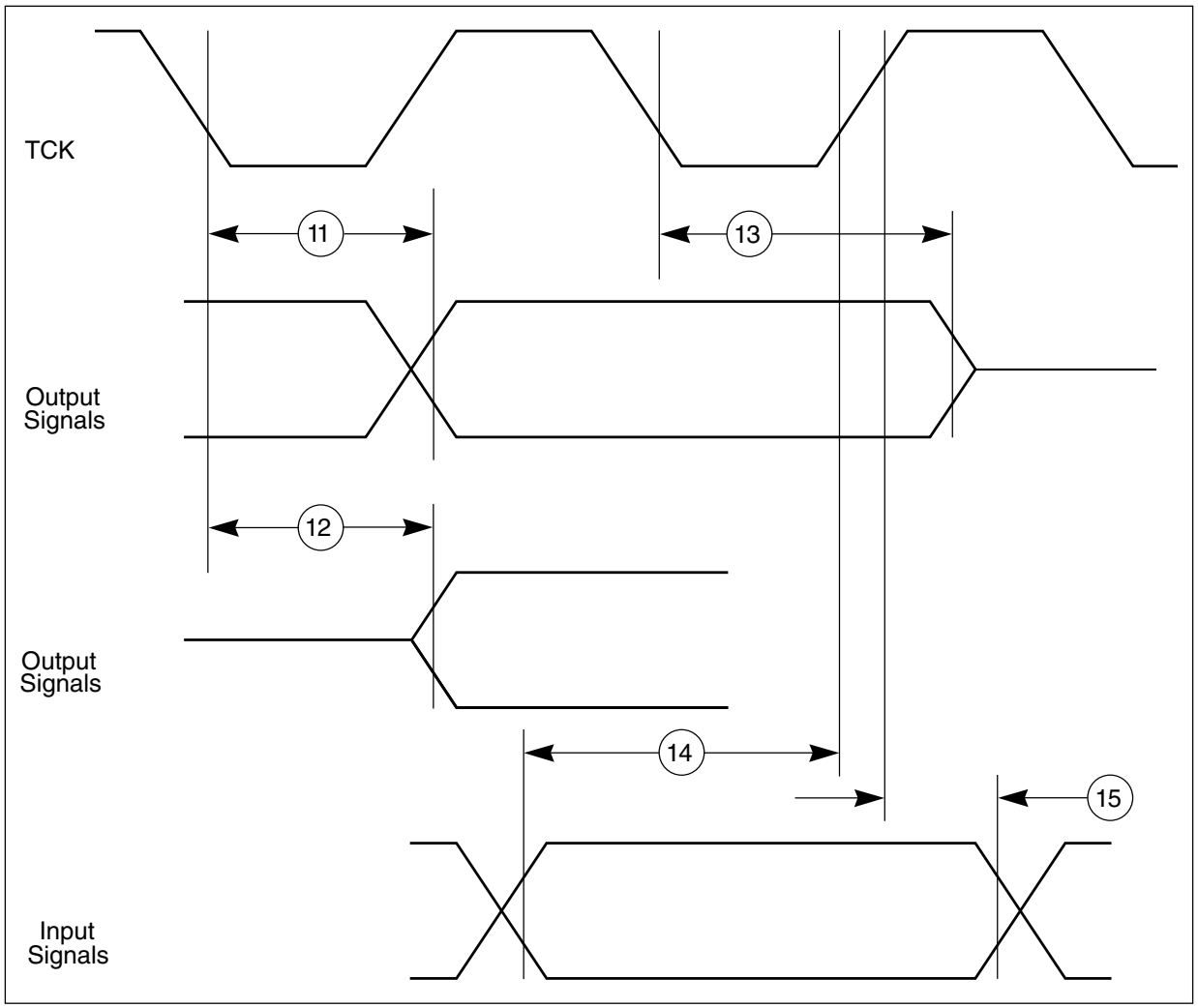

Figure 25. JTAG boundary scan timing

18.1.2 Nexus interface timing

Nexus timing specified for the whole V_{DD_LV} and $V_{DD\_HV\_IO}$ dynamic, $T_A = T_L$ to T_H, and maximum loading per pad type as specified in the I/O section of the data sheet.

Table 36. Nexus debug port timing

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{EVTIPW}	$\overline{EVTI}$ Pulse Width	4	—	t_{CYC}, [1]
2	t_{EVTOPW}	$\overline{EVTO}$ Pulse Width	40	—	ns
3	t_{TCYC}	TCK cycle time	4[2, 3]	—	t_{CYC}[1]
4	t_{TCYC}	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	40[5]	—	ns

Table continues on the next page...

1. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2. Maximum usable frequency does not take into account external device propagation delay.

18.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

The values presented in these sections are target values. A complete performance characterization of the pads (in all configuration combinations) is required before the final specifications can be released.

18.2.1.1 DSPI CMOS master mode – classic timing

All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

NOTE

In Table 40, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 40. DSPI CMOS master classic timing (full duplex and output only) - MTFE = 0, CPHA = 0 or 1

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive[2]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	SCK drive strength				
			Very strong	25 pF	33.0	—	ns
			Strong	50 pF	80.0	—	
			Medium	50 pF	200.0	—	
2	t_{CSC}	PCS to SCK delay	SCK and PCS drive strength				
			Very strong	25 pF	(N^3 x t_{SYS}, 4) - 16	—	ns
			Strong	50 pF	(N^3 x t_{SYS}, 4) - 16	—	
			Medium	50 pF	(N^3 x t_{SYS}, 4) - 16	—	
			PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N^3 x t_{SYS}, 4) - 29	—	
3	t_{ASC}	After SCK delay	SCK and PCS drive strength				
			Very strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}4) - 35	—	ns
			Strong	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, 4) - 35	—	
			Medium	PCS = 0 pF SCK = 50 pF	(M^5 x t_{SYS}, 4) - 35	—	
			PCS medium and SCK strong	PCS = 0 pF	(M^5 x t_{SYS}, 4) - 35	—	

Table continues on the next page...

Table 42. DSPI LVDS master timing - full duplex - modified transfer format (MTFE = 1), CPHA = 0 or 1 (continued)

#	Symbol	Characteristic	Condition		Value[1]		Unit
			Pad drive	Load	Min	Max	
		SIN hold time from SCK CPHA = 0[6]	SCK drive strength				
			LVDS	0 pF differential	-1 + (P[7] x t_{SYS}, [3])	—	ns
		SIN hold time from SCK CPHA = 1[6]	SCK drive strength				
			LVDS	0 pF differential	-1	—	ns
9	t_{SUO}	SOUT data valid time (after SCK edge)					
		SOUT data valid time from SCK CPHA = 0[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	—	7.0 + t_{SYS}[3]	ns
		SOUT data valid time from SCK CPHA = 1[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	SOUT data hold time (after SCK edge)					
		SOUT data hold time after SCK CPHA = 0[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	-7.5 + t_{SYS}[3]	—	ns
		SOUT data hold time after SCK CPHA = 1[8]	SOUT and SCK drive strength				
			LVDS	15 pF to 25 pF differential	-7.5	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
3. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
4. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
6. Input timing assumes an input slew rate of 1 ns (10% - 90%) and LVDS differential voltage = ±100 mV.
7. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.
8. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

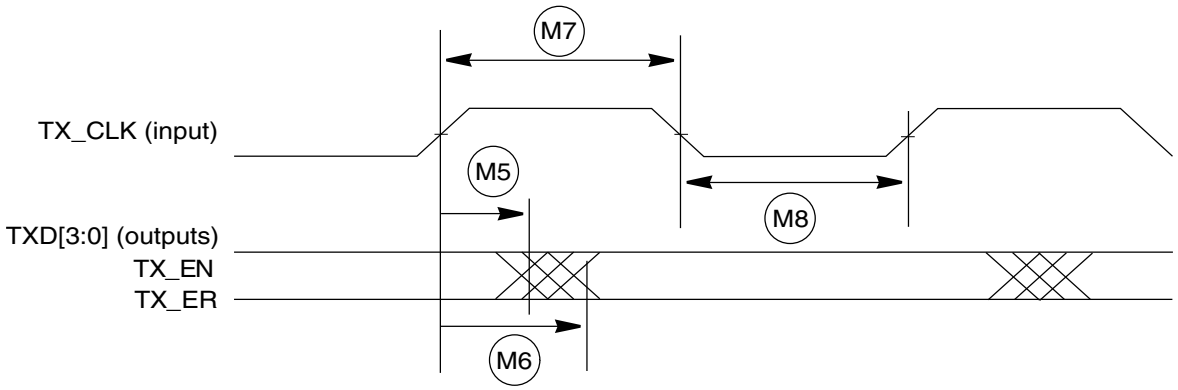

Figure 42. MII-lite transmit signal timing diagram

18.3.3 MII-lite async inputs signal timing (CRS and COL)

Table 48. MII-lite async inputs signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
M9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 43. MII-lite async inputs timing diagram

18.3.4 MII-lite serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

NOTE

All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

Table 51. RMII receive signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
R1	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	REF_CLK pulse width low	35%	65%	REF_CLK period

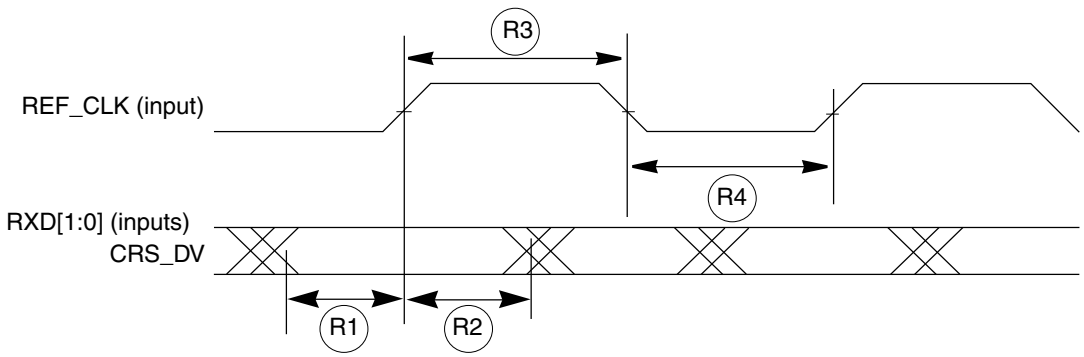

Figure 46. RMII receive signal timing diagram

18.3.7 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. This options allows the use of non-compliant RMII PHYs.

All timing specifications are referenced from REF_CLK = 1.4 V to the valid output levels.

Table 52. RMII transmit signal timing

Spec	Characteristic	Value		Unit
		Min	Max	
R5	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	REF_CLK pulse width low	35%	65%	REF_CLK period

Table 57. Thermal characteristics for the 176-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	37.8	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	28.2	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	21.0	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	7.8	°C/W
Junction to Package Top[6]	Natural Convection	ψ_{JT}	0.3	°C/W
Junction to Package Lead[7]	Natural Convection	ψ_{JB}	13.0	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Table 58. Thermal characteristics for the 252-pin MAPBGA package with full solder balls

Rating	Conditions	Symbol	Value	Unit
Junction to Ambient Natural Convection [1, 2]	Single layer board (1s)	$R_{\theta JA}$	43.0	°C/W
Junction to Ambient Natural Convection[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	26.5	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	33.2	°C/W
Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	22.2	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	12.5	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	6.3	°C/W
Junction to Package Top[6]	Natural Convection	ψ_{JT}	0.3	°C/W
Junction to Package Lead[7]	Natural Convection	ψ_{JB}	8.7	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 61. Revision history (continued)

Revision	Date	Description of changes
		• Removed parenthetical phrase from table title. • Made overall updates to spec values. • Removed footnote 7. In section Flash memory Array Integrity and Margin Read specifications, Table 31 : • Removed parenthetical phrase from table title. • Made overall updates to spec values. In section Flash memory module life specifications, Table 32, removed parenthetical phrase from table title. In section Flash memory AC timing specifications, Table 33, removed parenthetical phrase from table title. Added section Flash read wait state and address pipeline control settings. In section Power management integration, Table 28, changed the footnotes for t_{TCYC} Min values to have the same footnote number as they were identical. In section DSPI timing with CMOS and LVDS, Table 39, LVDS (Master mode) specification: changed Max usuable frequency to 40 MHz (was 33 MHz). In section DSPI CMOS master mode – classic timing : • Added NOTE. • In Table 40, changed PCS strobe timing values. In section DSPI CMOS master mode – modified timing : • Added NOTE. • In Table 41, changed PCS strobe timing values. In section DSPI LVDS master mode – modified timing, Table 42, changed significant digits for some values. In section DSPI master mode – output only : • Modified format paragraphs leading the tables. Removed NOTE. • In Table 43, changed the t_{CSV} strong drive value and t_{HO} LVDS value. • In Table 44, changed significant digits for some values. In section FEC timing, corrected the title of MII-lite and RMII serial management channel timing subsections. In section MII-lite transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK), Table 47, modified footnote for output parameters. In section RMII serial management channel timing (MDIO and MDC), added Note on reference for timing specifications. In section RMII transmit signal timing (TXD[1:0], TX_EN), Table 52, modified R6 max value. In section UART timings, Table 53, removed 100 MHz specification. "Package drawings" section renamed to Obtaining package dimensions, with package drawing document numbers to search at the Freescale website. Drawings removed from this document. In section Thermal characteristics : • Added table for 144 LQFP. • Moved table for 176 LQFP before 252 MAPBGA and updated table. • Replaced table for 252 MAPBGA with two separate tables for package with full solder balls and package with 16 removed balls. In section Ordering information, replaced the table.
3	09/2015	On the cover page:

Table continues on the next page...

Table 61. Revision history (continued)

Revision	Date	Description of changes

		• Added NOTE "For spec complaint operation, do not expose clock sources, including crystal oscillator, IRC, PLL0, and PLL1 on the CLKOUT pads while the SAR ADC is converting."
		• Added NOTE: "The ADC performance specifications are not guaranteed if two or more ADCs simultaneously sample the same shared channel".
		
		In section S/D ADC :
		• In Table 20 :
		  • For $THD_{DIFF333}$ GAIN = 16, updated Min value.
		  • For I_{ADV_D}, updated Max value.
		
		In section LFAST and MSC /DSPI LVDS interface electrical characteristics :
		• After table Table 24 added NOTE "For optimum LVDS performance, it is recommended to set the neighbouring GPIO pads to use Weak Drive".
		
		In section Device voltage monitoring :
		• In Table 29 :
		  • For LVD_core_hot, LVD_HV, and LVD_IO specs, removed the untrimmed Rising voltage and Falling voltage rows.
		  • For LVD_core_hot, changed Mask Opt. value to "No".
		
		In section Regulator example for the 2SCR574d transistor, figure "Regulator example", changed “5V or Vcollector” to “3.3V or Vcollector”.
		
		In section DSPI CMOS master mode – classic timing, Table 40 :
		• Changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		• In tSUI and tHI specs' footnote, removed reference to "Automotive" thresholds.
		
		In section DSPI CMOS master mode – modified timing, Table 41 :
		• Changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		• In tSUI and tHI specs' footnote, removed reference to "Automotive" thresholds.
		
		In section DSPI master mode – output only, Table 44, changed tSDC spec's Condition SCK drive strength from "0 pF" to "0 to 50 pF".
		
		Added section eMIOS timing.
		
		In section Ordering information, Table 60 :
		• Updated Part Numbers.
		• Updated Emulation device footnote.

4	03/2016	In section Block diagram, Figure 2 : • "DECIM" changed to "DECFILTER". • "SIPI" changed to "Zipwire". • I/O lines added to Zipwire, SIUL2, REACM, eTPU, eMIOS, IGF, and XOSC. In section Absolute maximum ratings table "Absolute maximum ratings", removed I_{IOMAX} spec and added I_{MAXSEG} spec. In section Operating conditions table "Device operating conditions": • For the FEC I/O supply voltage, MSC I/O supply voltage, and JTAG I/O supply voltage specs, removed the LVD enabled/disabled distinction. • Added footnote to I_{MAXSEG}. In section I/O pad current specifications : • Modified the descriptions in the two paragraphs after the tables. • Removed the third paragraph after the tables and the first Note. Added section DSPI CMOS slave mode.

Table continues on the next page...