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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN Exposed Pad
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl02z8vfg4r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ordering Information

Part Number	Mer	Maximum number of I\O's	
	Flash (KB)	SRAM (KB)	
MKL02Z8VFG4	8	1	14
MKL02Z16VFG4	16	2	14
MKL02Z32VFG4	32	4	14
MKL02Z16VFK4	16	2	22
MKL02Z32VFK4	32	4	22
MKL02Z16VFM4	16	2	28
MKL02Z32VFM4	32	4	28

Related Resources

Туре	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL0XPB ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL02P32M48SF0RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL02P32M48SF0 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN33H ²
Package	Package dimensions are provided in package drawings.	QFN 16-pin: 98ASA00525D ¹
drawing		QFN 24-pin: 98ASA00474D ¹
		QFN 32-pin: 98ASA00473D ¹

- 1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
- 2. To find the associated resource, go to http://www.freescale.com and perform a search using this term with the "x" replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{LVW1H}	 Level 1 falling (LVWV = 00) 	2.62	2.70	2.78	V	
V _{LVW2H}	 Level 2 falling (LVWV = 01) 	2.72	2.80	2.88	V	
V _{LVW3H}	 Level 3 falling (LVWV = 10) 	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	v	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range		±60		mV	_
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	_
	Low-voltage warning thresholds — low range					1
V _{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	v	
V _{LVW2L}	 Level 2 falling (LVWV = 01) 	1.84	1.90	1.96	v	
V _{LVW3L}	 Level 3 falling (LVWV = 10) 	1.94	2.00	2.06	v	
V _{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	v	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	_	±40	_	mV	_
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — Normal drive pad (except RESET)				1, 2
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -5 mA	V _{DD} – 0.5	—	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OH} = -2.5 mA	V _{DD} – 0.5	_	V	
V _{OH}	Output high voltage — High drive pad (except RESET)				1, 2
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -20 mA	V _{DD} – 0.5	—	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -10 \text{ mA}$	V _{DD} – 0.5	_	V	
I _{OHT}	Output high current total for all ports	—	100	mA	—
V _{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 5 mA	_	0.5	v	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 2.5 \text{ mA}$	_	0.5	V	



Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — High drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 20 mA	_	0.5	v	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 10 \text{ mA}$	—	0.5	V	
I _{OLT}	Output low current total for all ports	_	100	mA	—
I _{IN}	Input leakage current (per pin) for full temperature range	_	1	μA	3
I _{IN}	Input leakage current (per pin) at 25 °C	_	0.025	μA	3
I _{IN}	Input leakage current (total all pins) for full temperature range	_	41	μA	3
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	—
R _{PU}	Internal pullup resistors	20	50	kΩ	4

Table 7. Voltage and current operating behaviors (continued)

1. PTA12, PTA13, PTB0 and PTB1 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.

2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.

3. Measured at V_{DD} = 3.6 V

4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx \rightarrow RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8.	Power mode	transition	operating	behaviors
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Symbol	Description	Min.	Тур.	Max.	Unit	
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	_		300	μs	1
	• VLLS0 \rightarrow RUN	_	95	115	μs	

Table continues on the next page...

9



Symbol	Description	Temp.	Тур.	Max	Unit	Note
I _{DD_VLLS0}	I _{DD_VLLS0} Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	at 25 °C	0.12	0.23	μA	5
		at 50 °C	0.44	0.58	μA	
			1.21	1.55	μA	
		at 85 °C	3.01	3.57	μA	
		at 105 °C	7.34	8.89	μA	

Table 9. Power consumption operating behaviors (continued)

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.

2. MCG configured for FEI mode.

3. Incremental current consumption from peripheral activity is not included.

4. MCG configured for BLPI mode.

5. No brownout.

Table 10. Low power mode peripheral adders — typical value

Symbol	Description		Temperature (°C)				Unit		
			-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock Measured by entering STOP o with 4 MHz IRC enabled.	(IRC) adder. r VLPS mode	56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.		52	52	52	52	52	52	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock	VLLS1	440	490	540	560	570	580	nA
	adder by means of the	VLLS3	440	490	540	560	570	580	
	EREFSTEN] bits. Measured	VLPS	510	560	560	560	610	680	
	by entering all modes with the crystal enabled.	STOP	510	560	560	560	610	680	
ICMP	crystal enabled.CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	μA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA





Figure 3. Run mode supply current vs. core frequency



Peripheral operating requirements and behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200	_	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

 Table 19. Oscillator DC electrical specifications (continued)

- 1. V_{DD} =3.3 V, Temperature =25 °C
- 2. See crystal or resonator manufacturer's recommendation
- 3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
- 4. When low power mode is selected, R_F is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	_	40	kHz	
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)				ms	1, 2
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)				ms	

1. Proper PC board layout procedures must be followed to achieve specifications.

2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.



Peripheral operating requirements and behaviors

3.4.1.4 Reliability specifications Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes	
Program Flash							
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	_	years	_	
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	_	years	_	
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2	

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40 °C \leq T_i \leq 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.6.1.1 12-bit ADC operating conditions Table 25. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	3
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	3
V _{ADIN}	Input voltage		V _{REFL}	—	V _{REFH}	V	_
C _{ADIN}	Input capacitance	8-bit / 10-bit / 12-bit modes		4	5	pF	
R _{ADIN}	Input series resistance		_	2	5	kΩ	_



Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
R _{AS}	Analog source resistance (external)	12-bit modes f _{ADCK} < 4 MHz	_	_	5	kΩ	4
f _{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	_	18.0	MHz	5
C _{rate}	ADC conversion rate	 ≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time 	20.000	_	818.330	Ksps	6

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- For packages without dedicated VREFH and VREFL pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
- 4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.</p>
- 5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 6. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 7. ADC input impedance equivalency diagram



- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^{N}$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. ADC conversion clock < 3 MHz



Figure 8. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 27. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	—	3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	_	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	_	—	20	μA
V _{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V _{DD}	V
V _{AIO}	Analog input offset voltage	_	—	20	mV
V _H	Analog comparator hysteresis ¹				
	 CR0[HYSTCTR] = 00 	—	5	_	mV
	 CR0[HYSTCTR] = 01 	—	10	—	mV
	 CR0[HYSTCTR] = 10 	—	20	_	mV
	 CR0[HYSTCTR] = 11 	—	30	_	mV
V _{CMPOh}	Output high	V _{DD} – 0.5	—	—	V
V _{CMPOI}	Output low	_	_	0.5	V



Symbol	Description	Min.	Тур.	Max.	Unit
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	_	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	_	0.3	LSB

 Table 27. Comparator and 6-bit DAC electrical specifications (continued)

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} –0.6 V.

 Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.

^{3. 1} LSB = $V_{reference}/64$



Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)



Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

29

Num.	Symbol	Description	Min.	Max.	Unit	Note
4	t _{Lag}	Enable lag time	1	—	t _{periph}	—
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{periph} – 30	_	ns	_
6	t _{SU}	Data setup time (inputs)	3	—	ns	—
7	t _{HI}	Data hold time (inputs) 7		—	ns	—
8	t _a	Slave access time	23	t _{periph}	ns	3
9	t _{dis}	Slave MISO disable time	23	t _{periph}	ns	4
10	t _v	Data valid (after SPSCK edge)	—	25.7	ns	—
11	t _{HO}	Data hold time (outputs)	0	—	ns	—
12	t _{RI}	Rise time input	—	t _{periph} – 25	ns	—
	t _{FI}	Fall time input				
13	t _{RO}	Rise time output	_	25	ns	—
	t _{FO}	Fall time output				

Table 30. SPI slave mode timing on slew rate disabled pads (continued)

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).

2. $t_{periph} = 1/f_{periph}$

3. Time to data active from high-impedance state

4. Hold time to high-impedance state

Table 31. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f _{op}	Frequency of operation	0	f _{periph} /4	Hz	1
2	t _{SPSCK}	SPSCK period	4 x t _{periph}	—	ns	2
3	t _{Lead}	Enable lead time	1	—	t _{periph}	—
4	t _{Lag}	Enable lag time	1	—	t _{periph}	—
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{periph} – 30		ns	
6	t _{SU}	Data setup time (inputs)	2	_	ns	
7	t _{HI}	Data hold time (inputs)			ns	
8	t _a	Slave access time	—	t _{periph}	ns	3
9	t _{dis}	Slave MISO disable time	—	t _{periph}	ns	4
10	t _v	Data valid (after SPSCK edge)	—	122	ns	—
11	t _{HO}	Data hold time (outputs)	0	—	ns	—
12	t _{RI}	Rise time input	—	t _{periph} – 25	ns	—
	t _{FI}	Fall time input				
13	t _{RO}	Rise time output	_	36	ns	
	t _{FO}	Fall time output]			

1. For SPI0, f_{periph} is the bus clock (f_{\text{BUS}}).

2. $t_{periph} = 1/f_{periph}$

- 3. Time to data active from high-impedance state
- 4. Hold time to high-impedance state



Peripheral operating requirements and behaviors

Characteristic	Symbol	Standa	rd Mode	Fast	Mode	Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t _{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7	_	0.6	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	04	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ³ , ⁶	—	ns
Rise time of SDA and SCL signals	t _r	_	1000	20 +0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	_	300	20 +0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	_	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

3.8.2 Inter-Integrated Circuit Interface (I2C) timing Table 32. I2C timing

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V

The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves
acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL
lines.

- 3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
- 4. Input signal Slew = 10 ns and Output Load = 50 pF
- 5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- 6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU; DAT} \ge 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
- 7. C_b = total capacitance of the one bus line in pF.



Figure 15. Timing definition for fast and standard mode devices on the I²C bus





3.8.3 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin QFN	98ASA00525D
24-pin QFN	98ASA00474D
32-pin QFN	98ASA00473D

5 Pinout

5.1 KL02 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

PTB3 and PTB4 are true open drain pins. To use these pins as outputs, you must use an external pullup resistor to make them output correct values when using I2C, GPIO, and UART0.





32 QFN	24 QFN	16 QFN	Pin Name	Default	ALTO	ALT1	ALT2	ALT3
30	22	14	PTA0/ IRQ_0	SWD_CLK	ADC0_SE12/ CMP0_IN2	PTA0/ IRQ_0	TPM1_CH0	SWD_CLK
31	23	15	PTA1/ IRQ_1/ LPTMR0_ALT1	RESET_b		PTA1/ IRQ_1/ LPTMR0_ALT1	TPM_CLKIN0	RESET_b
32	24	16	PTA2	SWD_DIO		PTA2	CMP0_OUT	SWD_DIO

5.2 KL02 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see KL02 signal multiplexing and pin assignments.



Figure 16. KL02 32-pin QFN pinout diagram







Figure 18. KL02 16-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: PKL02 and MKL02

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.



8 Small package marking

In order to save space, small package devices use special marking on the chip.

Q FS FF (TP)

Table 34.	Small	package	marking
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Field	Description	Values
Q	Qualification status	 M = M P = P
FS	Kinetis family and CPU frequency	 (0)2T = KL02, 48 MHz of CPU
FF	Program flash memory size	 3 = 8 KB 4 = 16 KB 5 = 32 KB
ТР	Temperature range (°C) and package	 V = -40 to 105, 24 or 32 QFN blank = -40 to 105, 16 QFN

For example:

M2T4 = MKL02Z16VFG4

M02T4V = MKL02Z16VFK4

9 Terminology and guidelines

9.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

9.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V



9.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

9.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μΑ

9.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

9.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins		7	pF

9.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.





Typical value conditions 9.9

Typical values assume you meet the following conditions (or other conditions as specified):

Table 35. Typical value conditions

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	٥C
V _{DD}	3.3 V supply voltage	3.3	V

Revision history 10

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes	
2	05/2013	Public release.	
2.1	07/2013	Removed the specification on OSCERCLK (4 MHz external crystal) because KL02 does not support it.	
3	3/2014	Updated the front page and restructured the chapters	

Table 36. Revision history



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