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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	40
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151c3t6

MSB have a fixed value: 0x6.

3. The TS_Factory_CONV_V90 byte represents the LSB of the V_{90} 12-bit ADC1 conversion result. The MSB have a fixed value: 0x3.
4. Refer to *Table 8* for an overview of hardware register mapping, to *Table 7* for details on I/O port hardware registers, and to *Table 9* for information on CPU/SWIM/debug module controller registers.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1 Kbyte	0x00 0000	0x00 03FF
Flash program memory	8 Kbyte	0x00 8000	0x00 9FFF
	4 Kbyte	0x00 8000	0x00 8FFF

5.2 Register map

Table 6. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV	Value of the internal reference voltage measured during the factory phase	0xXX
0x00 4911	-	TS_Factory_CONV_V90	Value of the temperature sensor output voltage measured during the factory phase	0xXX

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 byte)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5317 to 0x00 533F	Reserved area (41 byte)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00

Table 12. Option byte description

Option byte No.	Option description
OPT0	**ROP[7:0]** Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L15x and STM8L16x reference manual (RM0031).
OPT1	**UBC[7:0]** Size of the user boot code area 0x00: UBC is not protected. 0x01: Page 0 is write protected. 0x02: Page 0 and 1 reserved for the UBC and write protected. It covers only the interrupt vectors. 0x03: Page 0 to 2 reserved for UBC and write protected. 0x7F to 0xFF - All 128 pages reserved for UBC and write protected. The protection of the memory area not protected by the UBC is enabled through the MASS keys. Refer to User boot code section in the STM8L15x and STM8L16x reference manual (RM0031).
OPT2	Reserved
OPT3	**IWDG_HW:** Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: Independent window watchdog off on Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW: Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT: Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	**HSECNT**: Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT: Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles Refer to *Table 31: LSE oscillator characteristics on page 74*.

Table 12. Option byte description (continued)

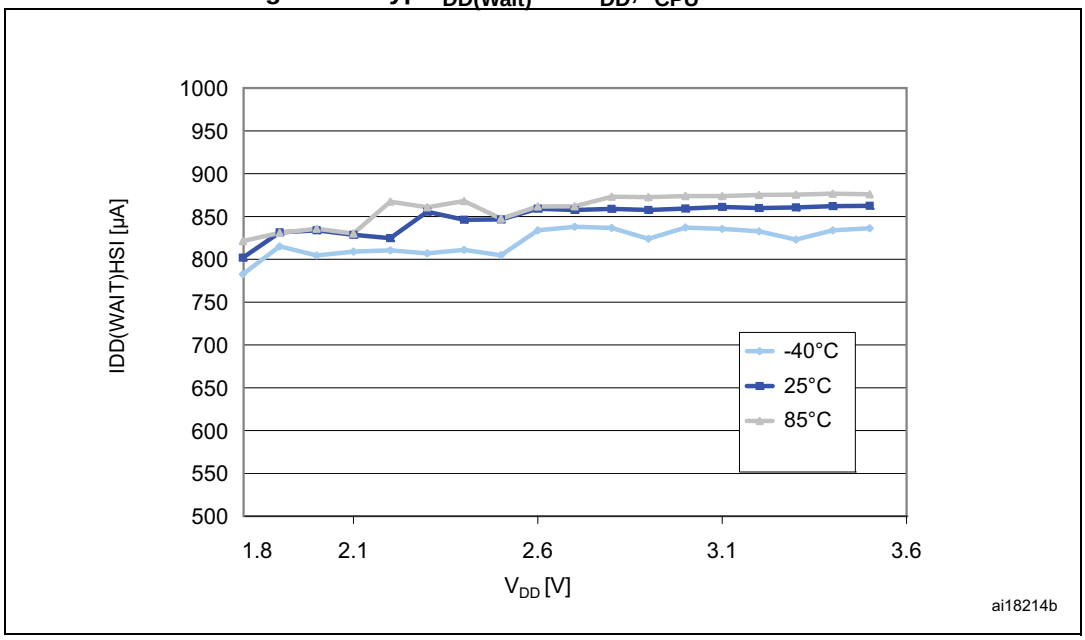
Option byte No.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 22* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

Table 19. Total current consumption in Run mode

Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55 °C	85 °C	105°C[2]	125 °C[2]	
$I_{DD(RUN)}$	Supply current in run mode[3]	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)[4]	f_{CPU} = 125 kHz	0.39	0.47	0.49	0.52	0.55	mA
				f_{CPU} = 1 MHz	0.48	0.56	0.58	0.61	0.65	
				f_{CPU} = 4 MHz	0.75	0.84	0.86	0.91	0.99	
				f_{CPU} = 8 MHz	1.10	1.20	1.25	1.31	1.40	
				f_{CPU} = 16 MHz	1.85	1.93	2.12[6]	2.29[6]	2.36[6]	
			HSE external clock ($f_{CPU}=f_{HSE}$)[5]	f_{CPU} = 125 kHz	0.05	0.06	0.09	0.11	0.12	
				f_{CPU} = 1 MHz	0.18	0.19	0.20	0.22	0.23	
				f_{CPU} = 4 MHz	0.55	0.62	0.64	0.71	0.77	
				f_{CPU} = 8 MHz	0.99	1.20	1.21	1.22	1.24	
				f_{CPU} = 16 MHz	1.90	2.22	2.23[6]	2.24[6]	2.28[6]	
			LSI RC osc. (typ. 38 kHz)	$f_{CPU} = f_{LSI}$	0.040	0.045	0.046	0.048	0.050	
			LSE external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.035	0.040	0.048[6]	0.050	0.062	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.[7]	f_{CPU} = 125 kHz	0.43	0.55	0.56	0.58	0.62	mA
				f_{CPU} = 1 MHz	0.60	0.77	0.80	0.82	0.87	
				f_{CPU} = 4 MHz	1.11	1.34	1.37	1.39	1.43	
				f_{CPU} = 8 MHz	1.90	2.20	2.23	2.31	2.40	
				f_{CPU} = 16 MHz	3.8	4.60	4.75	4.87	4.88	
			HSE external clock ($f_{CPU}=f_{HSE}$) [5]	f_{CPU} = 125 kHz	0.30	0.36	0.39	0.44	0.47	
				f_{CPU} = 1 MHz	0.40	0.50	0.52	0.55	0.56	
				f_{CPU} = 4 MHz	1.15	1.31	1.40	1.45	1.48	
				f_{CPU} = 8 MHz	2.17	2.33	2.44	2.56	2.77	
				f_{CPU} = 16 MHz	4.0	4.46	4.52	4.59	4.77	
			LSI RC osc.	$f_{CPU} = f_{LSI}$	0.110	0.123	0.130	0.140	0.150	
			LSE ext. clock (32.768 kHz)[8]	$f_{CPU} = f_{LSE}$	0.100	0.101	0.104	0.119	0.122	

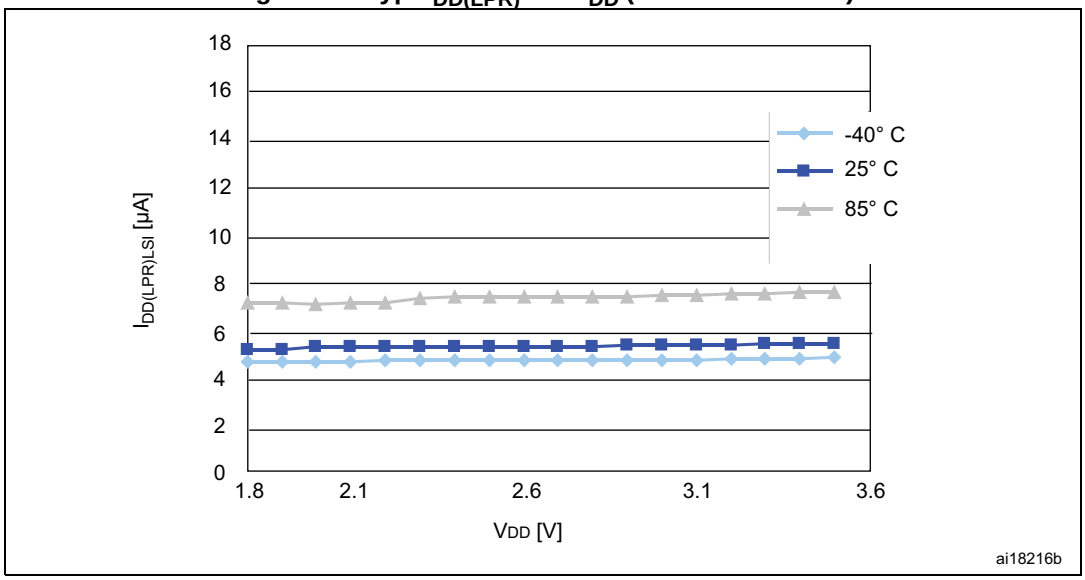
1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{SYSCLK}$
2. For devices with suffix 3
3. CPU executing typical data processing

Figure 13. Typ. $I_{DD(Wait)}$ vs. V_{DD}, f_{CPU} = 16 MHz [1)]



1. Typical current consumption measured with code executed from Flash memory.

Figure 14. Typ. $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source)



In the following table, data is based on characterization results, unless otherwise specified.

Table 25. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)(2)	Typ	Max	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	350	1400(3)	nA
		T_A = 55 °C	580	2000	
		T_A = 85 °C	1160	2800(3)	
		T_A = 105 °C	2560	6700(3)	
		T_A = 125 °C	4.4	13(3)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)	-	2.4	-	mA
$t_{WU\_HSI(Halt)}$(4)(5)	Wakeup time from Halt to Run mode (using HSI)	-	4.7	7	µs
$t_{WU\_LSI(Halt)}$ (4)(5)	Wakeup time from Halt mode to Run mode (using LSI)	-	150	-	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. T_A > 85 °C is valid only for devices with suffix 3 temperature range.
3. Tested in production.
4. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.
5. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.

Current consumption of on-chip peripherals

Table 26. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM2)}$	TIM2 supply current (1)		8	µA/MHz
$I_{DD(TIM3)}$	TIM3 supply current (1)		8	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		6	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		5	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		2	
$I_{DD(ALL)}$	Peripherals ON(3)		38	µA/MHz
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(COMP1)}$	Comparator 1 supply current(5)		0.160	µA
$I_{DD(COMP2)}$	Comparator 2 supply current(5)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (6)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (6)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM2, TIM3, TIM4, USART1, SPI1, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC1 in reset configuration and continuous ADC1 conversion.
5. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
6. Including supply current of internal reference voltage.

Figure 24. Typ. V_{OL} @ V_{DD} = 3.0 V (high sink ports)

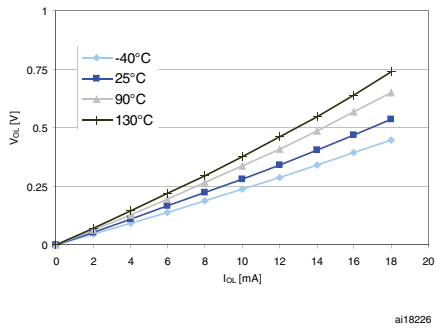


Figure 25. Typ. V_{OL} @ V_{DD} = 1.8 V (high sink ports)

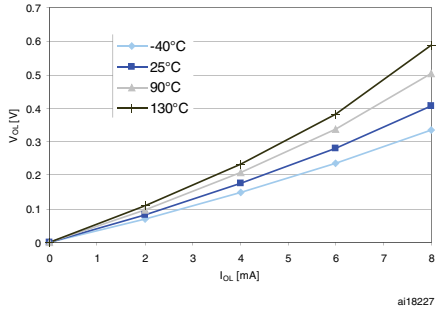


Figure 26. Typ. V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

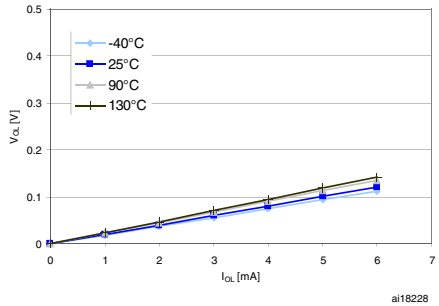


Figure 27. Typ. V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

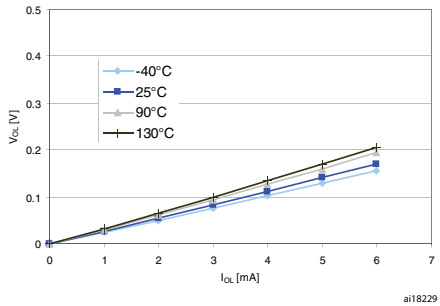


Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

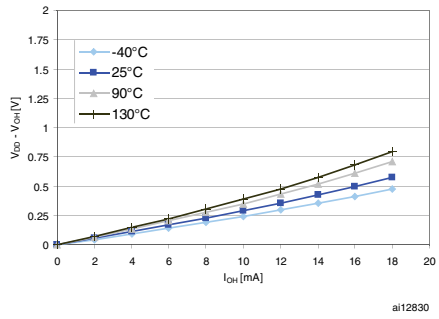
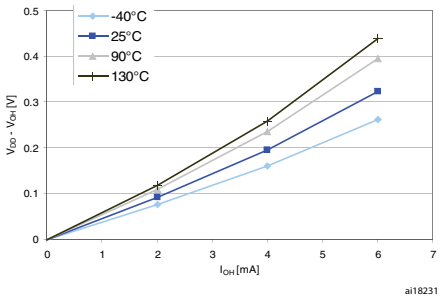


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



In the following table, data is guaranteed by design, not tested in production.

Table 47. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
T_A	Temperature range	-	-40	-	125	°C
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay in slow mode(2)	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay in fast mode(2)	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

9.3.12 12-bit ADC1 characteristics

In the following table, data is guaranteed by design, not tested in production.

Table 48. ADC1 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	2.4 V ≤ V_{DDA}≤ 3.6 V	2.4	-	V_{DDA}	V
		1.8 V ≤ V_{DDA}≤ 2.4 V	V_{DDA}			V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF+}	Current on the V_{REF+} input pin	-	-	400	700 (peak)(1)	µA
		-	-		450 (average)(1)	µA
V_{AIN}	Conversion voltage range	-	0(2)	-	V_{REF+}	V
T_A	Temperature range	-	-40	-	125	°C
R_{AIN}	External resistance on V_{AIN}	on PF0 fast channel	-	-	50(3)	kΩ
		on all other channels	-	-		
C_{ADC1}	Internal sample and hold capacitor	on PF0 fast channel	-	16	-	pF
		on all other channels	-		-	
f_{ADC1}	ADC1 sampling clock frequency	2.4 V≤ V_{DDA}≤ 3.6 V without zooming	0.320	-	16	MHz
		1.8 V≤ V_{DDA}≤ 2.4 V with zooming	0.320	-	8	MHz
f_{CONV}	12-bit conversion rate	V_{AIN} on PF0 fast channel	-	-	1(4)(5)	MHz
		V_{AIN} on all other channels	-	-	760(4)(5)	kHz
f_{TRIG}	External trigger frequency	-	-	-	t_{conv}	$1/f_{ADC1}$
t_{LAT}	External trigger latency	-	-	-	3.5	$1/f_{SYSCLK}$

In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 49. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC1} = 16 MHz	1	1.6	LSB
		f_{ADC1} = 8 MHz	1	1.6	
		f_{ADC1} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC1} = 16 MHz	1.2	2	
		f_{ADC1} = 8 MHz	1.2	1.8	
		f_{ADC1} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC1} = 16 MHz	2.2	3.0	
		f_{ADC1} = 8 MHz	1.8	2.5	
		f_{ADC1} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC1} = 16 MHz	1.5	2	LSB
		f_{ADC1} = 8 MHz	1	1.5	
		f_{ADC1} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC1} = 16 MHz	1	1.5	
		f_{ADC1} = 8 MHz			
		f_{ADC1} = 4 MHz			

Table 50. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 51. ADC1 accuracy with V_{DDA} = V_{REF}^+ = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 53. EMS data

Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

Table 54. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP48 conforming to IEC61967-2	0.1 MHz to 30 MHz	-3	dBµV
			30 MHz to 130 MHz	9	
			130 MHz to 1 GHz	4	
			SAE EMI Level	2	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results, not tested in production.

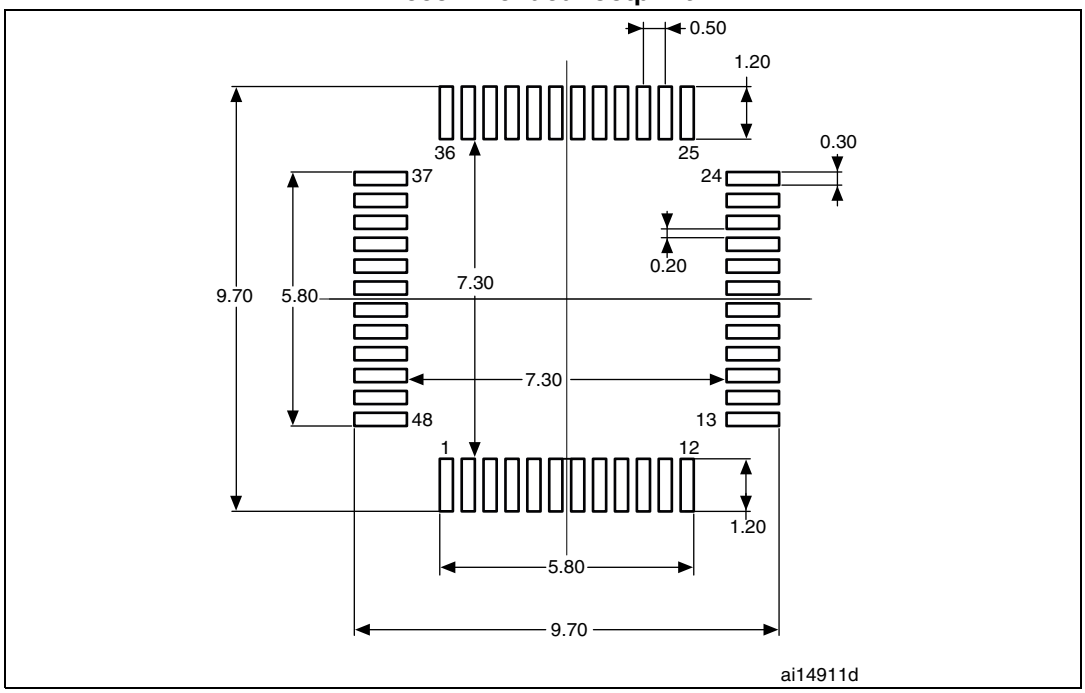
Static latch-up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 56. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

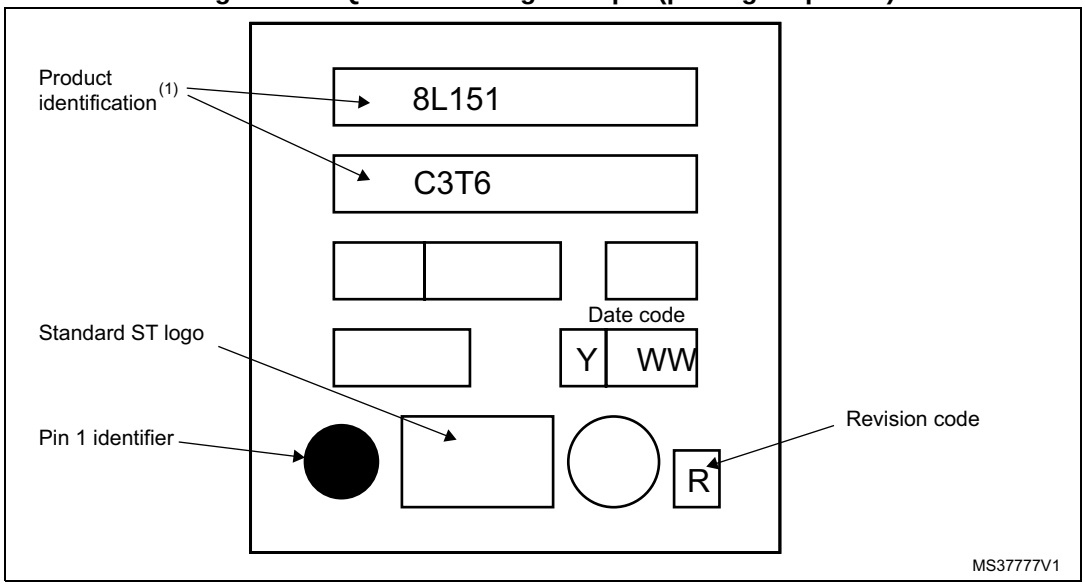


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

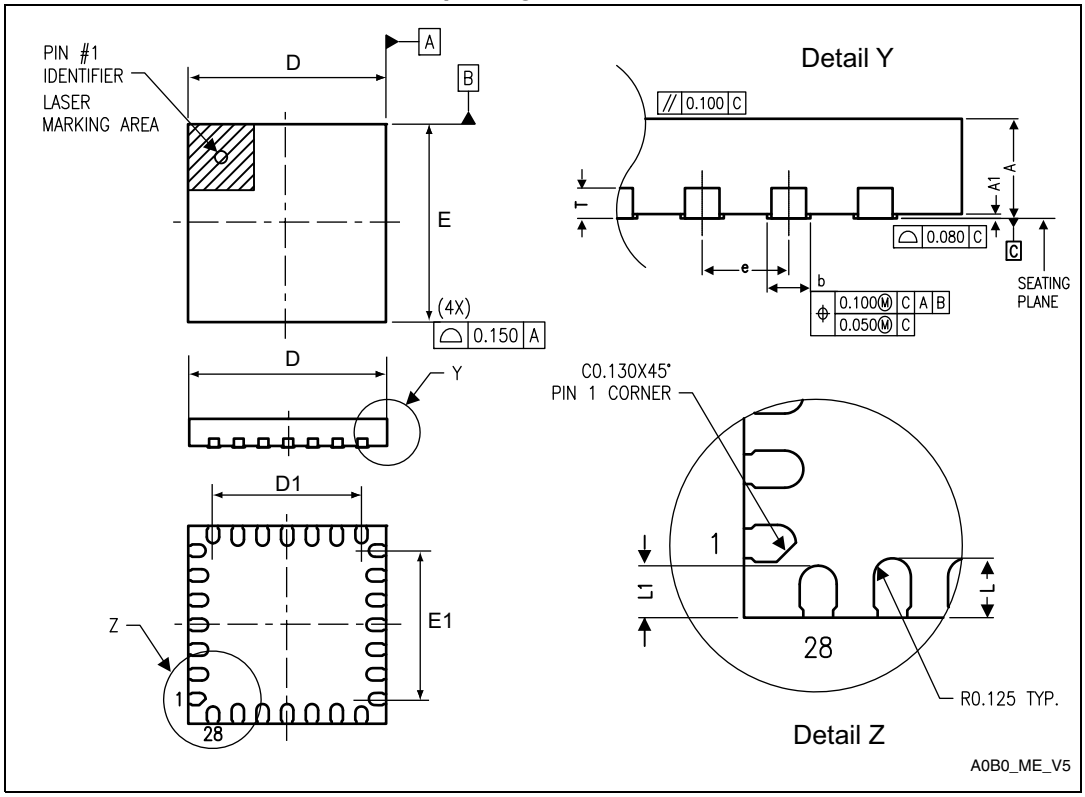
Figure 44. LQFP48 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.4 UFQFPN28 package information

Figure 48. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.

Table 59. UFQFPN28 - 28-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

Table 64. Document revision history (continued)

Date	Revision	Changes
18-Dec-2014	6	Updated *Section: UFQFPN20 package information.* Replaced “ultralow power” occurrences with “ultra-low-power”, and “Low density” with “low-density” where applicable.
08-Apr-2015	7	Added: – *Figure 44: LQFP48 marking example (package top view)*, – *Figure 47: UFQFPN32 marking example (package top view)*, – *Figure 50: UFQFPN28 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 56: TSSOP20 marking example (package top view)*. Updated: – *Table 63: Low-density STM8L151x2/3 ordering information scheme*. Moved *Section 10.7: Thermal characteristics* to *Section 10: Package information*.
01-Oct-2016	8	In *Table 4: Low-density STM8L151x2/3 pin description* row corresponding to pin names PD6/ADC1_IN8 / RTC_CALIB/COMP1_INP, inserted pin number 35 in LQFP48 column.