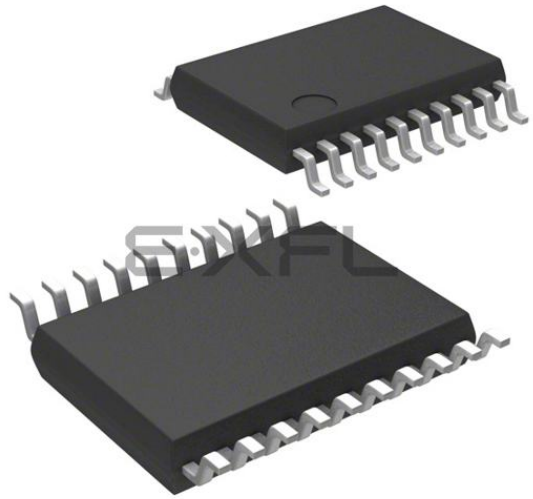

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

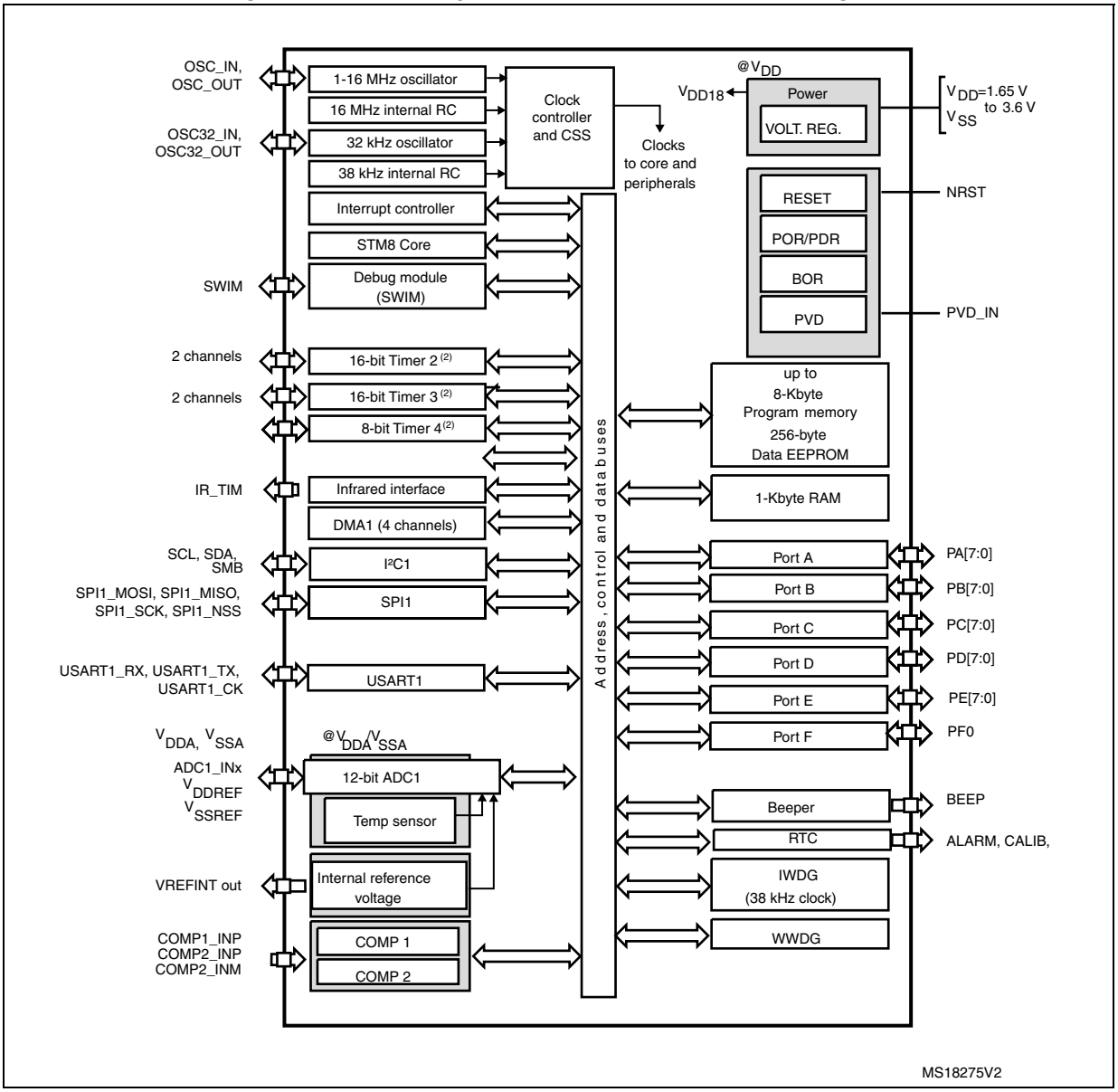
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151f2p6tr

List of tables

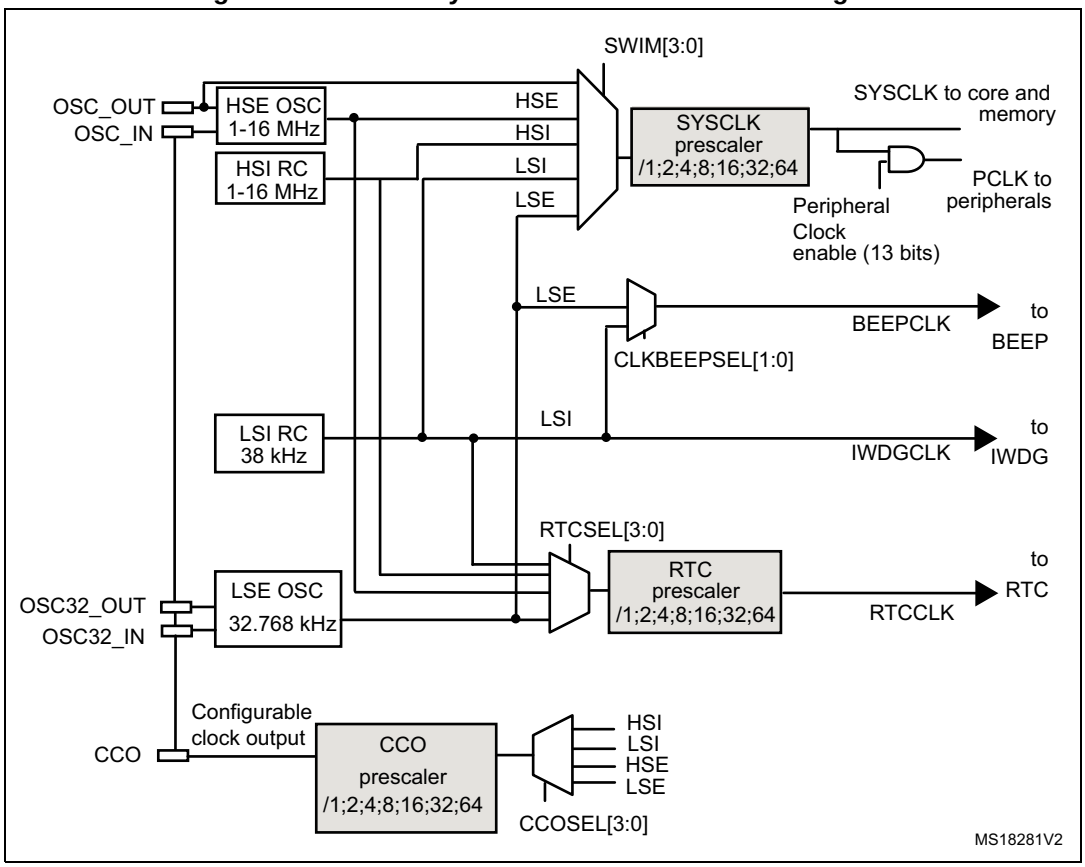
3 Functional overview

Figure 1. Low-density STM8L151x2/3 device block diagram



1. **Legend**:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   I²C: Inter-integrated circuit multi master interface
   IWDG: Independent watchdog
   POR/PDR: Power on reset / power down reset
   RTC: Real-time clock
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   WWDG: Window watchdog
2. There is no TIM1 on STM8L151x2, STM8L151x3 devices.

Figure 2. Low-density STM8L151x2/3 clock tree diagram



3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

Figure 5. STM8L151Gx UFQFPN28 package pinout

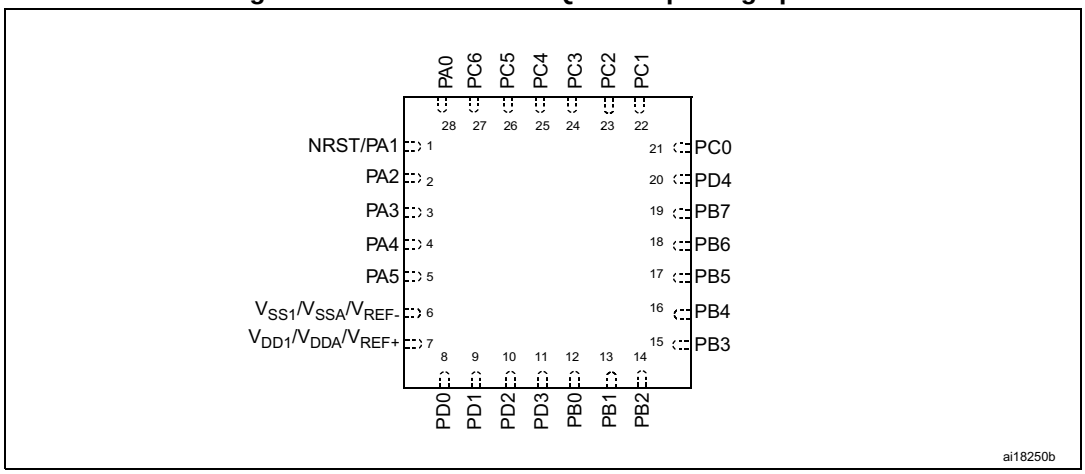


Figure 6. STM8L151Fx UFQFPN20 package pinout

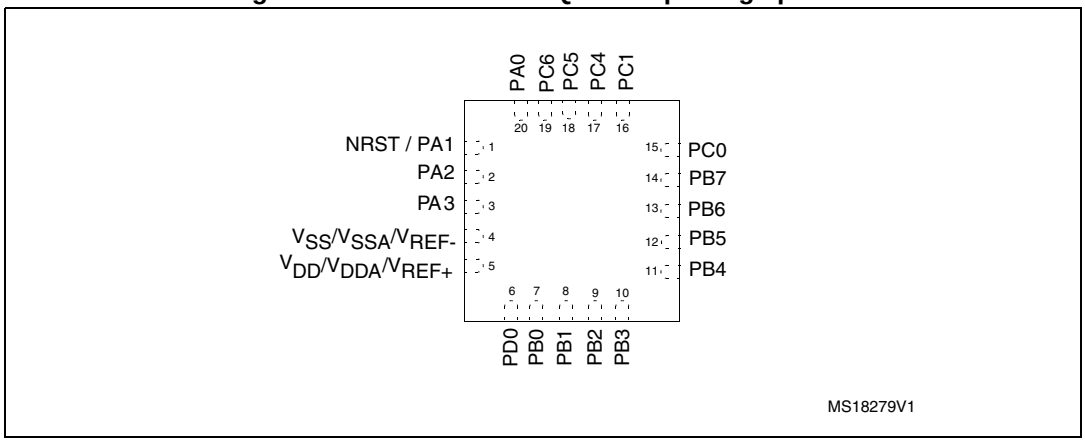
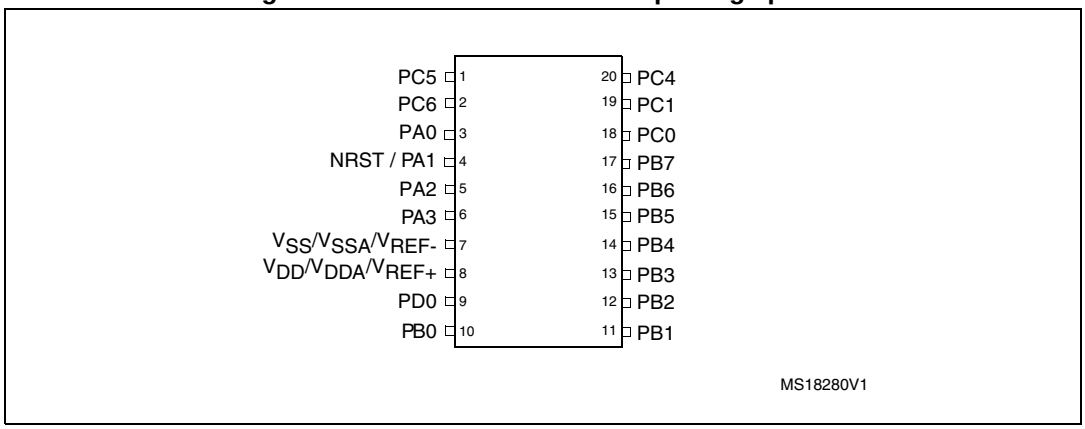


Figure 7. STM8L151Fx TSSOP20 package pinout

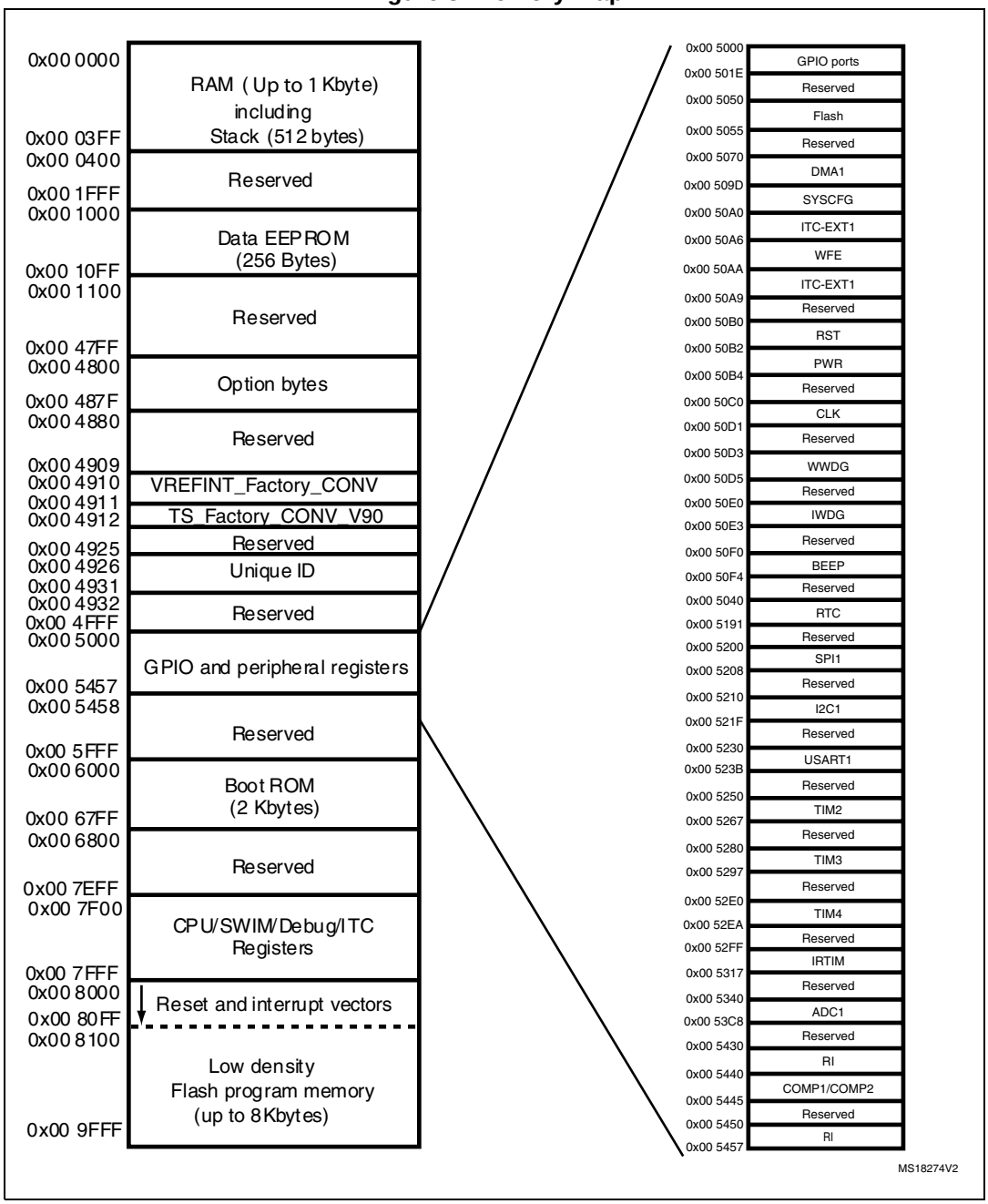


5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC1 conversion result. The

Table 7. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (44 byte)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Flash data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 542F	Reserved area (104 byte)			
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	RI timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	RI timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	RI I/O input register 1	0xXX
0x00 5434		RI_IOIR2	RI I/O input register 2	0xXX
0x00 5435		RI_IOIR3	RI I/O input register 3	0xXX
0x00 5436		RI_IOCMR1	RI I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	RI I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	RI I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	RI I/O switch register 1	0x00
0x00 543A		RI_IOSR2	RI I/O switch register 2	0x00
0x00 543B		RI_IOSR3	RI I/O switch register 3	0x00
0x00 543C		RI_IOGCR	RI I/O group control register	0xFF
0x00 543D		RI_ASCR1	RI analog switch register 1	0x00
0x00 543E		RI_ASCR2	RI analog switch register 2	0x00
0x00 543F		RI_RCR	RI resistor control register	0x00
0x00 5440	COMP1/ COMP2	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00
0x00 5445 to 0x00 544F	Reserved area (11 byte)			
0x00 5450	RI	RI_CR	RI I/O control register	0x00
0x00 5451		RI_MASKR1	RI I/O mask register 1	0x00
0x00 5452		RI_MASKR2	RI I/O mask register 2	0x00
0x00 5453		RI_MASKR3	RI I/O mask register 3	0x00
0x00 5454		RI_MASKR4	RI I/O mask register 4	0x00
0x00 5455		RI_IOIR4	RI I/O input register 4	0xXX
0x00 5456		RI_IOCMR4	RI I/O control mode register 4	0x00
0x00 5457		RI_IOSR4	RI I/O switch register 4	0x00

1. For device in 20-pin packages
2. These registers are not impacted by a system reset. They are reset at power-on.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 11* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	- 5 / +0	mA
	Injected current on 3.6 V tolerant pins (1)	- 5 / +0	
	Injected current on any other pin (1)	- 5 / +5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (2)	± 25	

1. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14.* for maximum allowed input voltage values.
2. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤ V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	-		1.65(2)	3.6	V
V_{DDA}	Analog operating voltage	ADC1 not used	Must be at the same potential as V_{DD}	1.65(2)	3.6	V
		ADC1 used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix 3 and suffix 6 devices	LQFP48		-	288	mW
		UFQFPN32		-	288	
		UFQFPN28		-	250	
		UFQFPN20		-	196	
		TSSOP20		-	181	
	Power dissipation at T_A= 125 °C for suffix 3 devices	LQFP48		-	77	
		UFQFPN32		-	185	
		UFQFPN28		-	62	
		UFQFPN20		-	49	
		TSSOP20		-	45	
T_A	Temperature range	1.65 V ≤ V_{DD} < 3.6 V (6 suffix version)		-40	85	°C
		1.65 V ≤ V_{DD} < 3.6 V (3 suffix version)		-40	125	
T_J	Junction temperature range	-40 °C ≤ T_A < 85 °C (6 suffix version)		-40	105(4)	
		-40 °C ≤ T_A < 125 °C (3 suffix version)		-40	130(4)	

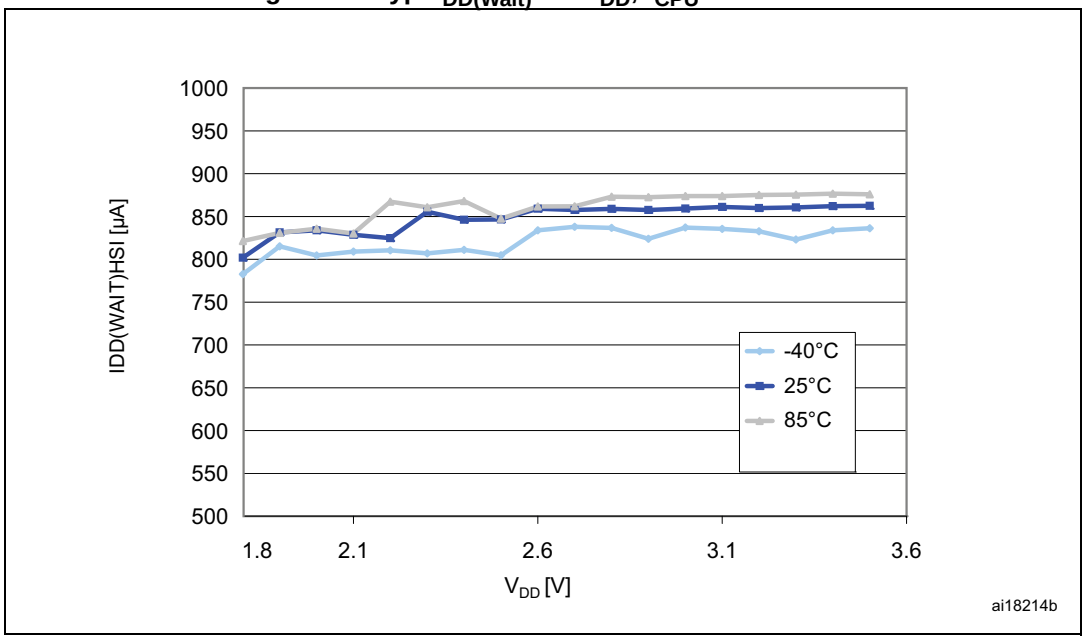
1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.
4. T_J max is given by the test limit. Above this value, the product behavior is not guaranteed.

Table 20. Total current consumption in Wait mode (continued)

Symbol	Parameter	Conditions[1]			Typ	Max				Unit
						55°C	85 °C	105 °C (2)	125 °C (2)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.48	0.49	0.50	0.56	mA
				f_{CPU} = 1 MHz	0.41	0.49	0.51	0.53	0.59	
				f_{CPU} = 4 MHz	0.50	0.57	0.58	0.62	0.66	
				f_{CPU} = 8 MHz	0.60	0.66	0.68	0.72	0.74	
				f_{CPU} = 16 MHz	0.79	0.84	0.86	0.87	0.90	
			HSE[4] external clock (f_{CPU}=HSE)	f_{CPU} = 125 kHz	0.06	0.08	0.09	0.10	0.12	
				f_{CPU} = 1 MHz	0.10	0.17	0.18	0.19	0.22	
				f_{CPU} = 4 MHz	0.24	0.36	0.39	0.41	0.44	
				f_{CPU} = 8 MHz	0.50	0.58	0.61	0.62	0.64	
				f_{CPU} = 16 MHz	1.00	1.08	1.14	1.16	1.18	
			LSI	$f_{CPU} = f_{LSI}$	0.055	0.058	0.065	0.073	0.080	
			LSE[6] external clock (32.768 kHz)	$f_{CPU} = f_{LSE}$	0.051	0.056	0.060	0.065	0.073	

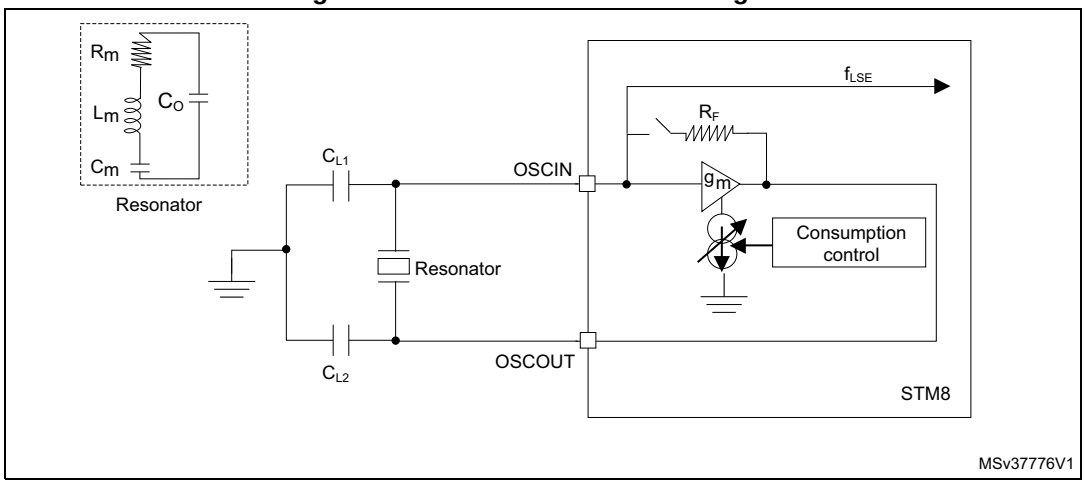
1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. For temperature range 3.
3. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 30*.
5. Tested in production.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.

Figure 13. Typ. $I_{DD(Wait)}$ vs. V_{DD}, f_{CPU} = 16 MHz [1)]



1. Typical current consumption measured with code executed from Flash memory.

Figure 17. LSE oscillator circuit diagram



Internal clock sources

Subject to general operating conditions for V_{DD}, and T_A.

High speed internal RC oscillator (HSI)

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 32. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)(2)	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1 (3)	-	1(3)	%
		V_{DD} = 3.0 V, 0 °C ≤ T_A ≤ 55 °C	-1.5	-	1.5	%
		V_{DD} = 3.0 V, -10 °C ≤ T_A ≤ 70 °C	-2	-	2	%
		V_{DD} = 3.0 V, -10 °C ≤ T_A ≤ 85 °C	-2.5	-	2	%
		V_{DD} = 3.0 V, -10 °C ≤ T_A ≤ 125 °C	-4.5	-	2	%
		1.65 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤ 125 °C	-4.5	-	3	%
TRIM	HSI user trimming step(4)	Trimming code ≠ multiple of 16	-	0.4	0.7	%
		Trimming code = multiple of 16	-		± 1.5	%
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6(5)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(5)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. T_A > 85 °C is valid only for devices with suffix 3 temperature range.
3. Tested in production.
4. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
5. Guaranteed by design, not tested in production.

Figure 22. Typical pull-up resistance R_{PU} vs V_{DD} with $V_{IN}=V_{SS}$

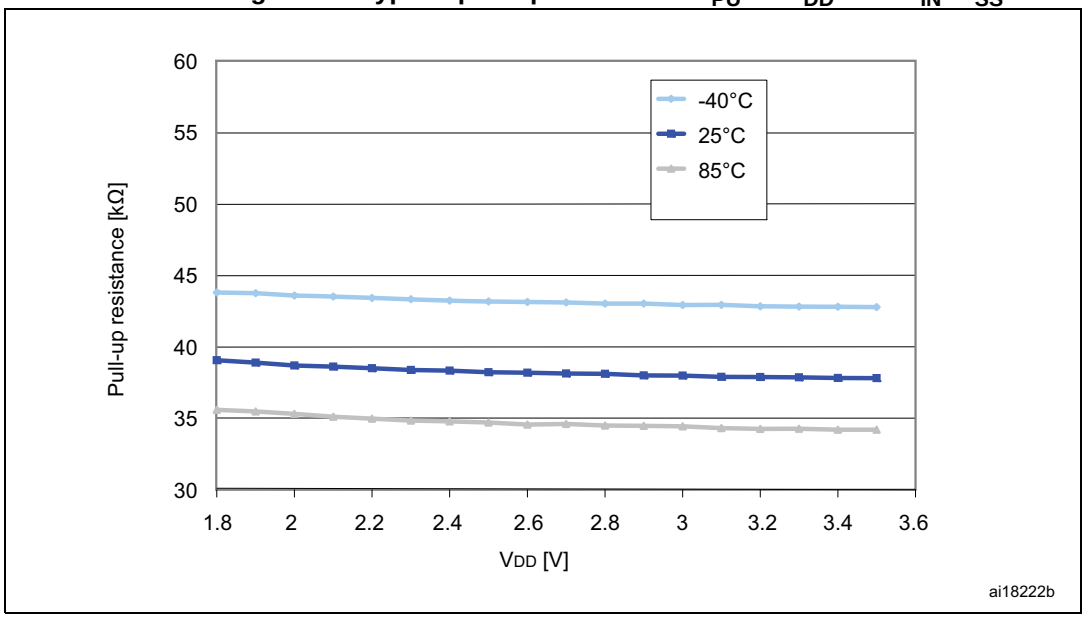


Figure 23. Typical pull-up current I_{pu} vs V_{DD} with $V_{IN}=V_{SS}$

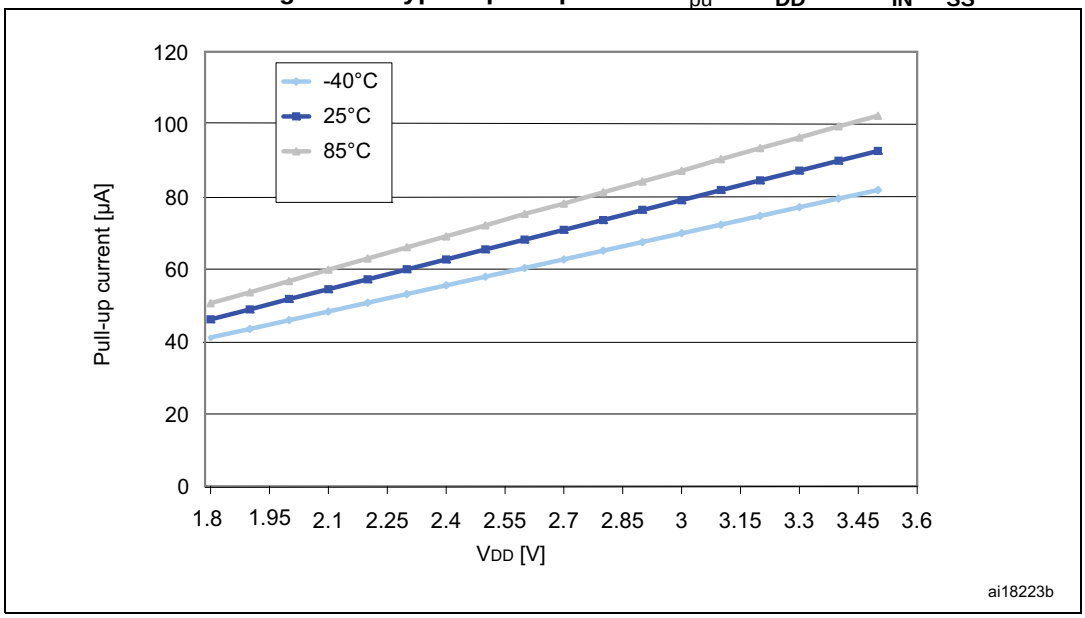
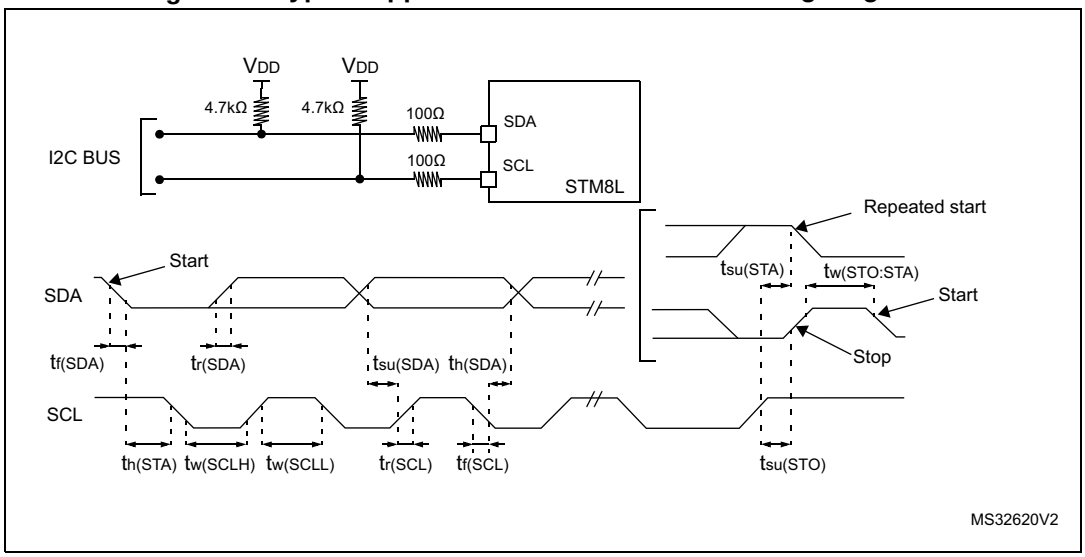


Figure 36. Typical application with I²C bus and timing diagram [1)]



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

Table 48. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)	-	-	µs
		V_{AIN} on PF0 fast channel 2.4 V ≤ V_{DDA}≤ 3.6 V	0.22(4)(5)	-	-	µs
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)	-	-	µs
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.41(4)(5)	-	-	µs
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC1}$
		16 MHz	1(4)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(6)	Time before a new conversion	T_A = +25 °C	-	-	1(7)	s
		T_A = +70 °C	-	-	20(7)	ms
		T_A = +125 °C	-	-	2(7)	ms
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 44*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design, not tested in production.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC1 ON and the first conversion must be lower than t_{IDLE}.
7. The t_{IDLE} maximum value is ∞ on the “Z” revision code of the device.

In the following three tables, data is guaranteed by characterization result, not tested in production.

Table 49. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
DNL	Differential non linearity	f_{ADC1} = 16 MHz	1	1.6	LSB
		f_{ADC1} = 8 MHz	1	1.6	
		f_{ADC1} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC1} = 16 MHz	1.2	2	
		f_{ADC1} = 8 MHz	1.2	1.8	
		f_{ADC1} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC1} = 16 MHz	2.2	3.0	
		f_{ADC1} = 8 MHz	1.8	2.5	
		f_{ADC1} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC1} = 16 MHz	1.5	2	LSB
		f_{ADC1} = 8 MHz	1	1.5	
		f_{ADC1} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC1} = 16 MHz	1	1.5	
		f_{ADC1} = 8 MHz			
		f_{ADC1} = 4 MHz			

Table 50. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

Table 51. ADC1 accuracy with V_{DDA} = V_{REF}^+ = 1.8 V to 2.4 V

Symbol	Parameter	Typ	Max	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

Figure 39. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

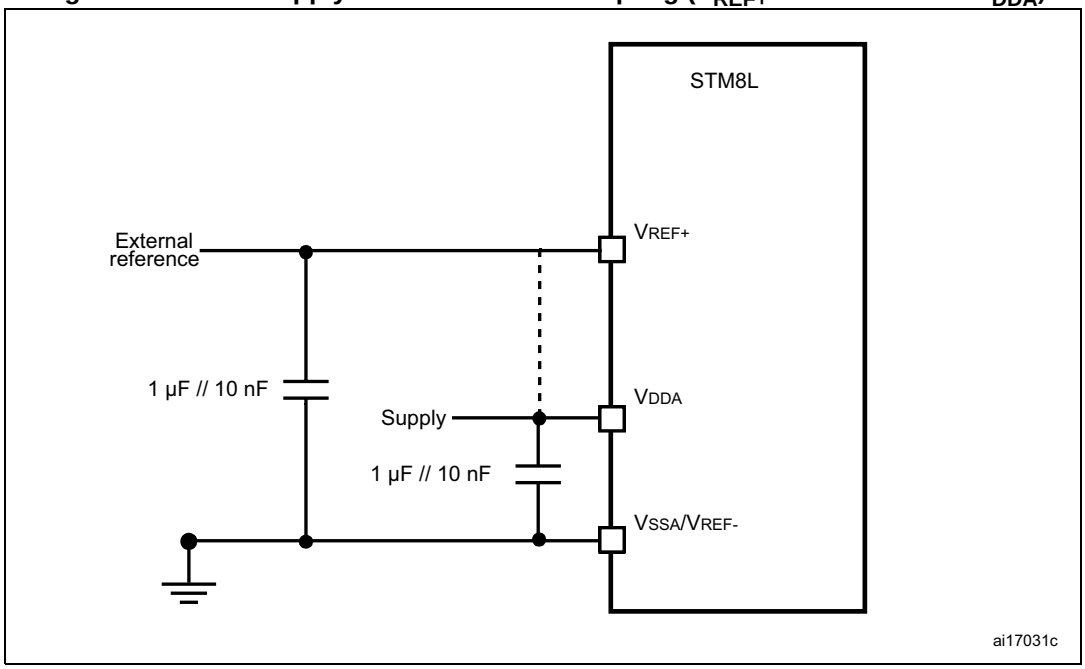


Figure 40. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

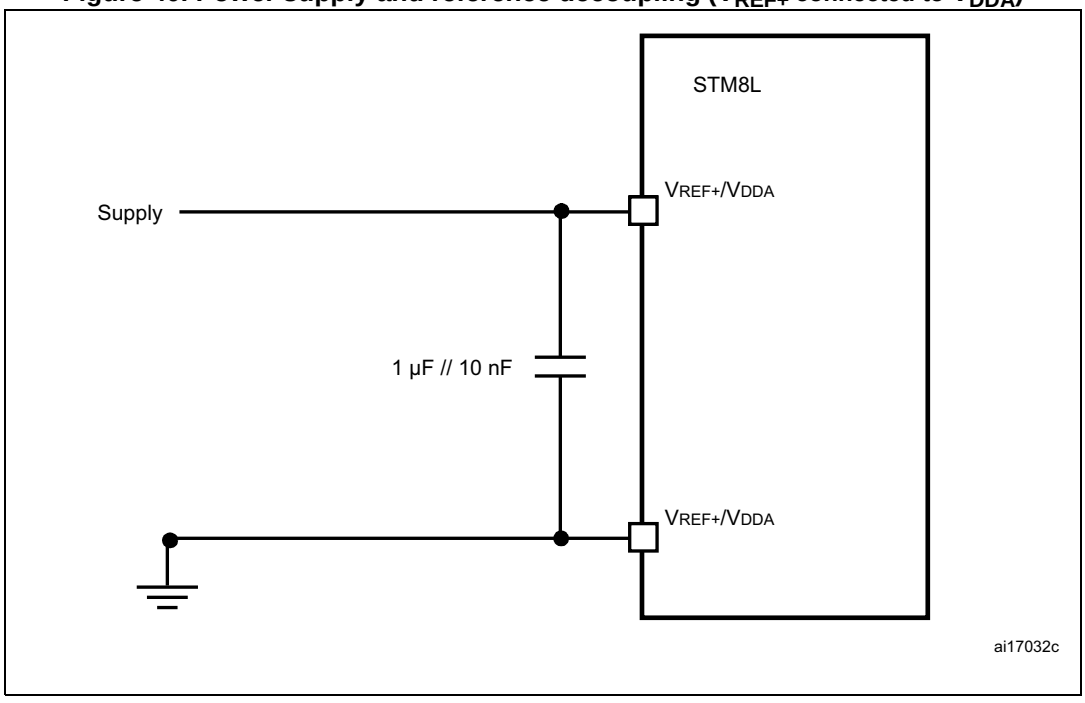
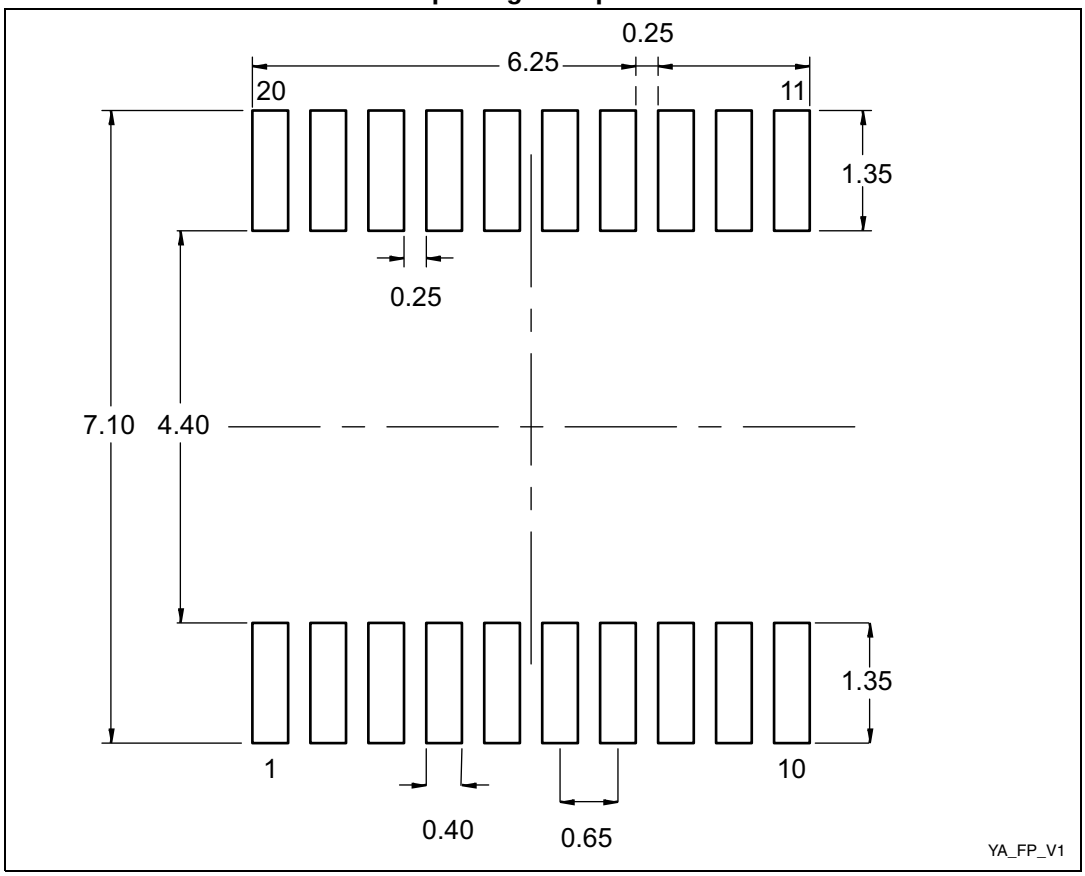


Table 61. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 55. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.