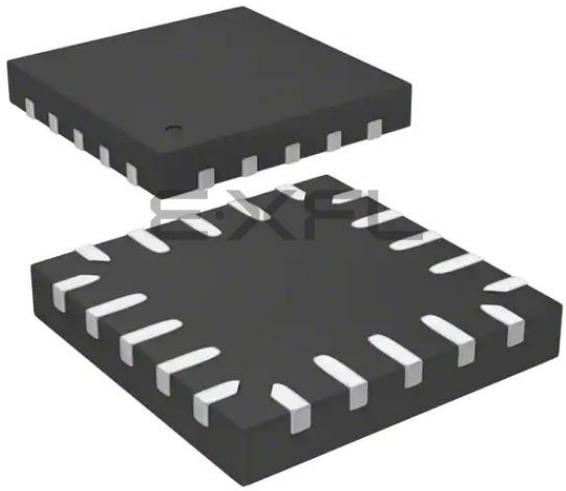

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151f2u6tr

Contents

3.10 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface controls the routing of internal analog signals to ADC1, COMP1, COMP2, and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (*Section 3.11: Touch sensing*).

3.11 Touch sensing

Low-density STM8L151x2/3 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (example, glass, plastic). The capacitive variation introduced by a finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In low-density STM8L15xxx devices, the acquisition sequence is managed either by software or by hardware and it involves analog I/O groups, the routing interface, and timers.Reliable touch sensing solutions can be quickly and easily implemented using the free STM8 Touch Sensing Library.

3.12 Timers

Low-density STM8L151x2/3devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 2 compares the features of the advanced control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	up/down	Any power of 2 from 1 to 128	Yes	2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

4 Pinout and pin description

Figure 3. STM8L151Cx LQFP48 package pinout

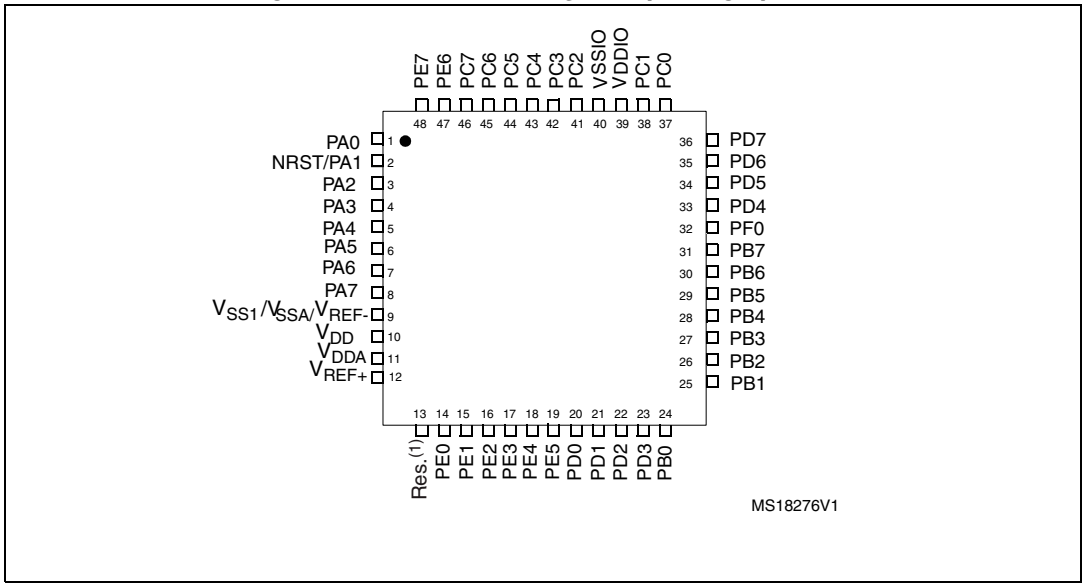


Figure 4. STM8L151Kx UFQFPN32 package pinout

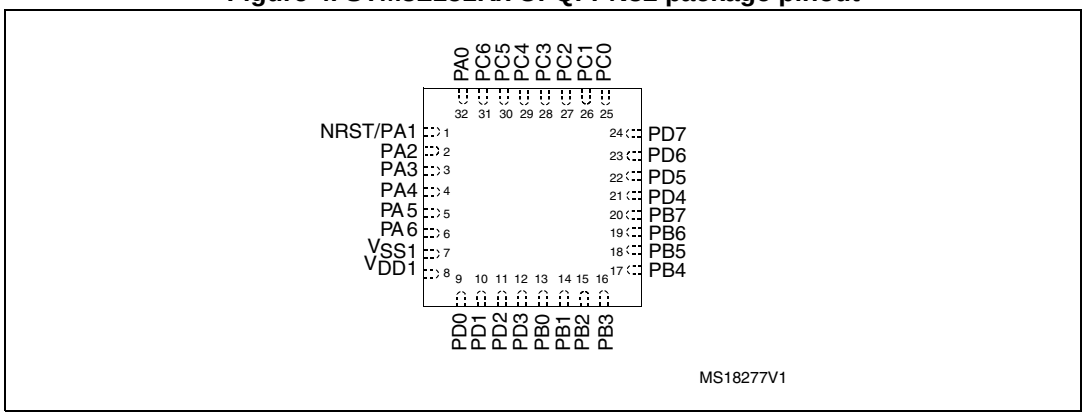


Table 4. Low-density STM8L151x2/3 pin description (continued)

Pin number					Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	UFQFPN32	UFQFPN28	UFQFPN20	TSSOP20				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
25	14	13	8	11	PB1/TIM3_CH1/ ADC1_IN17/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel1/ ADC1_IN17/ Comparator1 positive input
26	15	14	9	12	PB2/ TIM2_CH2/ ADC1_IN16/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel2 ADC1_IN16/ Comparator1 positive input
27	16	15	10	13	PB3/TIM2_ETR/ ADC1_IN15/RTC_ALARM[4]/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - external trigger / ADC1_IN15 / RTC_ALARM [4]/Comparator1 positive input
28	17	16	11	14	PB4[3]/SPI1_NSS/ ADC1_IN14/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B4**	SPI master/slave select / ADC1_IN14/ Comparator1 positive input
29	18	17	12	15	PB5/SPI_SCK/ /ADC1_IN13/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B5**	[SPI clock] / ADC1_IN13/ Comparator 1 positive input
30	19	18	13	16	PB6/SPI1_MOSI/ ADC1_IN12/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B6**	SPI master out/ slave in / ADC1_IN12/ Comparator1 positive input
31	20	19	14	17	PB7/SPI1_MISO/ ADC1_IN11/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in-slave out/ ADC1_IN11/ Comparator1 positive input
37	25	21	15	18	PC0/I2C_SDA	I/O	FT	**X**		X		T[5]		**Port C0**	I2C data
38	26	22	16	19	PC1/I2C_SCL	I/O	FT	**X**		X		T[5]		**Port C1**	I2C clock
41	27	23	-	-	PC2/USART_RX/ADC 1_IN6/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port C2**	USART receive / ADC1_IN6/ Comparator1 positive input
42	28	24	-	-	PC3/USART_TX/ ADC1_IN5/ COMP1_INP/ COMP2_INM	I/O	-	**X**	X	X	HS	X	X	**Port C3**	USART transmit / ADC1_IN5/ Comparator1 positive input/Comparator 2 negative input

MSB have a fixed value: 0x6.

3. The TS_Factory_CONV_V90 byte represents the LSB of the V_{90} 12-bit ADC1 conversion result. The MSB have a fixed value: 0x3.
4. Refer to *Table 8* for an overview of hardware register mapping, to *Table 7* for details on I/O port hardware registers, and to *Table 9* for information on CPU/SWIM/debug module controller registers.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1 Kbyte	0x00 0000	0x00 03FF
Flash program memory	8 Kbyte	0x00 8000	0x00 9FFF
	4 Kbyte	0x00 8000	0x00 8FFF

5.2 Register map

Table 6. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV	Value of the internal reference voltage measured during the factory phase	0xXX
0x00 4911	-	TS_Factory_CONV_V90	Value of the temperature sensor output voltage measured during the factory phase	0xXX

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x0C
				0x2C(1)
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 byte)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 542F	Reserved area (104 byte)			
0x00 5430	RI	Reserved area (1 byte)		0x00
0x00 5431		RI_ICR1	RI timer input capture routing register 1	0x00
0x00 5432		RI_ICR2	RI timer input capture routing register 2	0x00
0x00 5433		RI_IOIR1	RI I/O input register 1	0xXX
0x00 5434		RI_IOIR2	RI I/O input register 2	0xXX
0x00 5435		RI_IOIR3	RI I/O input register 3	0xXX
0x00 5436		RI_IOCMR1	RI I/O control mode register 1	0x00
0x00 5437		RI_IOCMR2	RI I/O control mode register 2	0x00
0x00 5438		RI_IOCMR3	RI I/O control mode register 3	0x00
0x00 5439		RI_IOSR1	RI I/O switch register 1	0x00
0x00 543A		RI_IOSR2	RI I/O switch register 2	0x00
0x00 543B		RI_IOSR3	RI I/O switch register 3	0x00
0x00 543C		RI_IOGCR	RI I/O group control register	0xFF
0x00 543D		RI_ASCR1	RI analog switch register 1	0x00
0x00 543E		RI_ASCR2	RI analog switch register 2	0x00
0x00 543F		RI_RCR	RI resistor control register	0x00
0x00 5440	COMP1/ COMP2	COMP_CSR1	Comparator control and status register 1	0x00
0x00 5441		COMP_CSR2	Comparator control and status register 2	0x00
0x00 5442		COMP_CSR3	Comparator control and status register 3	0x00
0x00 5443		COMP_CSR4	Comparator control and status register 4	0x00
0x00 5444		COMP_CSR5	Comparator control and status register 5	0x00
0x00 5445 to 0x00 544F	Reserved area (11 byte)			
0x00 5450	RI	RI_CR	RI I/O control register	0x00
0x00 5451		RI_MASKR1	RI I/O mask register 1	0x00
0x00 5452		RI_MASKR2	RI I/O mask register 2	0x00
0x00 5453		RI_MASKR3	RI I/O mask register 3	0x00
0x00 5454		RI_MASKR4	RI I/O mask register 4	0x00
0x00 5455		RI_IOIR4	RI I/O input register 4	0xXX
0x00 5456		RI_IOCMR4	RI I/O control mode register 4	0x00
0x00 5457		RI_IOSR4	RI I/O switch register 4	0x00

1. For device in 20-pin packages
2. These registers are not impacted by a system reset. They are reset at power-on.

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics is indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

9.1.2 Typical values

Unless otherwise specified, typical data is based on T_A = 25 °C, V_{DD} = 3 V. It is given only as design guidelines and is not tested.

Typical ADC1 accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

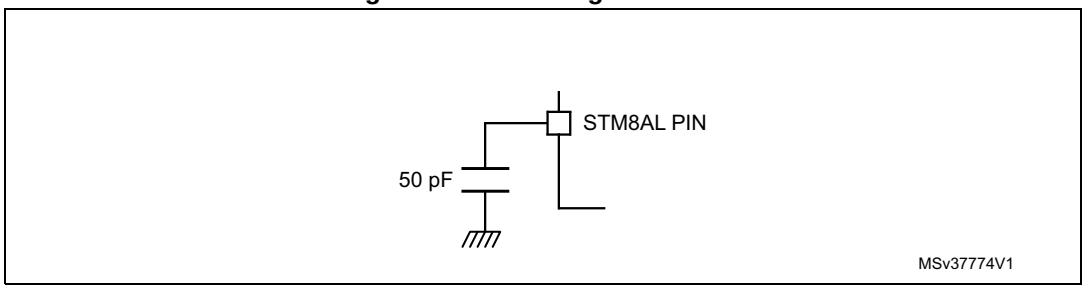
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

Figure 9. Pin loading conditions



In the following table, data is based on characterization results, unless otherwise specified.

Table 22. Total current consumption in Low power wait mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)(2)			Typ	Max	Unit
$I_{DD(LPW)}$	Supply current in Low power wait mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	3	3.3	µA
				T_A = 55 °C	3.3	3.6	
				T_A = 85 °C	4.4	5	
				T_A = 105 °C	6.7	8	
				T_A = 125 °C	11	14	
			with TIM2 active(3)	T_A = -40 °C to 25 °C	3.4	3.7	
				T_A = 55 °C	3.7	4	
				T_A = 85 °C	4.8	5.4	
				T_A = 105 °C	7	8.3	
				T_A = 125 °C	11.3	14.5	
		LSE external clock(4) (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	2.35	2.7	
				T_A = 55 °C	2.42	2.82	
				T_A = 85 °C	3.10	3.71	
				T_A = 105 °C	4.36	5.7	
				T_A = 125 °C	7.20	11	
			with TIM2 active (3)	T_A = -40 °C to 25 °C	2.46	2.75	
				T_A = 55 °C	2.50	2.81	
				T_A = 85 °C	3.16	3.82	
				T_A = 105 °C	4.51	5.9	
				T_A = 125 °C	7.28	11	

1. No floating I/Os.
2. T_A > 85 °C is valid only for devices with suffix 3 temperature range.
3. Timer 2 clock enabled and counter is running.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 31*.

Table 37. I/O static characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3	-	0.3 x V_{DD}	V
		Input voltage on any other pin	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on any other pin	0.70 x V_{DD}	-	V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ High sink I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(2)(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 23*).

Figure 24. Typ. V_{OL} @ V_{DD} = 3.0 V (high sink ports)

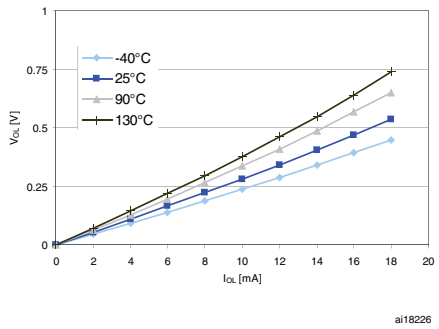


Figure 25. Typ. V_{OL} @ V_{DD} = 1.8 V (high sink ports)

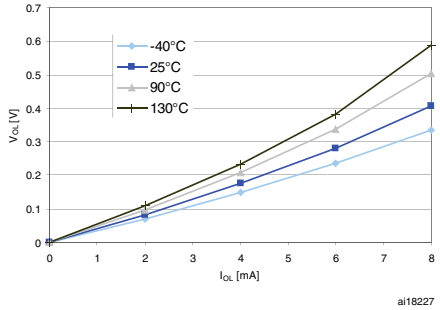


Figure 26. Typ. V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

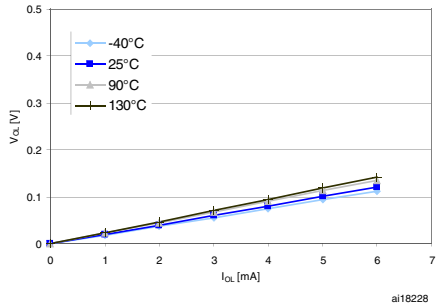


Figure 27. Typ. V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

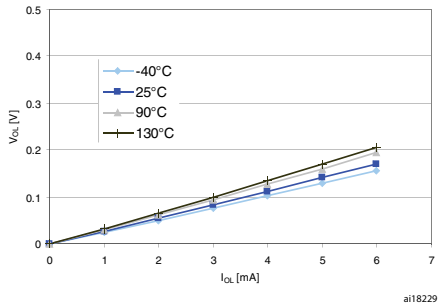


Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

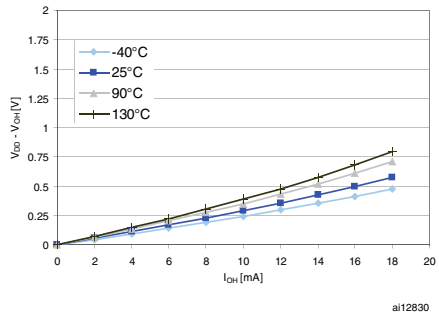
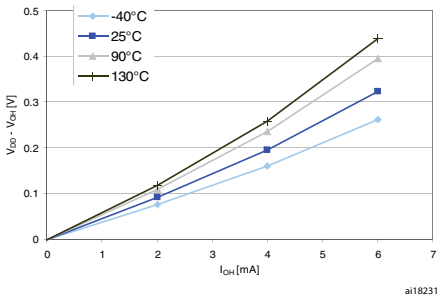


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)



NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD} (2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results, not tested in production.
2. 200 mV min.
3. Data guaranteed by design, not tested in production.

Figure 30. Typical NRST pull-up resistance R_{PU} vs V_{DD}

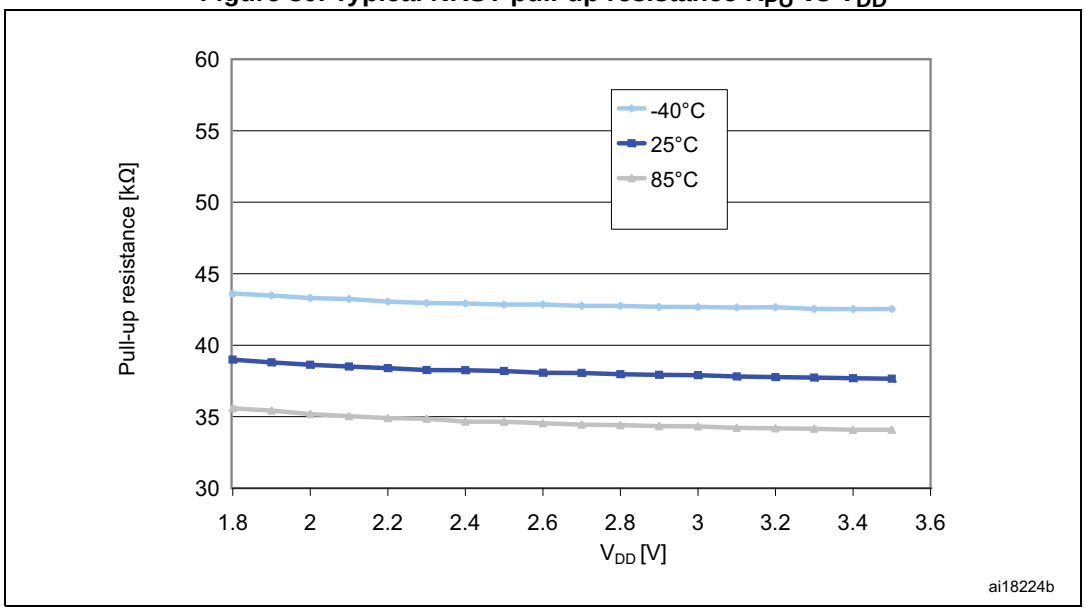
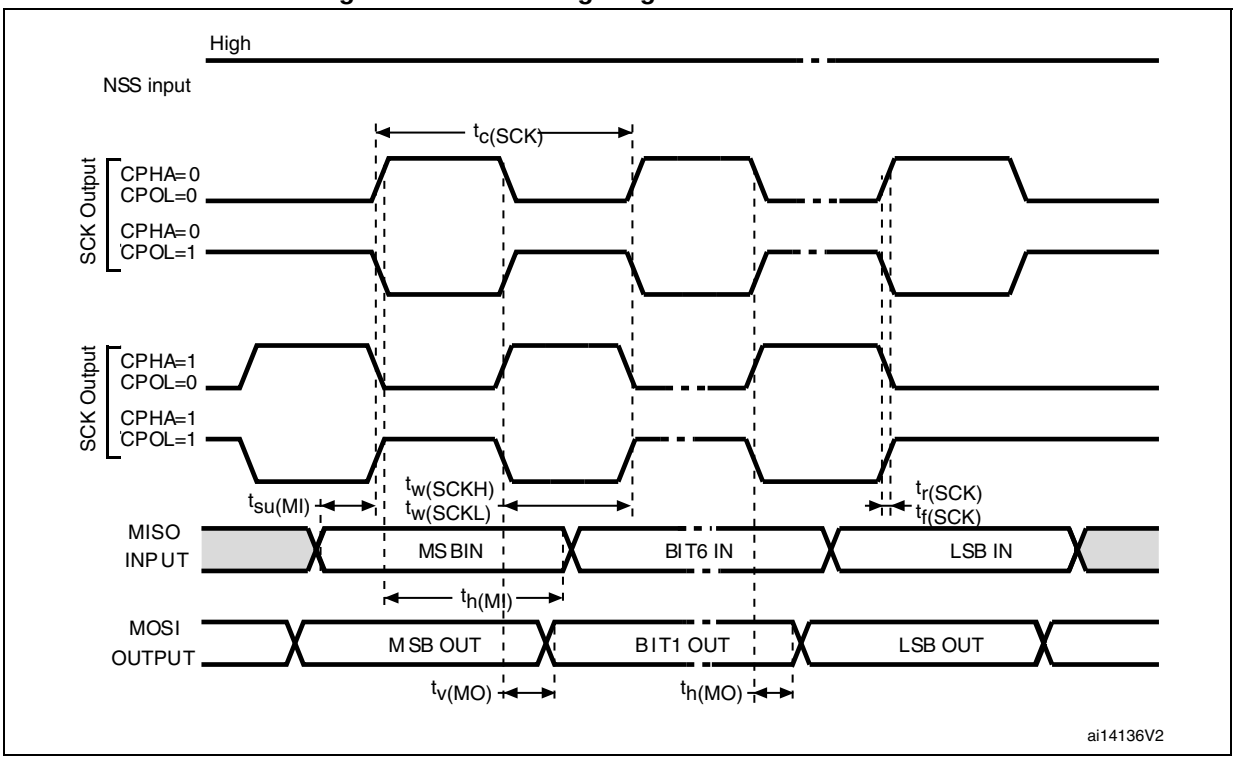


Figure 35. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.9 Embedded reference voltage

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 44. Reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC1 sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(2)	Internal reference voltage buffer consumption (used for ADC1)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202(3)	1.224	1.242(3)	V
I_{LPBUF}(2)	Internal reference voltage low power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(2)	Buffer output current(4)	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(2)	Internal reference voltage buffer startup time once enabled (1)	-	-	-	10	µs
$ACC_{VREFINT}$	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte(5)	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤ T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤ T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Defined when ADC1 output reaches its final value ±1/2LSB
2. Data guaranteed by Design. Not tested in production.
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guaranty less than 1% V_{REFOUT} deviation.
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC1 conversion accuracy.

Table 48. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)	-	-	µs
		V_{AIN} on PF0 fast channel 2.4 V ≤ V_{DDA}≤ 3.6 V	0.22(4)(5)	-	-	µs
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)	-	-	µs
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.41(4)(5)	-	-	µs
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC1}$
		16 MHz	1(4)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(6)	Time before a new conversion	T_A = +25 °C	-	-	1(7)	s
		T_A = +70 °C	-	-	20(7)	ms
		T_A = +125 °C	-	-	2(7)	ms
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 44*	ms

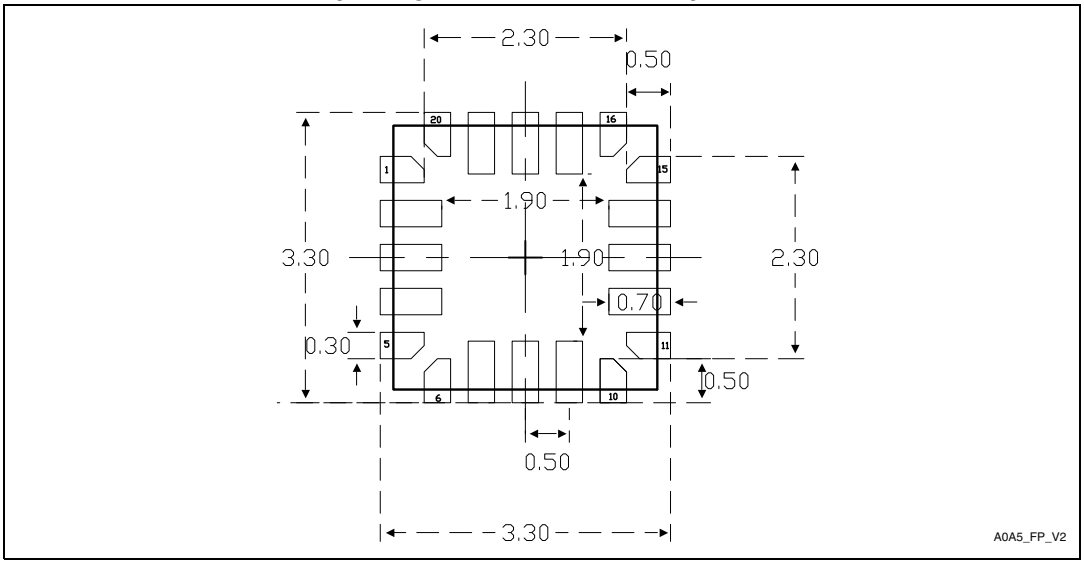
1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design, not tested in production.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC1 ON and the first conversion must be lower than t_{IDLE}.
7. The t_{IDLE} maximum value is ∞ on the “Z” revision code of the device.

Table 60. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-		0.0148	
L4	-	0.200	-		0.0079	
L5	-	0.150	-		0.0059	
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

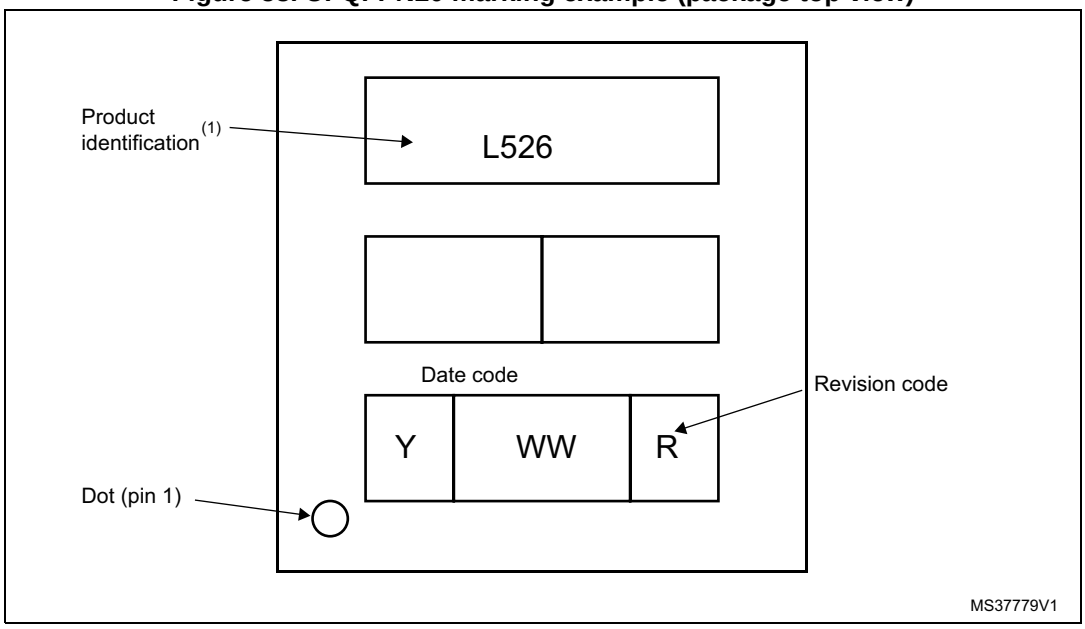


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 53. UFQFPN20 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

12 Revision history

Table 64. Document revision history

Date	Revision	Changes
08-Jun-2011	1	Initial release
02-Sep-2011	2	Modified *Figure: Memory map.* Modified OPT1 description in *Table: Option byte addresses.* Modified t_{prog} in *Table: Flash program and data EEPROM memory.* Modified *Figure: Recommended NRST pin configuration.* Modified L2 in *Figure: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.* Replaced PM0051 with PM0054 and UM0320 with UM0470.
09-Feb-2012	3	Added part number STM8L151C2. Updated the captions of *Figure 3* and *Figure 4*. *Table: Low-density STM8L151x2/3 pin description*: updated OD column of NRST/PA1 pin. *Figure: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline:* removed the line over A1. *Figure Recommended UFQFPN28 footprint (dimensions in mm):* updated title. *Table: TSSOP20 - 20-pin thin shrink small outline package mechanical data:* updated title.
06-Jul-2012	4	Added “I/O level” in *Table: Legend/abbreviation for table 4* and *Table: Low-density STM8L151x2/3 pin description.* Updated *Figure: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3).* Updated *Figure: SPI1 timing diagram - master mode.* Updated *Table: Voltage characteristics* and *Table: I/O static characteristics.*
11-Apr-2014	5	Updated *Table: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3x3) package mechanical data,* added notes on *Table: TSSOP20 - 20-pin thin shrink small outline package mechanical data.* Changed reset value of SYSCFG_RMPCR1 register on *Table: General hardware register map.* Updated *Table: Low-density STM8L151x2/3 pin description* and *Table: Embedded reset and power control block characteristics.*