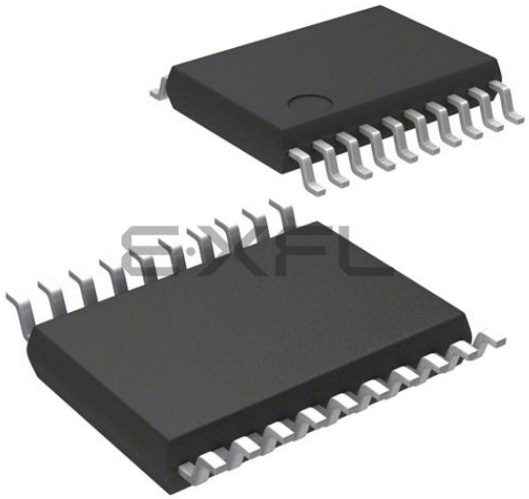

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151f3p3

2.2 Ultra-low-power continuum

The ultra-low-power low-density STM8L151x2/3 devices are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra-low leakage process.

Note: 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L151xx/152xx and STM8L15xxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1 and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L151xx/152xx and STM8L15xxx devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V, down to 1.65 V at power down
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L15x and STM32L15xxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbyte

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- $V_{SSA;}$ V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2}; V_{DD2} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The low-density STM8L151x2/3 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

Table 4. Low-density STM8L151x2/3 pin description (continued)

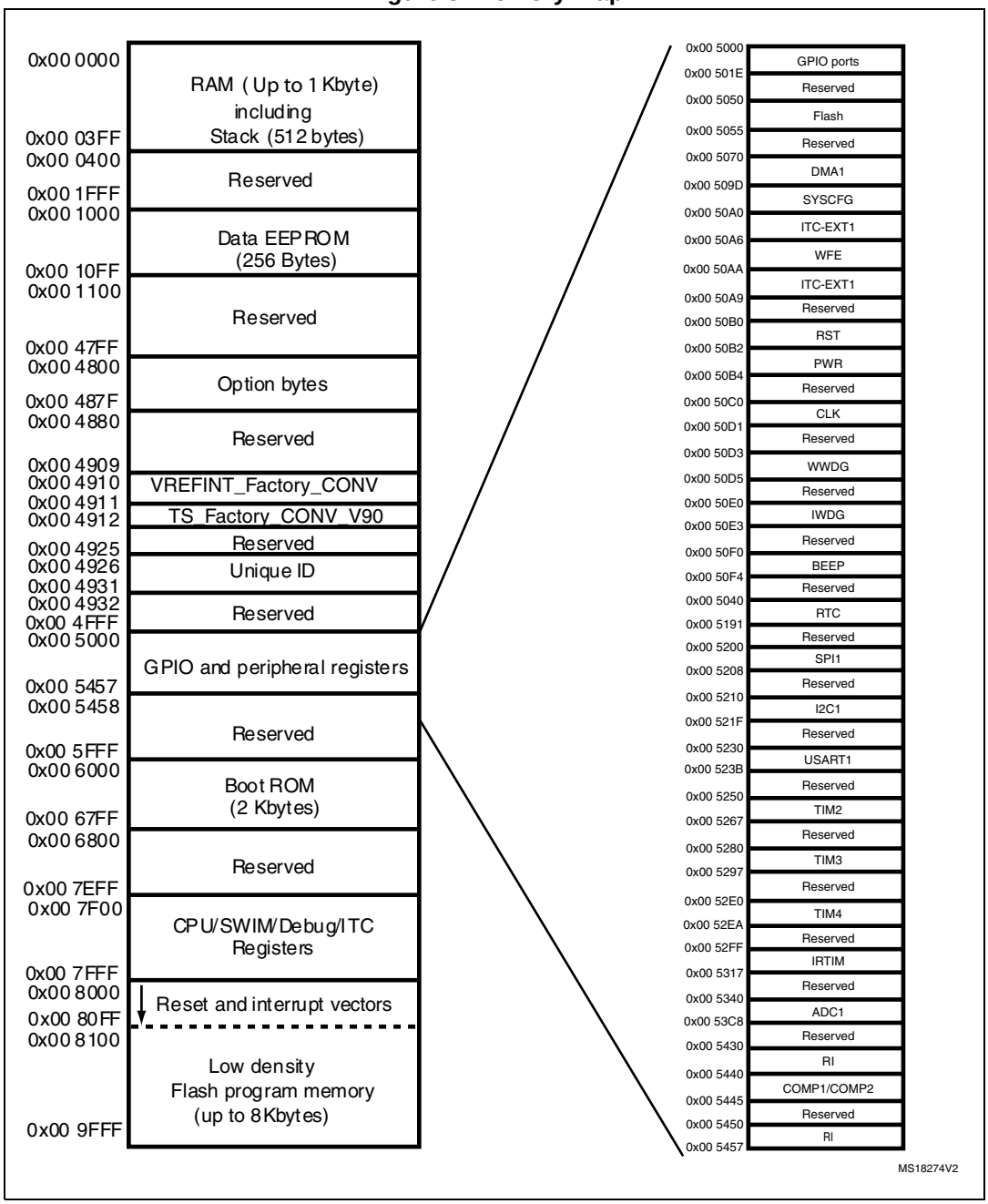
Pin number					Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	UFQFPN32	UFQFPN28	UFQFPN20	TSSOP20				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
43	29	25	17	20	PC4/USART_CK]/ I2C_SMB/CCO/ ADC1_IN4/ COMP1_INP/ COMP2_INM	I/O	-	**X**	X	X	HS	X	X	**Port C4**	USART synchronous clock / I2C1_SMB / Configurable clock output / ADC1_IN4/ Comparator1 positive input/Comparator 2 negative input
44	30	26	18	1	PC5/OSC32_IN /*[SPI1_NSS]*(2)/ *[USART_TX]*(2)/ TIM2_CH1(6)	I/O	-	**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI master/slave select] / [USART transmit]/ Timer 2 -channel 1*(6)
45	31	27	19	2	PC6/OSC32_OUT/ *[SPI_SCK]*(2)/ *[USART_RX]*(2)/ TIM2_CH2(6)	I/O	-	**X**	X	X	HS	X	X	**Port C6**	LSE oscillator output / *[SPI clock] / [USART receive]/ Timer 2 -channel 2*(6)
46	-	-	-	-	PC7/ADC1_IN3/ COMP1_INP/ COMP2_INM	I/O	-	**X**	X	X	HS	X	X	**Port C7**	ADC1_IN3/ Comparator1 positive input/Comparator 2 negative input
20	9	8	6	9	PD0/TIM3_CH2/ *[ADC1_TRIG]*(2)/ ADC1_IN22/ COMP1_INP/ COMP2_INP	I/O	-	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / *[ADC1_Trigger]* / ADC1_IN22/ Comparator1 positive input/Comparator 2 positive input
21	10	9	-	-	PD1/TIM3_ETR/ ADC1_IN21/ COMP1_INP/ COMP2_INP	I/O	-	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - external trigger / ADC1_IN21/ Comparator1 positive input/Comparator 2 positive input
22	11	10	-	-	PD2/ADC1_IN20/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port D2**	ADC1_IN20/ Comparator1 positive input
23	12	11	-	-	PD3/ADC1_IN19/ RTC_CALIB(7)/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port D3**	ADC1_IN19/ RTC calibration(7)/ Comparator1 positive input
33	21	20	-	-	PD4/ADC1_IN10/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port D4**	ADC1_IN10/ Comparator1 positive input

5 Memory and register map

5.1 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. The VREFINT_Factory_CONV byte represents the LSB of the V_{REFINT} 12-bit ADC1 conversion result. The

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C0	CLK	CLK_CKDIVR	CLK clock master divider register	0x03
0x00 50C1		CLK_CRTCR	CLK clock RTC register	0x00(2)
0x00 50C2		CLK_ICKCR	CLK internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	CLK peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	CLK peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	CLK configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	CLK external clock control register	0x00
0x00 50C7		CLK_SCSR	CLK system clock status register	0x01
0x00 50C8		CLK_SWR	CLK system clock switch register	0x01
0x00 50C9		CLK_SWCR	CLK clock switch control register	0xX0
0x00 50CA		CLK_CSSR	CLK clock security system register	0x00
0x00 50CB		CLK_CBEEPR	CLK clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	CLK HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	CLK HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	CLK HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	CLK main regulator control status register	0bxx11 100X
0x00 50D0		CLK_PCKENR3	CLK peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 byte)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0x01
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 byte)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 byte)			

Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	CPU	Reserved area (85 byte)		
0x00 7F60		CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

Table 12. Option byte description (continued)

Option byte No.	Option description
OPT5	**BOR_ON**: 0: Brownout reset off 1: Brownout reset on
	BOR_TH[3:1]: Brownout reset thresholds. Refer to *Table 22* for details on the thresholds according to the value of BOR_TH bits.
OPTBL	**OPTBL[15:0]**: This option is checked by the boot ROM code after reset. Depending on content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 bootloader user manual for more details.

In the following table, data is based on characterization results, unless otherwise specified.

Table 23. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions (1)(2)		Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	T_A = -40 °C to 25 °C	0.9	2.1	µA
			T_A = 55 °C	1.2	3	
			T_A = 85 °C	1.5	3.4	
			T_A = 105 °C	2.6	6.6	
			T_A = 125 °C	5.1	12	
		LSE external clock (32.768 kHz) (3)	T_A = -40 °C to 25 °C	0.5	1.2	
			T_A = 55 °C	0.62	1.4	
			T_A = 85 °C	0.88	2.1	
			T_A = 105 °C	2.1	4.85	
			T_A = 125 °C	4.8	11	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	2.4	-	mA
$t_{WU\_HSI(AH)}$ (4)(5)	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	4.7	7	µs
$t_{WU\_LSI(AH)}$ (4) (5)	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	150	-	µs

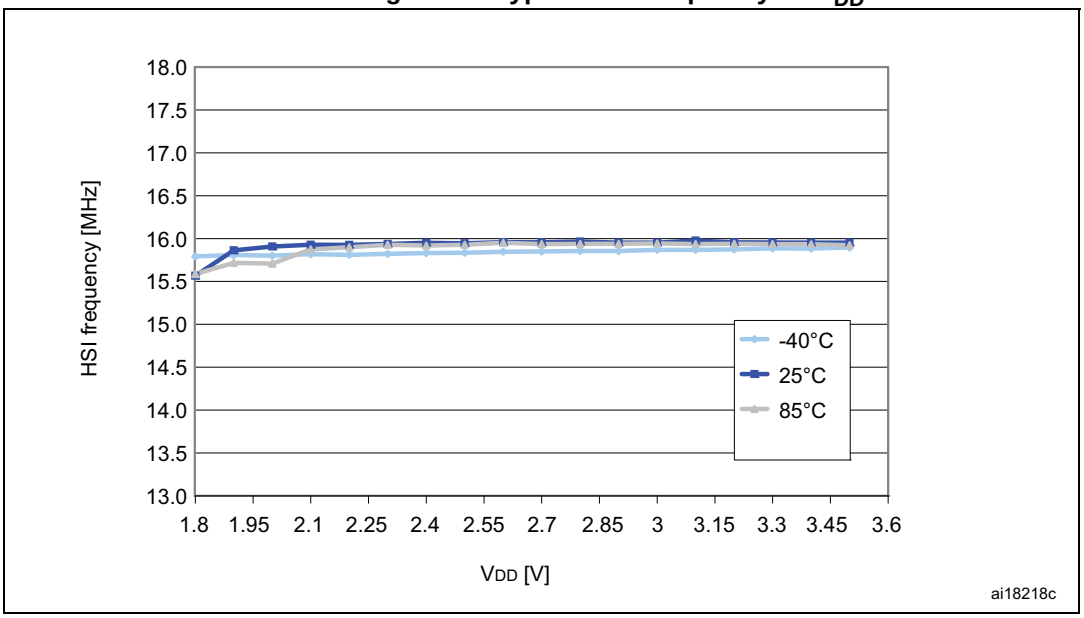
1. No floating I/O, unless otherwise specified.
2. T_A > 85 °C is valid only for devices with suffix 3 temperature range.
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 31*
4. Wakeup time until start of interrupt vector fetch.
The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}.
5. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

Table 24. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal

Symbol	Parameter	Condition(1)		Typ	Unit
$I_{DD(AH)}$ (2)	Supply current in Active-halt mode	V_{DD} = 1.8 V	LSE	1.15	µA
			LSE/32(3)	1.05	
		V_{DD} = 3 V	LSE	1.30	
			LSE/32(3)	1.20	
		V_{DD} = 3.6 V	LSE	1.45	
			LSE/32(3)	1.35	

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

Figure 18. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

In the following table, data is based on characterization results, not tested in production.

Table 33. LSI oscillator characteristics

Symbol	Parameter (1)	Conditions(1)	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	200(2)	µs
$I_{DD(LSI)}$	LSI oscillator frequency drift(3)	0 °C ≤ T_A ≤ 85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. This is a deviation for an individual part, once the initial frequency has been measured.

9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 35. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1 or 64 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 64 bytes (block) write cycles (on erased byte)	-	-	3	-	ms
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-	0.7	-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +85 °C (3 and 6 suffix)	T_{RET} = +85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +85 °C (3 and 6 suffix)	T_{RET} = +85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A= –40 to +125 °C (3 suffix)	T_{RET} = +125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A = –40 to +85 °C (3 and 6 suffix), T_A = –40 to +105 °C (3 suffix) or T_A = –40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

1. Data based on characterization results, not tested in production.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Table 48. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time	V_{AIN} on PF0 fast channel V_{DDA} < 2.4 V	0.43(4)(5)	-	-	µs
		V_{AIN} on PF0 fast channel 2.4 V ≤ V_{DDA}≤ 3.6 V	0.22(4)(5)	-	-	µs
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(4)(5)	-	-	µs
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.41(4)(5)	-	-	µs
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC1}$
		16 MHz	1(4)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(6)	Time before a new conversion	T_A = +25 °C	-	-	1(7)	s
		T_A = +70 °C	-	-	20(7)	ms
		T_A = +125 °C	-	-	2(7)	ms
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 44*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} or V_{DDA} must be tied to ground.
3. Guaranteed by design, not tested in production.
4. Minimum sampling and conversion time is reached for maximum Rext = 0.5 kΩ.
5. Value obtained for continuous conversion on fast channel.
6. The time between 2 conversions, or between ADC1 ON and the first conversion must be lower than t_{IDLE}.
7. The t_{IDLE} maximum value is ∞ on the “Z” revision code of the device.

Figure 41. Max. dynamic current consumption on V_{REF+} supply pin during ADC conversion

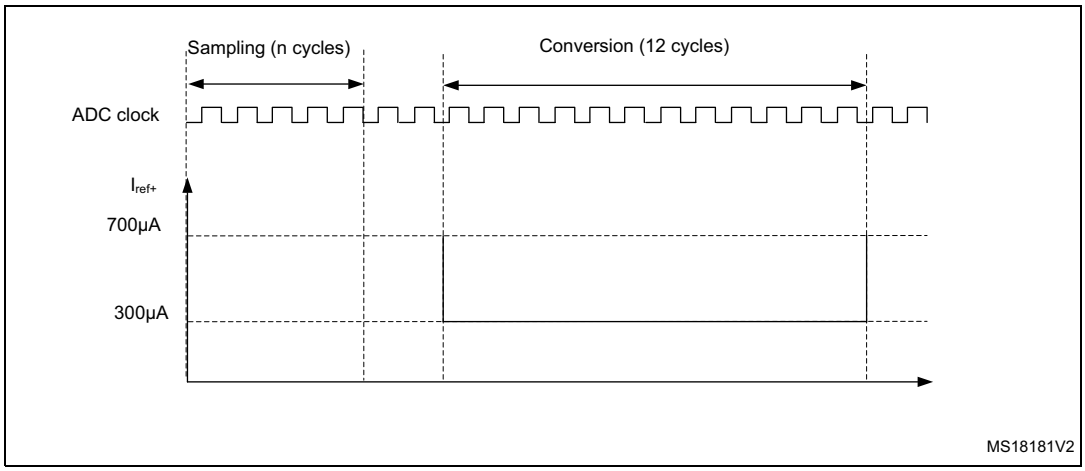


Table 52. R_{AIN} max for f_{ADC} = 16 MHz

t_S (cycles)	t_S (µs)	R_{AIN} max (kohm)			
		Slow channels		Fast channels	
		2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.3 V	1.8 V < V_{DDA} < 2.4 V
4	0.25	Not allowed	Not allowed	0.7	Not allowed
9	0.5625	0.8	Not allowed	2.0	1.0
16	1	2.0	0.8	4.0	3.0
24	1.5	3.0	1.8	6.0	4.5
48	3	6.8	4.0	15.0	10.0
96	6	15.0	10.0	30.0	20.0
192	12	32.0	25.0	50.0	40.0
384	24	50.0	50.0	50.0	50.0

9.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

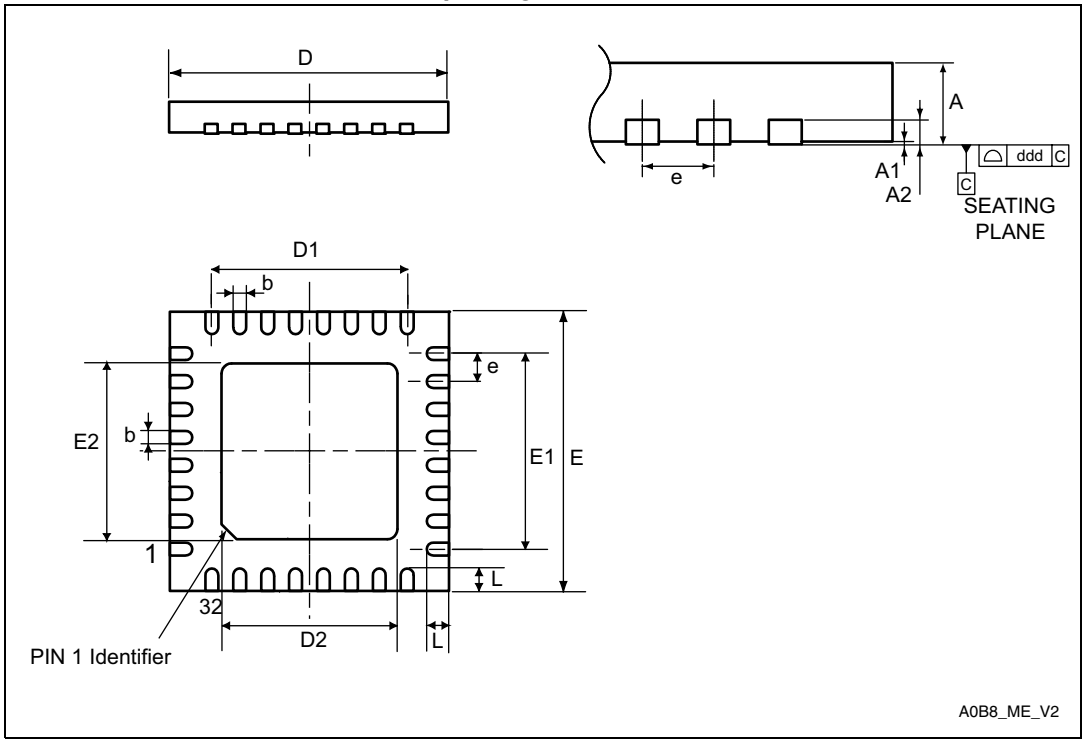
Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

10.3 UFQFPN32 package information

Figure 45. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

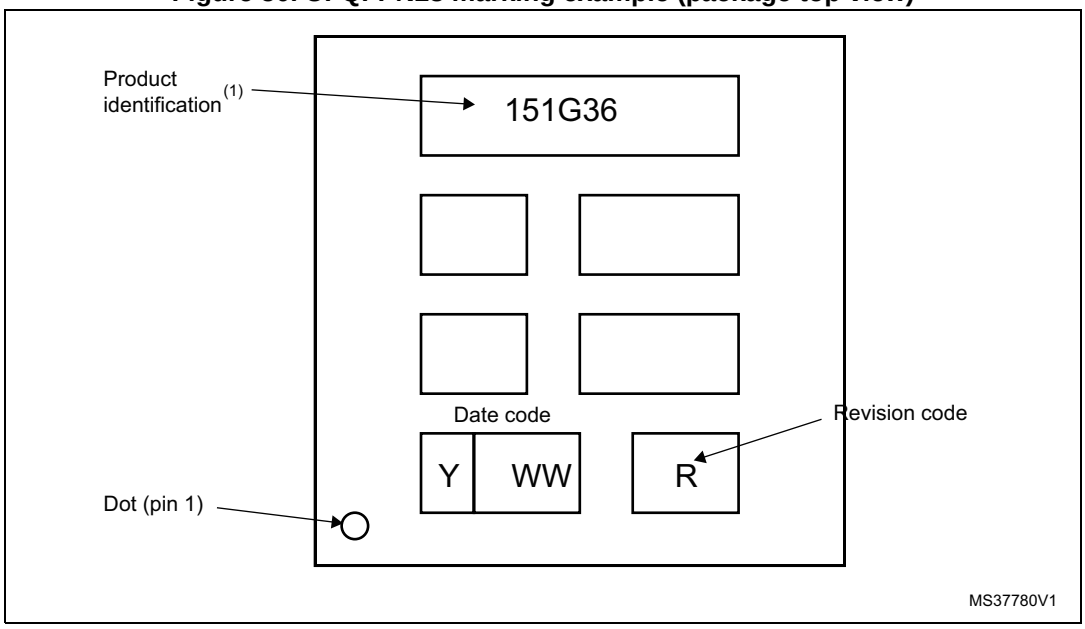


1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

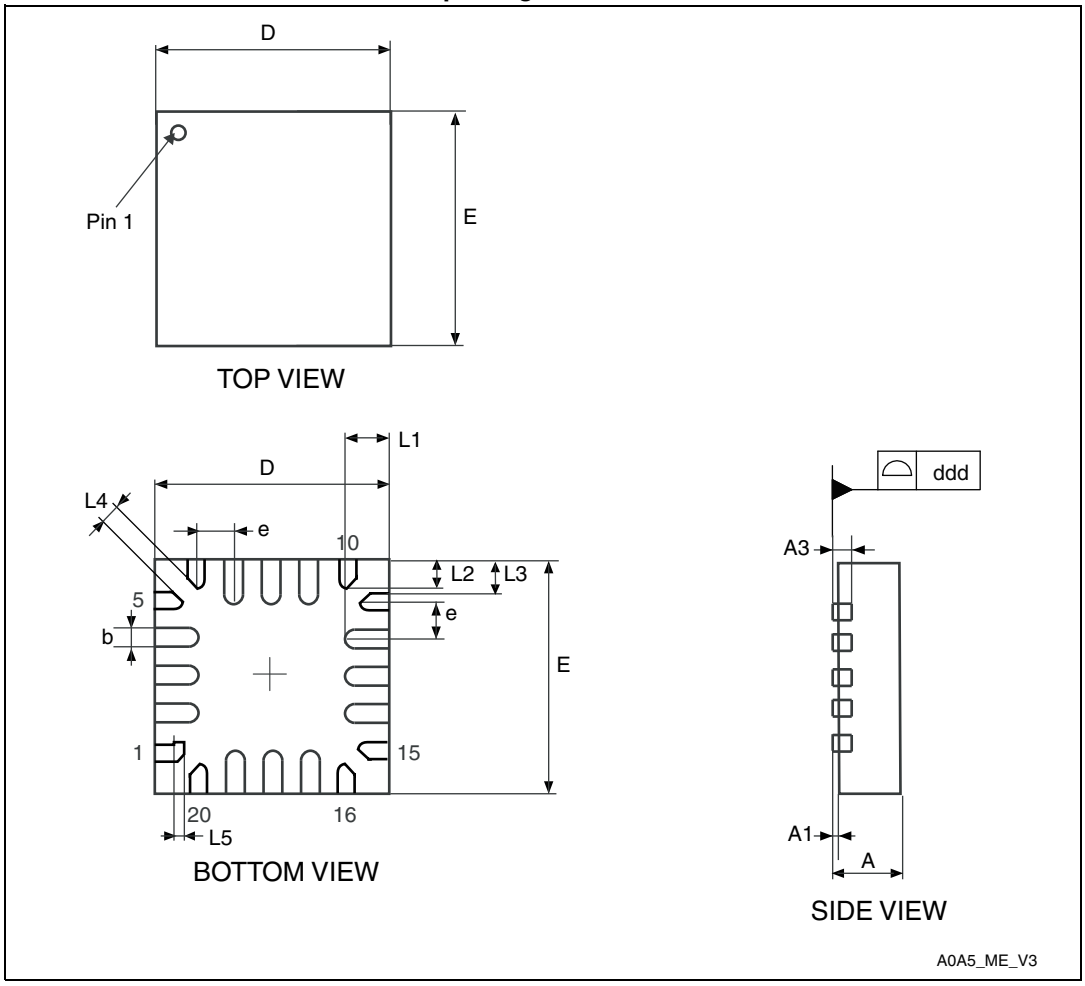
Figure 50. UFQFPN28 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.5 UFQFPN20 package information

Figure 51. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



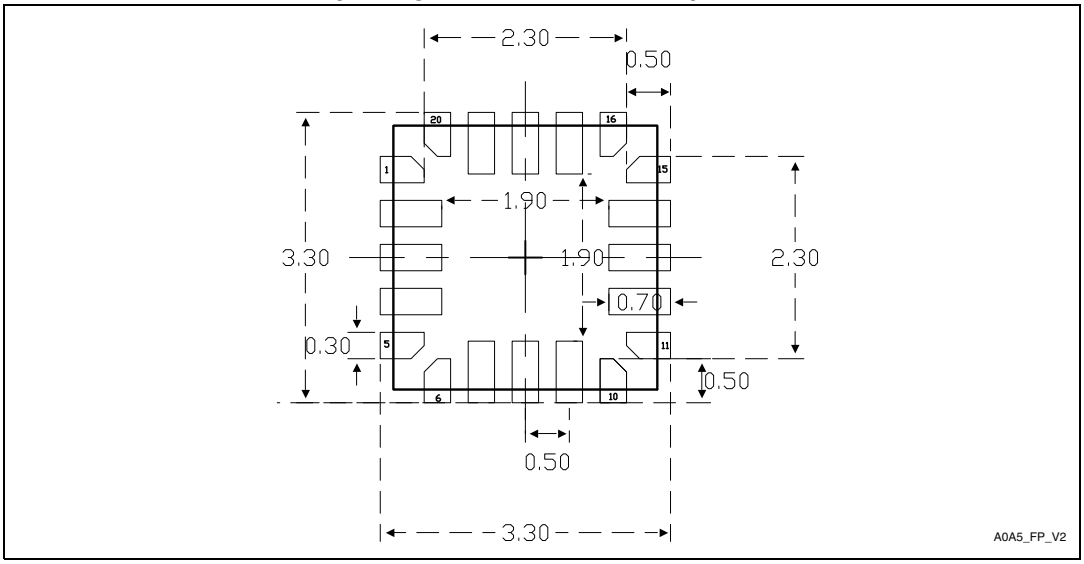
1. Drawing is not to scale.

Table 60. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-		0.0148	
L4	-	0.200	-		0.0079	
L5	-	0.150	-		0.0059	
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

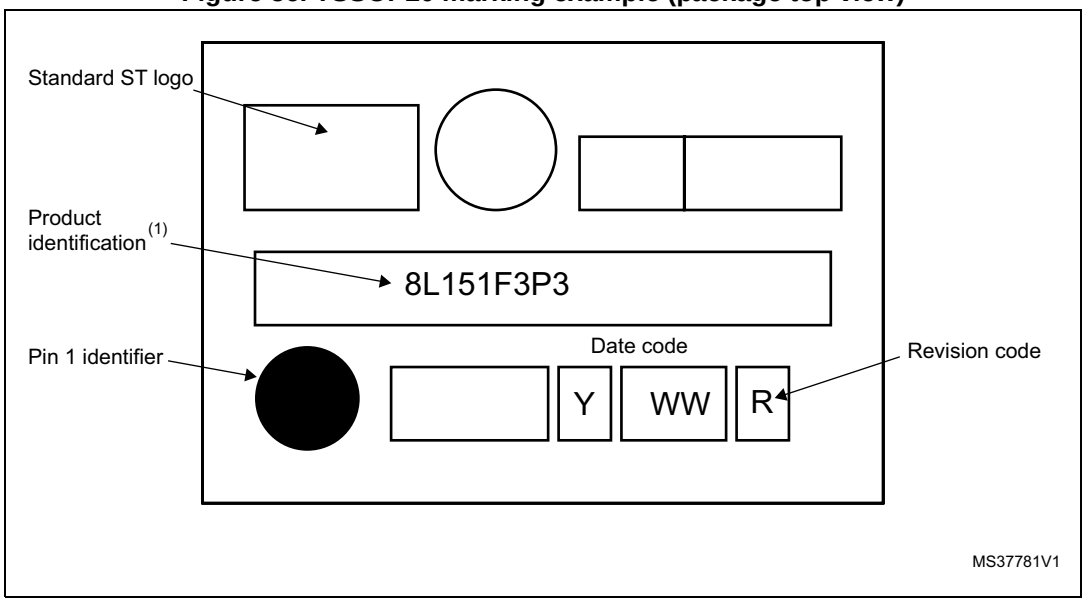


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 56. TSSOP20 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

12 Revision history

Table 64. Document revision history

Date	Revision	Changes
08-Jun-2011	1	Initial release
02-Sep-2011	2	Modified *Figure: Memory map.* Modified OPT1 description in *Table: Option byte addresses.* Modified t_{prog} in *Table: Flash program and data EEPROM memory.* Modified *Figure: Recommended NRST pin configuration.* Modified L2 in *Figure: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.* Replaced PM0051 with PM0054 and UM0320 with UM0470.
09-Feb-2012	3	Added part number STM8L151C2. Updated the captions of *Figure 3* and *Figure 4*. *Table: Low-density STM8L151x2/3 pin description*: updated OD column of NRST/PA1 pin. *Figure: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline:* removed the line over A1. *Figure Recommended UFQFPN28 footprint (dimensions in mm):* updated title. *Table: TSSOP20 - 20-pin thin shrink small outline package mechanical data:* updated title.
06-Jul-2012	4	Added “I/O level” in *Table: Legend/abbreviation for table 4* and *Table: Low-density STM8L151x2/3 pin description.* Updated *Figure: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3).* Updated *Figure: SPI1 timing diagram - master mode.* Updated *Table: Voltage characteristics* and *Table: I/O static characteristics.*
11-Apr-2014	5	Updated *Table: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3x3) package mechanical data,* added notes on *Table: TSSOP20 - 20-pin thin shrink small outline package mechanical data.* Changed reset value of SYSCFG_RMPCR1 register on *Table: General hardware register map.* Updated *Table: Low-density STM8L151x2/3 pin description* and *Table: Embedded reset and power control block characteristics.*