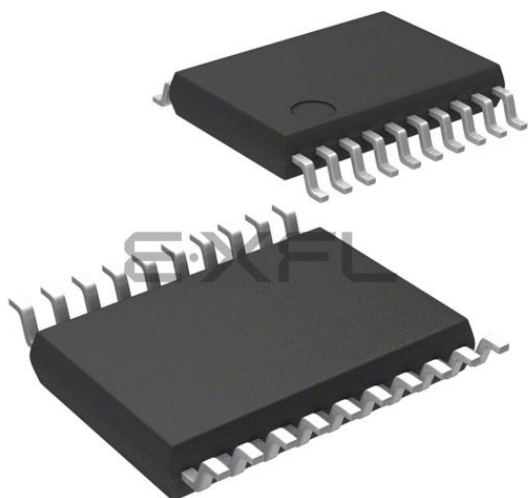




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Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151f3p6tr

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2.1 Device overview

Table 1. Low-density STM8L151x2/3 low power device features and peripheral counts

Features		STM8L151F3	STM8L151G3	STM8L151K3/ STM8L151C3	STM8L151F2	STM8L151G2	STM8L151K2/ STM8L151C2
Flash (Kbyte)		8			4		
Data EEPROM (byte)		256					
RAM (Kbyte)		1					
Timers	Basic	1 (8-bit)					
	General purpose	2 (16-bit)					
Commun- ication interfaces	SPI	1					
	I2C	1					
	USART	1					
GPIOs		18 ⁽¹⁾	26 ⁽¹⁾	30 ⁽²⁾ /41 ⁽¹⁾⁽²⁾	18 ⁽¹⁾	26 ⁽¹⁾	30 ⁽²⁾ /41 ⁽¹⁾⁽²⁾
12-bit synchronized ADC (number of channels)		1 (10)	1 (18)	1 (23/28) ⁽³⁾	1 (10)	1 (18)	1 (23/28) ⁽³⁾
Comparators (COMP1/COMP2)		2					
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR 1.65 to 3.6 V without BOR					
Operating temperature		– 40 to +85 °C / – 40 to +125 °C					
Packages		TSSOP20 UFQFPN20	UFQFPN28	UFQFPN32 LQFP48	TSSOP20 UFQFPN20	UFQFPN28	UFQFPN32 LQFP48

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).
2. 26 GPIOs in the STM8L151K3 and 40 GPIOs in the STM8L151C3.
3. 22 channels in the STM8L151K3 and 28 channels in the STM8L151C3.

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1} ; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1} .
- V_{SSA} ; V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1} , respectively.
- V_{SS2} ; V_{DD2} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1} , respectively.
- V_{REF+} ; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The low-density STM8L151x2/3 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

Table 7. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xFF
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xFF
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xFF
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xFF
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 8. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (44 byte)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH_PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH_DUKR	Flash data EEPROM unprotection key register	0x00
0x00 5054		FLASH_IAPSR	Flash in-application programming status register	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5055 to 0x00 506F	Reserved area (27 byte)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074		Reserved area (3 byte)		
0x00 5075		DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E		Reserved area (2 byte)		
0x00 507F		DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C0	CLK	CLK_CKDIVR	CLK clock master divider register	0x03
0x00 50C1		CLK_CRTCR	CLK clock RTC register	0x00 ⁽²⁾
0x00 50C2		CLK_I CKCR	CLK internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	CLK peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	CLK peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	CLK configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	CLK external clock control register	0x00
0x00 50C7		CLK_SCSR	CLK system clock status register	0x01
0x00 50C8		CLK_SWR	CLK system clock switch register	0x01
0x00 50C9		CLK_SWCR	CLK clock switch control register	0xX0
0x00 50CA		CLK_CSSR	CLK clock security system register	0x00
0x00 50CB		CLK_CBEEPR	CLK clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	CLK HSI calibration register	0xXX
0x00 50CD		CLK_HSI TRIMR	CLK HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	CLK HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	CLK main regulator control status register	0bxx11 100X
0x00 50D0		CLK_PCKENR3	CLK peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 byte)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDG window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0x01
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 byte)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to 0x00 513F	Reserved area (76 byte)			

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_DER	TIM4 DMA1 request enable register	0x00
0x00 52E4		TIM4_IER	TIM4 Interrupt enable register	0x00
0x00 52E5		TIM4_SR1	TIM4 status register 1	0x00
0x00 52E6		TIM4_EGR	TIM4 Event generation register	0x00
0x00 52E7		TIM4_CNTR	TIM4 counter	0x00
0x00 52E8		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E9		TIM4_ARR	TIM4 Auto-reload register	0x00
0x00 52EA to 0x00 52FE	Reserved area (21 byte)			
0x00 52FF	IRTIM	IR_CR	Infrared control register	0x00
0x00 5317 to 0x00 533F	Reserved area (41 byte)			
0x00 5340	ADC1	ADC1_CR1	ADC1 configuration register 1	0x00
0x00 5341		ADC1_CR2	ADC1 configuration register 2	0x00
0x00 5342		ADC1_CR3	ADC1 configuration register 3	0x1F
0x00 5343		ADC1_SR	ADC1 status register	0x00
0x00 5344		ADC1_DRH	ADC1 data register high	0x00
0x00 5345		ADC1_DRL	ADC1 data register low	0x00
0x00 5346		ADC1_HTRH	ADC1 high threshold register high	0x0F
0x00 5347		ADC1_HTRL	ADC1 high threshold register low	0xFF
0x00 5348		ADC1_LTRH	ADC1 low threshold register high	0x00
0x00 5349		ADC1_LTRL	ADC1 low threshold register low	0x00
0x00 534A		ADC1_SQR1	ADC1 channel sequence 1 register	0x00
0x00 534B		ADC1_SQR2	ADC1 channel sequence 2 register	0x00
0x00 534C		ADC1_SQR3	ADC1 channel sequence 3 register	0x00
0x00 534D		ADC1_SQR4	ADC1 channel sequence 4 register	0x00
0x00 534E		ADC1_TRIGR1	ADC1 trigger disable 1	0x00
0x00 534F		ADC1_TRIGR2	ADC1 trigger disable 2	0x00
0x00 5350		ADC1_TRIGR3	ADC1 trigger disable 3	0x00
0x00 5351		ADC1_TRIGR4	ADC1 trigger disable 4	0x00

Table 12. Option byte description

Option byte No.	Option description
OPT0	ROP[7:0] Memory readout protection (ROP) 0xAA: Disable readout protection (write access via SWIM protocol) Refer to Readout protection section in the STM8L15x and STM8L16x reference manual (RM0031).
OPT1	UBC[7:0] Size of the user boot code area 0x00: UBC is not protected. 0x01: Page 0 is write protected. 0x02: Page 0 and 1 reserved for the UBC and write protected. It covers only the interrupt vectors. 0x03: Page 0 to 2 reserved for UBC and write protected. 0x7F to 0xFF - All 128 pages reserved for UBC and write protected. The protection of the memory area not protected by the UBC is enabled through the MASS keys. Refer to User boot code section in the STM8L15x and STM8L16x reference manual (RM0031).
OPT2	Reserved
OPT3	IWDG_HW : Independent watchdog 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT : Independent window watchdog off on Halt/Active-halt 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode
	WWDG_HW : Window watchdog 0: Window watchdog activated by software 1: Window watchdog activated by hardware
	WWDG_HALT : Window window watchdog reset on Halt/Active-halt 0: Window watchdog stopped in Halt mode 1: Window watchdog generates a reset when MCU enters Halt mode
OPT4	HSECNT : Number of HSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles
	LSECNT : Number of LSE oscillator stabilization clock cycles 0x00 - 1 clock cycle 0x01 - 16 clock cycles 0x10 - 512 clock cycles 0x11 - 4096 clock cycles Refer to Table 31: LSE oscillator characteristics on page 74 .

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 13. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_A \text{ max}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics is indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\Sigma$).

9.1.2 Typical values

Unless otherwise specified, typical data is based on $T_A = 25\text{ °C}$, $V_{DD} = 3\text{ V}$. It is given only as design guidelines and is not tested.

Typical ADC1 accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\Sigma$).

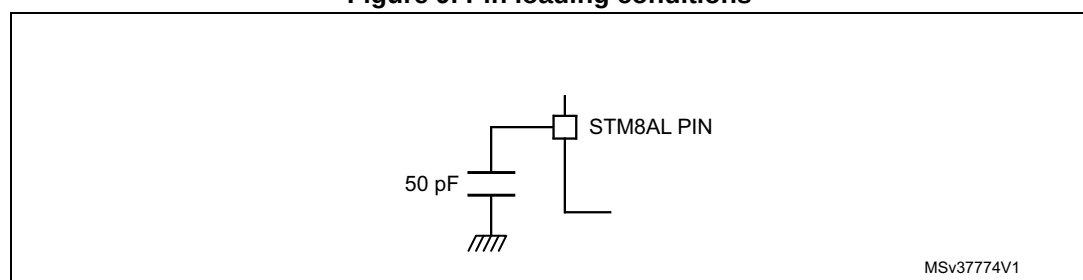
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

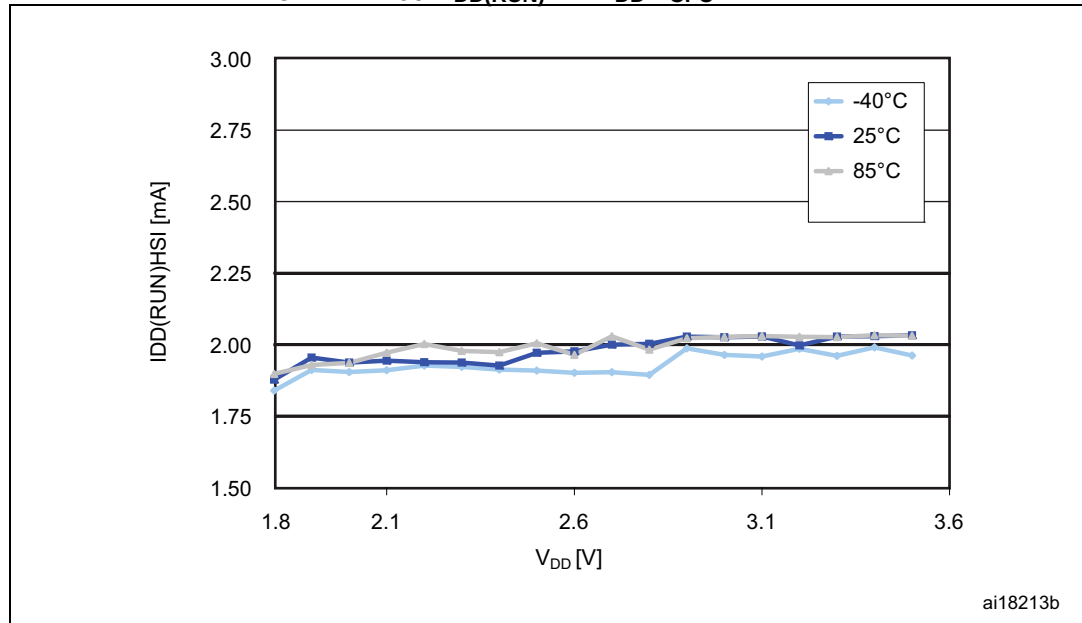
The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

Figure 9. Pin loading conditions



4. The run from RAM consumption can be approximated with the linear formula:
 $I_{DD}(\text{run_from_RAM}) = \text{Freq} \times 90 \mu\text{A/MHz} + 380 \mu\text{A}$
5. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD \text{ HSE}}$) must be added. Refer to [Table 30](#).
6. Tested in production.
7. The run from Flash consumption can be approximated with the linear formula:
 $I_{DD}(\text{run_from_Flash}) = \text{Freq} \times 195 \mu\text{A/MHz} + 440 \mu\text{A}$
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD \text{ LSE}}$) must be added. Refer to [Table 31](#).

Figure 12. Typ. $I_{DD}(\text{RUN})$ vs. V_{DD} , $f_{\text{CPU}} = 16 \text{ MHz}$



1. Typical current consumption measured with code executed from RAM

Figure 22. Typical pull-up resistance R_{PU} vs V_{DD} with $V_{IN}=V_{SS}$

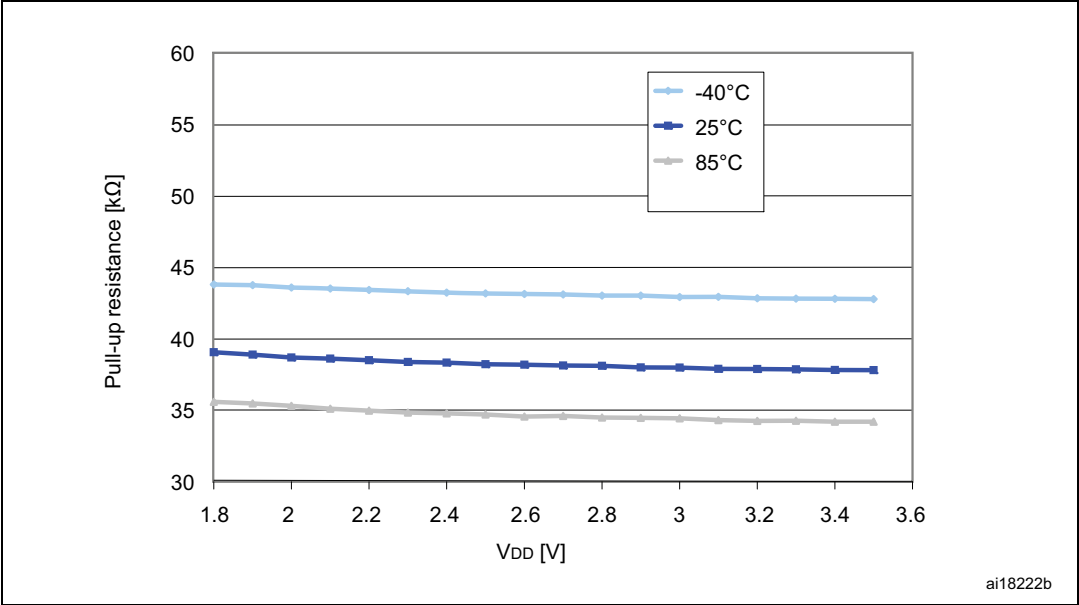
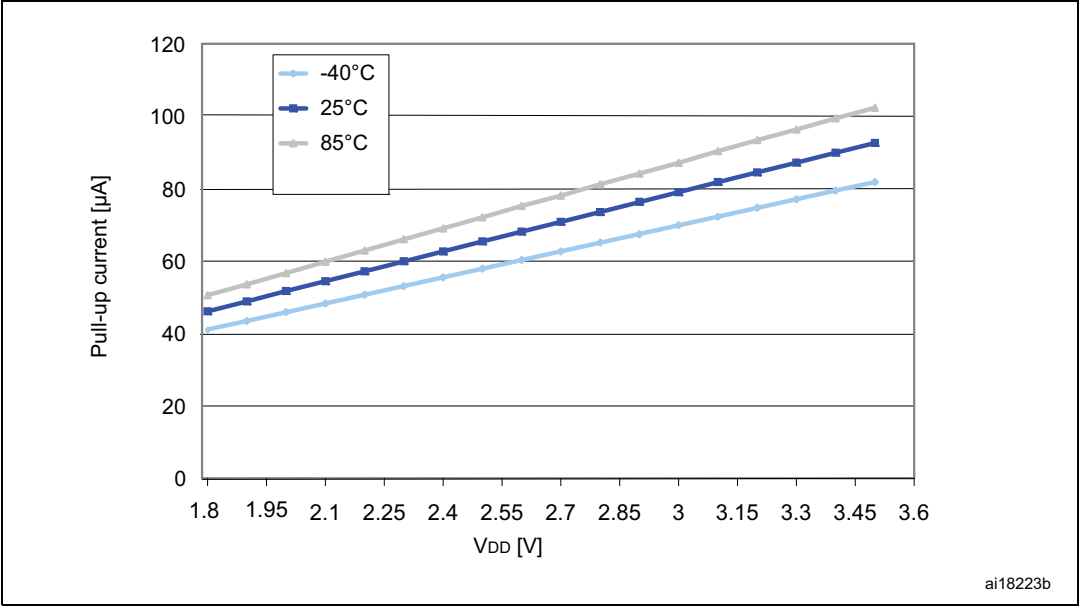


Figure 23. Typical pull-up current I_{PU} vs V_{DD} with $V_{IN}=V_{SS}$



Output driving current

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 38. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
High sink	$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +2 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	-	0.45	V
			$I_{IO} = +2 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$	-	0.45	V
			$I_{IO} = +10 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	-	0.7	V
	$V_{OH}^{(2)}$	Output high level voltage for an I/O pin	$I_{IO} = -2 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	$V_{DD}-0.45$	-	V
			$I_{IO} = -1 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$	$V_{DD}-0.45$	-	V
			$I_{IO} = -10 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	$V_{DD}-0.7$	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .

Table 39. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
Open drain	$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +3 \text{ mA}$, $V_{DD} = 3.0 \text{ V}$	-	0.45	V
			$I_{IO} = +1 \text{ mA}$, $V_{DD} = 1.8 \text{ V}$	-	0.45	

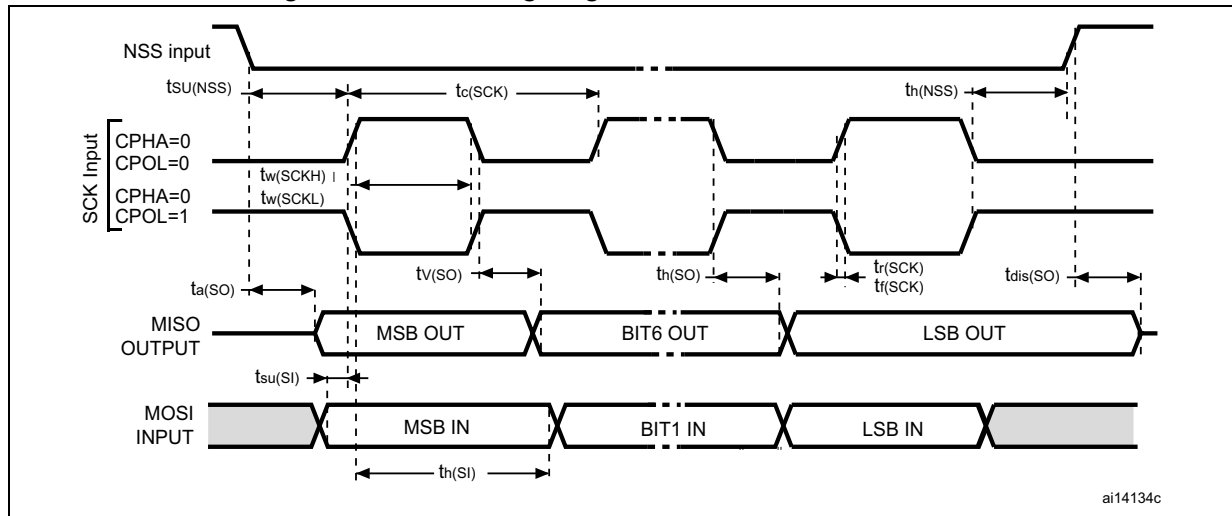
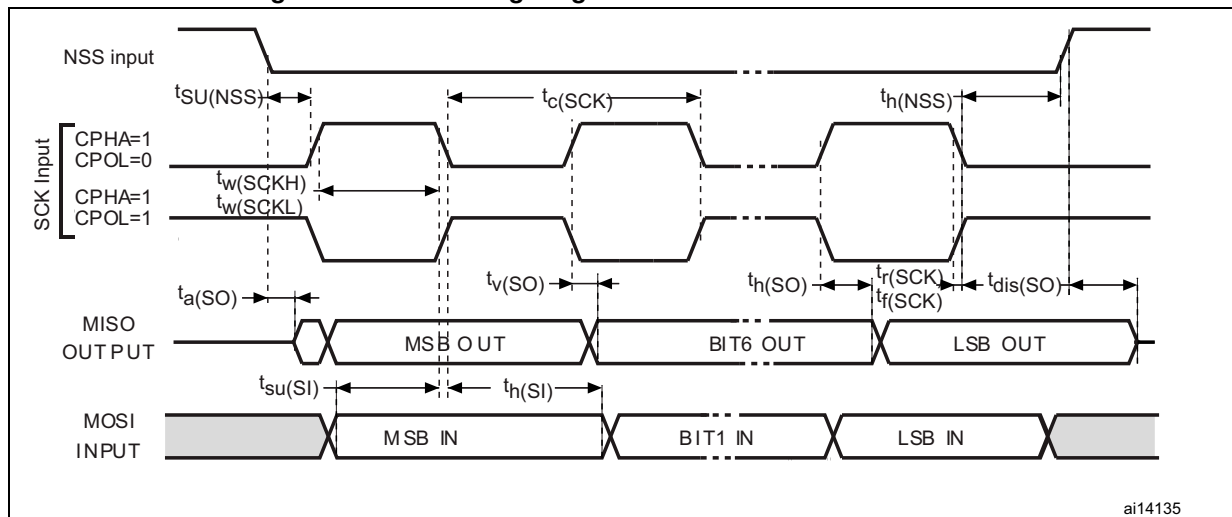
1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .

Table 40. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min	Max	Unit
$\overline{R}$	$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$, $V_{DD} = 2.0 \text{ V}$	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .

Figure 33. SPI1 timing diagram - slave mode and CPHA=0

Figure 34. SPI1 timing diagram - slave mode and CPHA=1⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

In the following table, data is guaranteed by design, not tested in production.

Table 47. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
T_A	Temperature range	-	-40	-	125	°C
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	μs
		Slow mode	-	20	25	
$t_{d \text{ slow}}$	Propagation delay in slow mode ⁽²⁾	$1.65 \text{ V} \leq V_{DDA} \leq 2.7 \text{ V}$	-	1.8	3.5	
		$2.7 \text{ V} \leq V_{DDA} \leq 3.6 \text{ V}$	-	2.5	6	
$t_{d \text{ fast}}$	Propagation delay in fast mode ⁽²⁾	$1.65 \text{ V} \leq V_{DDA} \leq 2.7 \text{ V}$	-	0.8	2	
		$2.7 \text{ V} \leq V_{DDA} \leq 3.6 \text{ V}$	-	1.2	4	
V_{offset}	Comparator offset error	-	-	± 4	± 20	mV
I_{COMP2}	Current consumption ⁽³⁾	Fast mode	-	3.5	5	μA
		Slow mode	-	0.5	2	

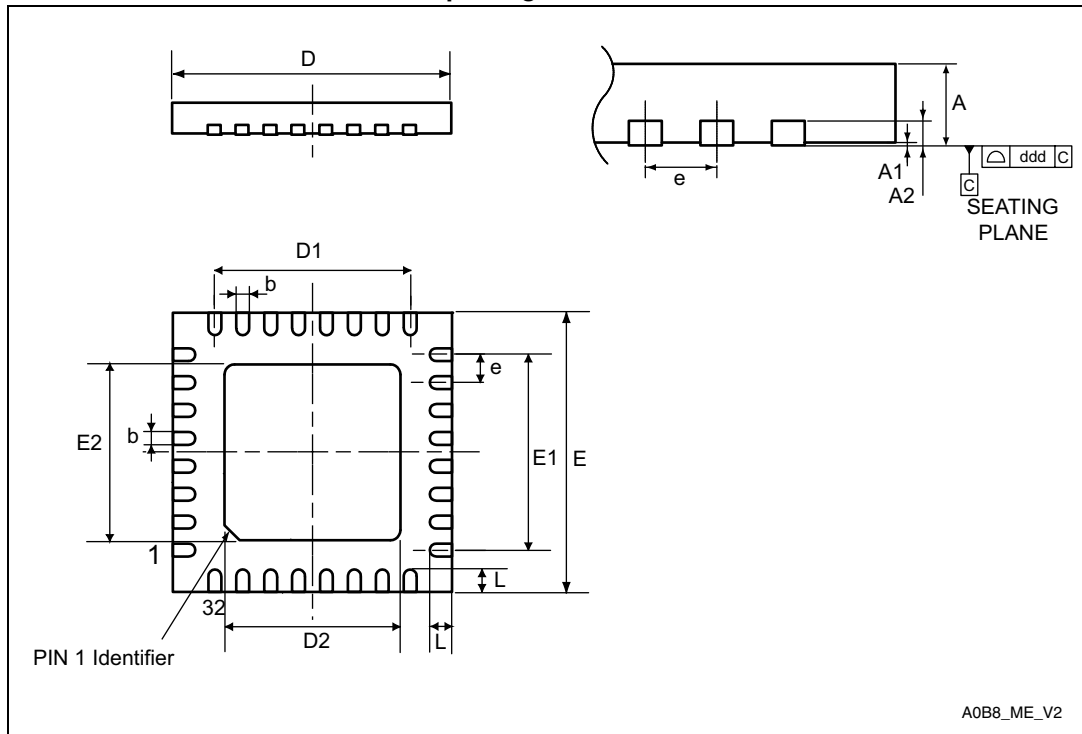
1. Based on characterization, not tested in production.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage not included.

10.3 UFQFPN32 package information

Figure 45. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

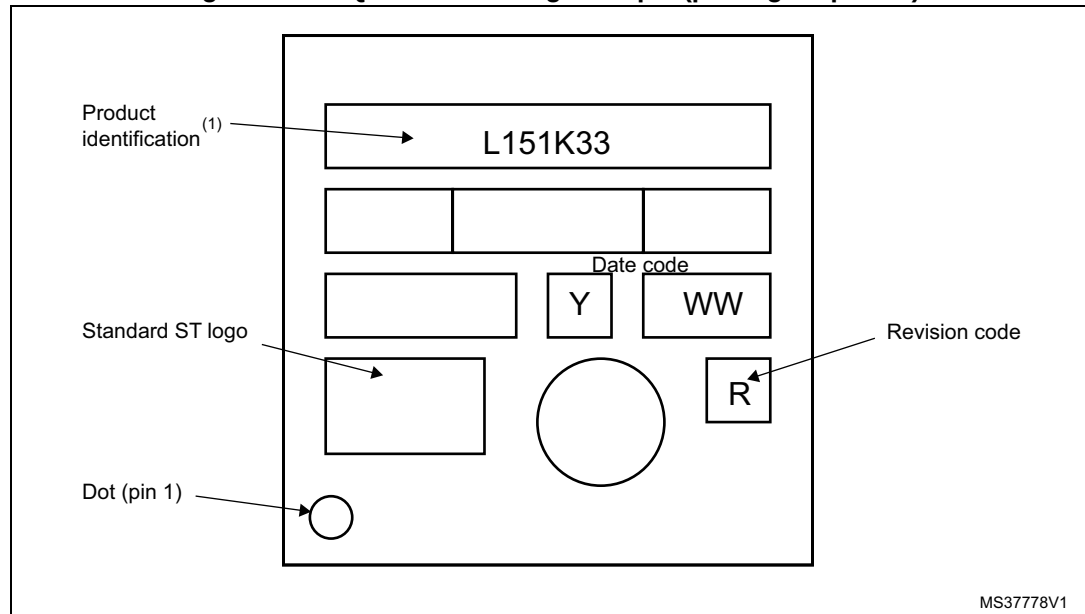


1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 47. UFQFPN32 marking example (package top view)

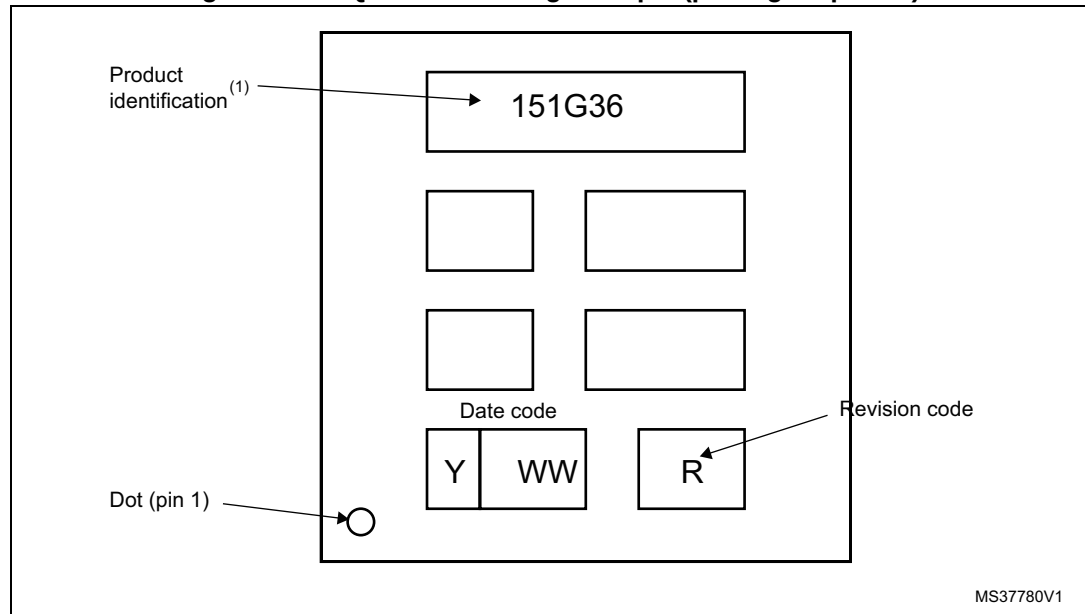


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 50. UFQFPN28 marking example (package top view)

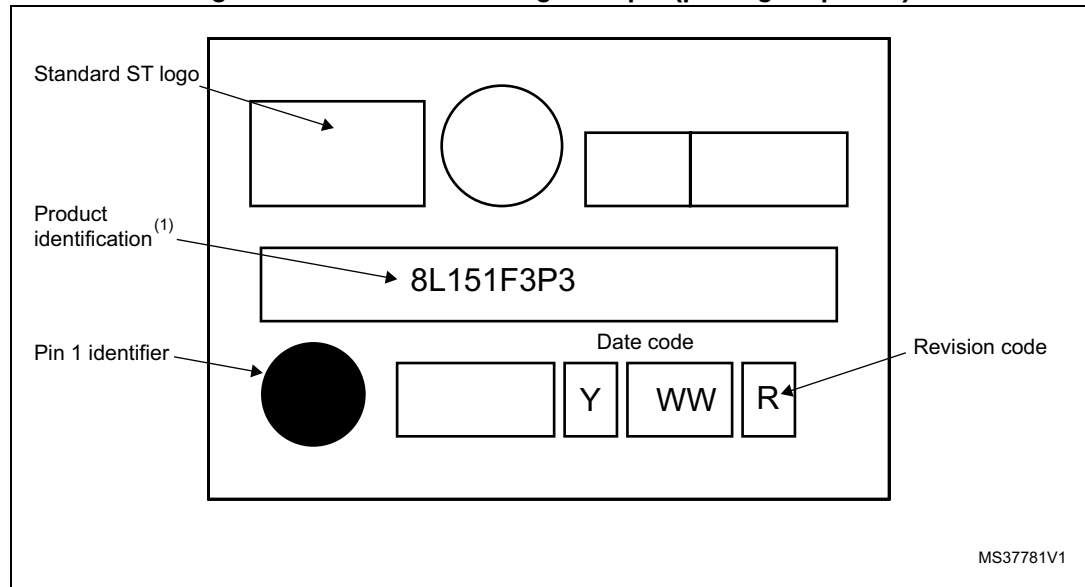


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 56. TSSOP20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.