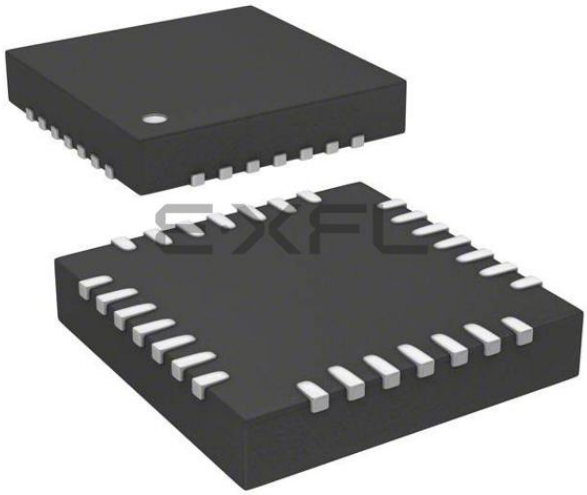

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, POR, PWM, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l151g2u6

Contents

2.1 Device overview

Table 1. Low-density STM8L151x2/3 low power device features and peripheral counts

Features		STM8L151F3	STM8L151G3	STM8L151K3/ STM8L151C3	STM8L151F2	STM8L151G2	STM8L151K2/ STM8L151C2
Flash (Kbyte)		8			4		
Data EEPROM (byte)		256					
RAM (Kbyte)		1					
Timers	Basic	1 (8-bit)					
	General purpose	2 (16-bit)					
Commun-ication interfaces	SPI	1					
	I2C	1					
	USART	1					
GPIOs		18 (1)	26 (1)	30(2)/41(1)(2)	18 (1)	26 (1)	30(2)/41(1)(2)
12-bit synchronized ADC (number of channels)		1 (10)	1 (18)	1 (23/28)(3)	1 (10)	1 (18)	1 (23/28)(3)
Comparators (COMP1/COMP2)		2					
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR 1.65 to 3.6 V without BOR					
Operating temperature		– 40 to +85 °C / – 40 to +125 °C					
Packages		TSSOP20 UFQFPN20	UFQFPN28	UFQFPN32 LQFP48	TSSOP20 UFQFPN20	UFQFPN28	UFQFPN32 LQFP48

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).
2. 26 GPIOs in the STM8L151K3 and 40 GPIOs in the STM8L151C3.
3. 22 channels in the STM8L151K3 and 28 channels in the STM8L151C3.

3.1 Low-power modes

The low-density STM8L151x2/3 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 20*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 21*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 22*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 23* and *Table 24*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 25*.

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

3.6 Memories

The low-density STM8L151x2/3 devices have the following main features:

- Up to 1 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 8 Kbyte of low-density embedded Flash program memory
  - 256 byte of data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature.

The option byte protects part of the Flash program memory from write and readout piracy.

3.7 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, I2C1, SPI1, USART1, the three Timers.

3.8 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.9 Ultra-low-power comparators

The low-density STM8L151x2/3 embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - External I/O
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.17 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The single-wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

The low-density STM8L151x2/3 ultra-low-power devices feature a built-in bootloader (see *UM0560: STM8 bootloader user manual*).

The bootloader is used to download application software into the device memories, including RAM, program and data memory, using standard serial interfaces. It is a complementary solution to programming via the SWIM debugging interface.

Table 4. Low-density STM8L151x2/3 pin description (continued)

Pin number					Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP48	UFQFPN32	UFQFPN28	UFQFPN20	TSSOP20				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
34	22	-	-	-	PD5/ ADC1_IN9/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port D5**	ADC1_IN9/ Comparator1 positive input
35	23	-	-	-	*PD6/ADC1_IN8/ RTC_CALIB/ COMP1_INP*	I/O	-	**X**	X	X	HS	X	X	**Port D6**	ADC1_IN8 / RTC calibration/ Comparator1 positive input
36	24	-	-	-	PD7 /ADC1_IN7/ RTC_ALARM/ COMP1_INP	I/O	-	**X**	X	X	HS	X	X	**Port D7**	ADC1_IN7/RTC alarm/ Comparator1 positive input
14	-	-	-	-	PE0	I/O	-	**X**	X	X	HS	X	X	**Port E0**	-
15	-	-	-	-	PE1	I/O	-	**X**	X	X	HS	X	X	**Port E1**	-
16	-	-	-	-	PE2	I/O	-	**X**	X	X	HS	X	X	**Port E2**	-
17	-	-	-	-	PE3/ADC1_IN26	I/O	-	**X**	X	X	HS	X	X	**Port E3**	ADC1_IN26
18	-	-	-	-	PE4/ADC1_IN27	I/O	-	**X**	X	X	HS	X	X	**Port E4**	ADC1_IN27
19	-	-	-	-	PE5/ADC1_IN23/ COMP1_INP/ COMP2_INP	I/O	-	**X**	X	X	HS	X	X	**Port E5**	ADC1_IN23/ Comparator 1 positive input/Comparator 2 positive input
47	-	-	-	-	PE6/PVD_IN	I/O	-	**X**	X	X	HS	X	X	**Port E6**	PVD_IN
48	-	-	-	-	PE7/ADC1_IN25	I/O	-	**X**	X	X	HS	X	X	**Port E7**	ADC1_IN25
32	-	-	-	-	PF0/ADC1_IN24	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24
10	-	-	-	-	V_{DD}	S	-	-	-	-	-	-	-	Digital supply voltage	
-	8	7	5	8	V_{DD} /V_{DDA} / V_{REF+}	S	-	-	-	-	-	-	-	Digital supply voltage / ADC1 positive voltage reference	
9	7	6	4	7	V_{SS} / V_{REF-} / V_{SSA}	S	-	-	-	-	-	-	-	Ground voltage / ADC1 negative voltage reference / Analog ground voltage	
11	-	-	-	-	V_{DDA}	S	-	-	-	-	-	-	-	Analog supply voltage	
12	-	-	-	-	V_{REF+}	S	-	-	-	-	-	-	-	ADC1 positive voltage reference	
1	32	28	20	3	PA0(8)/*[USART_CK]*(2) / SWIM/BEEP/IR_TIM (9)	I/O		X	**X**	X	HS (9)	X	X	**Port A0**	*[USART1 synchronous clock]*(2) / SWIM input and output / Beep output / Infrared Timer output

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5140	RTC	RTC_TR1	RTC time register 1	0x00
0x00 5141		RTC_TR2	RTC time register 2	0x00
0x00 5142		RTC_TR3	RTC time register 3	0x00
0x00 5143		Reserved area (1 byte)		
0x00 5144		RTC_DR1	RTC date register 1	0x01
0x00 5145		RTC_DR2	RTC date register 2	0x21
0x00 5146		RTC_DR3	RTC date register 3	0x00
0x00 5147		Reserved area (1 byte)		
0x00 5148		RTC_CR1	RTC control register 1	0x00(2)
0x00 5149		RTC_CR2	RTC control register 2	0x00(2)
0x00 514A		RTC_CR3	RTC control register 3	0x00(2)
0x00 514B		Reserved area (1 byte)		
0x00 514C		RTC_ISR1	RTC initialization and status register 1	0x01
0x00 514D		RTC_ISR2	RTC initialization and Status register 2	0x00
0x00 514E 0x00 514F		Reserved area (2 byte)		
0x00 5150		RTC_SPRERH	RTC synchronous prescaler register high	0x00(2)
0x00 5151		RTC_SPRERL	RTC synchronous prescaler register low	0xFF(2)
0x00 5152		RTC_APRER	RTC asynchronous prescaler register	0x7F(2)
0x00 5153		Reserved area (1 byte)		
0x00 5154		RTC_WUTRH	RTC wakeup timer register high	0xFF(2)
0x00 5155		RTC_WUTRL	RTC wakeup timer register low	0xFF(2)
0x00 5156		Reserved area (1 byte)		
0x00 5157		RTC_SSRL	RTC subsecond register low	0x00
0x00 5158		RTC_SSRH	RTC subsecond register high	0x00
0x00 5159		RTC_WPR	RTC write protection register	0x00
0x00 5158		RTC_SSRH	RTC subsecond register high	0x00
0x00 5159		RTC_WPR	RTC write protection register	0x00
0x00 515A		RTC_SHIFTRH	RTC shift register high	0x00
0x00 515B		RTC_SHIFTRL	RTC shift register low	0x00
0x00 515C		RTC_ALRMAR1	RTC alarm A register 1	0x00(2)
0x00 515D		RTC_ALRMAR2	RTC alarm A register 2	0x00(2)
0x00 515E		RTC_ALRMAR3	RTC alarm A register 3	0x00(2)
0x00 515F		RTC_ALRMAR4	RTC alarm A register 4	0x00(2)

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 11* for details on option byte addresses.

The option bytes can also be modified ‘on the fly’ by the application in IAP mode, except for the ROP and UBC values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 11. Option byte addresses

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x00 4800	Read-out protection (ROP)	OPT0	ROP[7:0]								0xAA
0x00 4802	UBC (User Boot code size)	OPT1	UBC[7:0]								0x00
0x00 4807	Reserved										0x00
0x00 4808	Independent watchdog option	OPT3 [3:0]	Reserved				WWDG_HALT	WWDG_HW	IWDG_HALT	IWDG_HW	0x00
0x00 4809	Number of stabilization clock cycles for HSE and LSE oscillators	OPT4	Reserved				LSECNT[1:0]		HSECNT[1:0]		0x00
0x00 480A	Brownout reset (BOR)	OPT5 [3:0]	Reserved				BOR_TH			BOR_ON	0x01
0x00 480B	Bootloader option bytes (OPTBL)	OPTBL [15:0]	OPTBL[15:0]								0x00
0x00 480C											0x00

In the following table, data is based on characterization results, unless otherwise specified.

Table 20. Total current consumption in Wait mode

Symbol	Parameter	Conditions(1)			Typ	Max				Unit
						55°C	85 °C	105 °C (2)	125 °C (2)	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode(3), V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.33	0.39	0.41	0.43	0.45	mA
				f_{CPU} = 1 MHz	0.35	0.41	0.44	0.45	0.48	
				f_{CPU} = 4 MHz	0.42	0.51	0.52	0.54	0.58	
				f_{CPU} = 8 MHz	0.52	0.57	0.58	0.59	0.62	
				f_{CPU} = 16 MHz	0.68	0.76	0.79	0.82 (5)	0.85 (5)	
			HSE external clock (f_{CPU}=f_{HSE}) (4)	f_{CPU} = 125 kHz	0.032	0.056	0.068	0.072	0.093	
				f_{CPU} = 1 MHz	0.078	0.121	0.144	0.163	0.197	
				f_{CPU} = 4 MHz	0.218	0.26	0.30	0.36	0.40	
				f_{CPU} = 8 MHz	0.40	0.52	0.57	0.62	0.66	
				f_{CPU} = 16 MHz	0.760	1.01	1.05	1.09 (5)	1.16 (5)	
			LSI	f_{CPU} = f_{LSI}	0.035	0.044	0.046	0.049	0.054	
			LSE(6) external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.032	0.036	0.038	0.044	0.051	

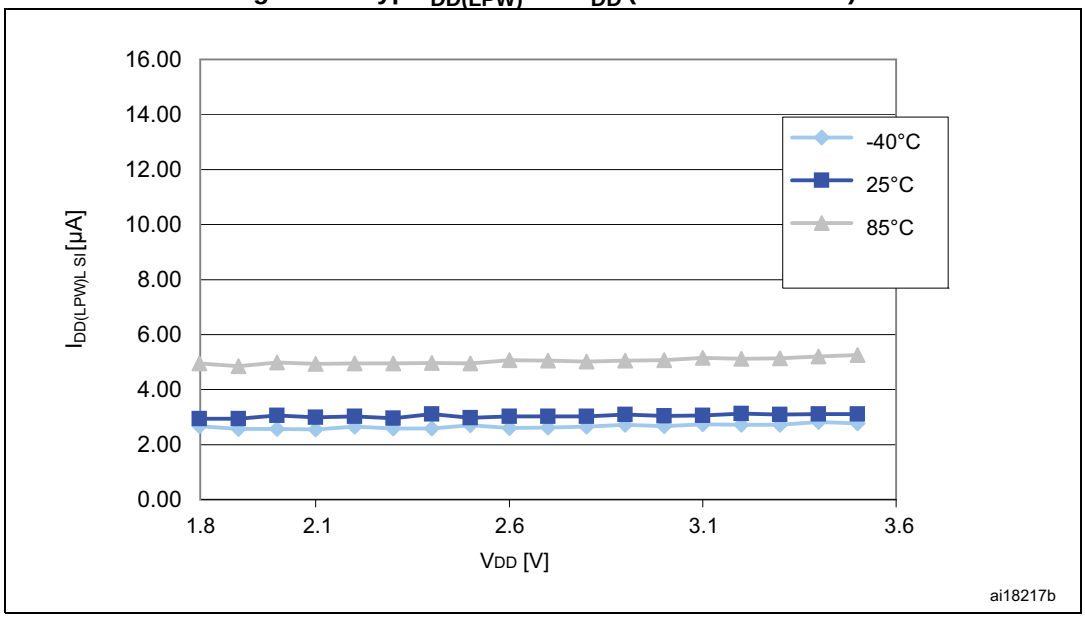
In the following table, data is based on characterization results, unless otherwise specified.

Table 21. Total current consumption and timing in Low power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1][2]			Typ	Max	Unit
$I_{DD(LPR)}$	Supply current in Low power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.1	5.4	µA
				T_A = 55 °C	5.7	6	
				T_A = 85 °C	6.8	7.5	
				T_A = 105 °C	9.2	10.4	
				T_A = 125 °C	13.4	16.6	
			with TIM2 active[3]	T_A = -40 °C to 25 °C	5.4	5.7	
				T_A = 55 °C	6.0	6.3	
				T_A = 85 °C	7.2	7.8	
				T_A = 105 °C	9.4	10.7	
				T_A = 125 °C	13.8	17	
		LSE [4] external clock (32.768 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.25	5.6	
				T_A = 55 °C	5.67	6.1	
				T_A = 85 °C	5.85	6.3	
				T_A = 105 °C	7.11	7.6	
				T_A = 125 °C	9.84	12	
			with TIM2 active [3]	T_A = -40 °C to 25 °C	5.59	6	
				T_A = 55 °C	6.10	6.4	
				T_A = 85 °C	6.30	7	
				T_A = 105 °C	7.55	8.4	
				T_A = 125 °C	10.1	15	

1. No floating I/Os
2. T_A > 85 °C is valid only for devices with suffix 3 temperature range.
3. Timer 2 clock enabled and counter running
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 31*

Figure 15. Typ. $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source)



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification),
C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 31. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	ΔV = 200 mV	-	1.2	-	MΩ
$C^{(1)}$	Recommended load capacitance (2)	-	-	8	-	pF
$I_{DD(LSE)}$	LSE oscillator power consumption	-	-	-	1.4(3)	µA
		V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3 V	-	600	-	
		V_{DD} = 3.6 V	-	750	-	
g_m	Oscillator transconductance	-	3(3)	-	-	µA/V
$t_{SU(LSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	s

1. C=C_{L1}=C_{L2} is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Data guaranteed by Design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

NRST pin

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis(3)	-	10%V_{DD} (2)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (1)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	

1. Data based on characterization results, not tested in production.
2. 200 mV min.
3. Data guaranteed by design, not tested in production.

Figure 30. Typical NRST pull-up resistance R_{PU} vs V_{DD}

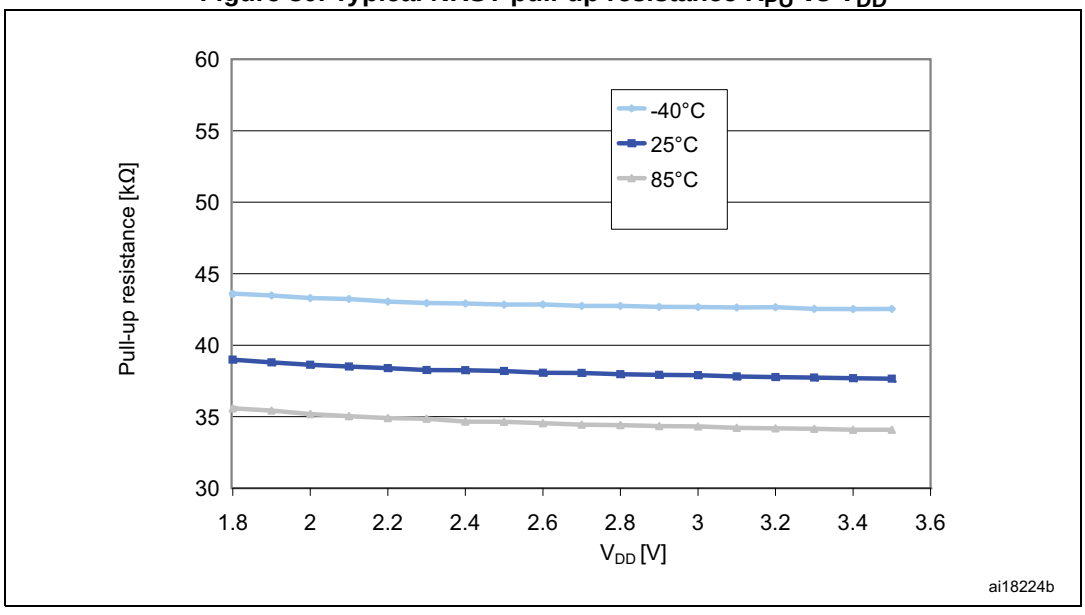


Figure 33. SPI1 timing diagram - slave mode and CPHA=0

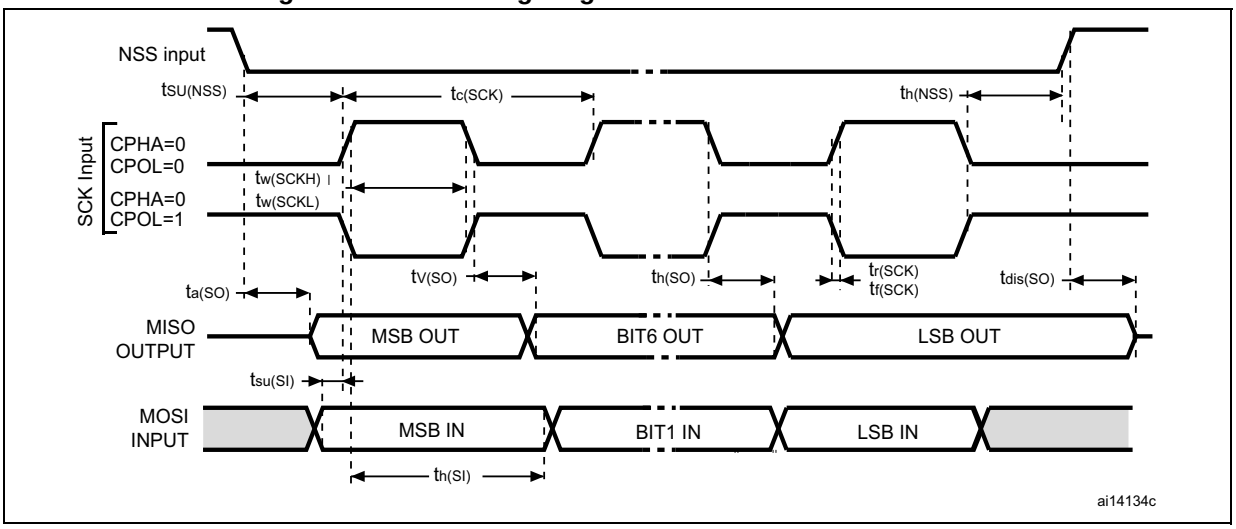
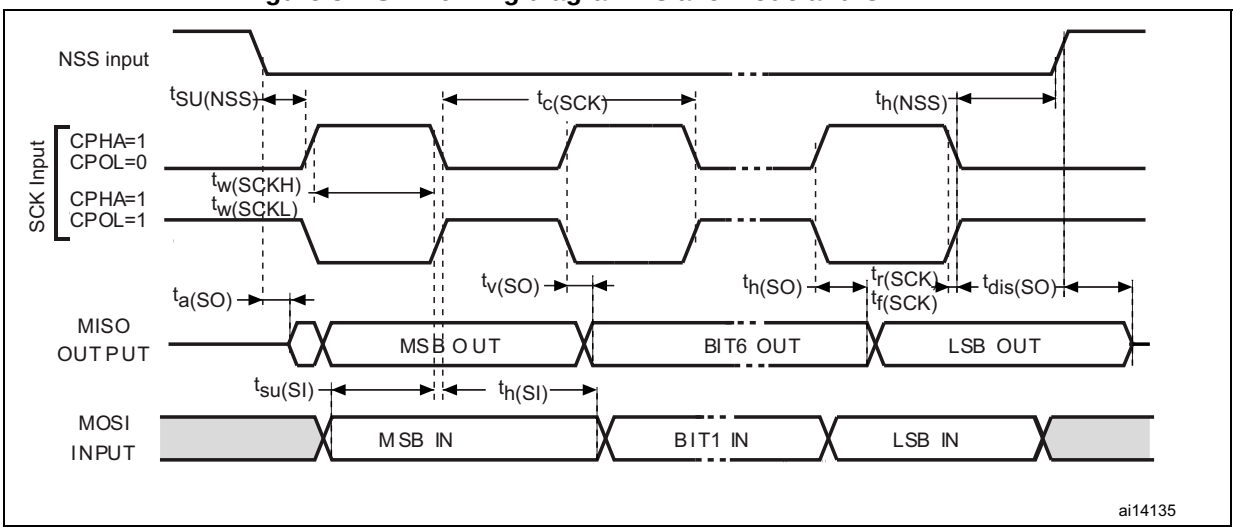
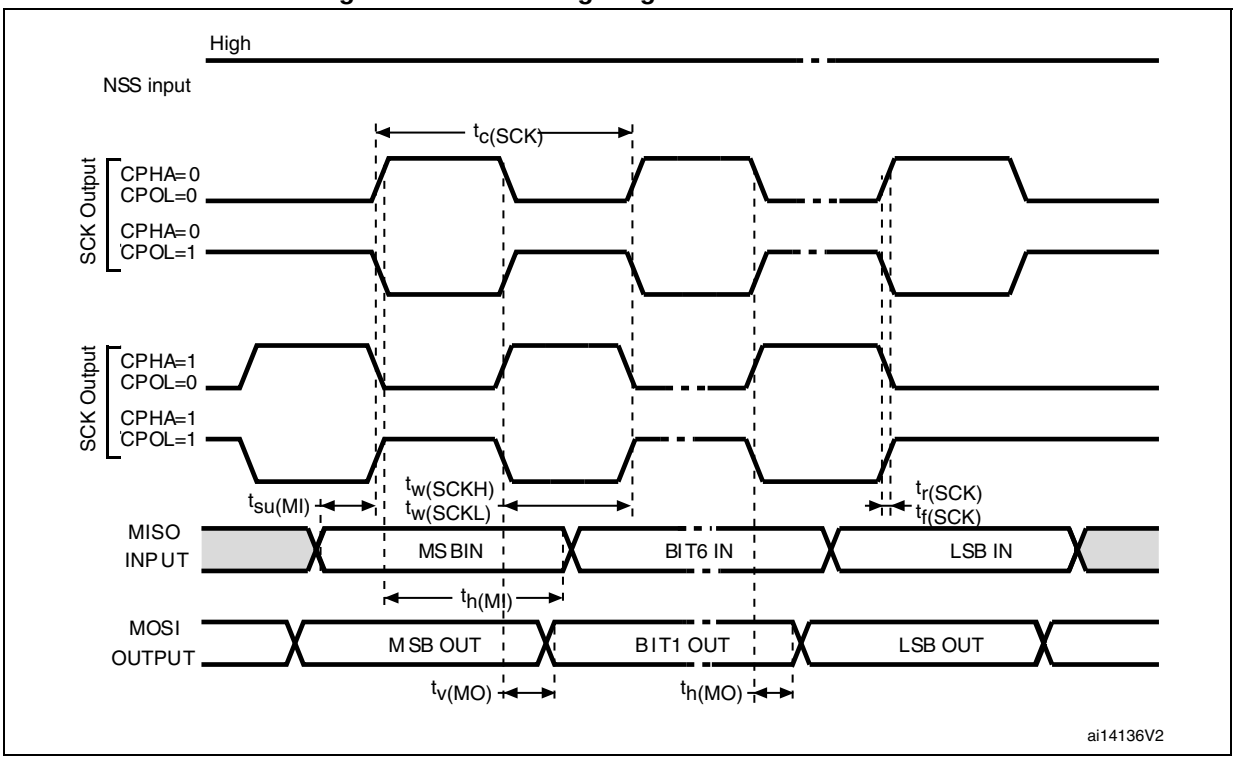


Figure 34. SPI1 timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 35. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.10 Temperature sensor

In the following table, data is based on characterization results, not tested in production, unless otherwise specified.

Table 45. TS characteristics

Symbol	Parameter	Min	Typ	Max.	Unit
V_{125}(1)	Sensor reference voltage at 90°C ±5 °C,	0.640	0.660	0.680	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope (2)	Average slope	1.59	1.62	1.65	mV/°C
$I_{DD(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC1 sampling time when reading the temperature sensor	10	-	-	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC1 conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Data guaranteed by design, not tested in production.
3. Defined for ADC1 output reaching its final value ±1/2LSB.

9.3.11 Comparator characteristics

In the following table, data is guaranteed by design, not tested in production, unless otherwise specified.

Table 46. Comparator 1 characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	1.65	-	3.6	V
T_A	Temperature range	-40	-	125	°C
R_{400K}	R_{400K} value	300	400	500	kΩ
R_{10K}	R_{10K} value	7.5	10	12.5	
V_{IN}	Comparator 1 input voltage range	0.6	-	V_{DDA}	V
V_{REFINT}	Internal reference voltage(2)	1.202	1.224	1.242	
t_{START}	Comparator startup time	-	7	10	µs
t_d	Propagation delay(3)	-	3	10	
V_{offset}	Comparator offset error	-	±3	±10	mV
I_{COMP1}	Current consumption(4)	-	160	260	nA

1. Based on characterization, not tested in production.
2. Tested in production at V_{DD} = 3 V ±10 mV.
3. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
4. Comparator consumption only. Internal reference voltage not included.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/A115A standard.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results, not tested in production.

Static latch-up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 56. Electrical sensitivities

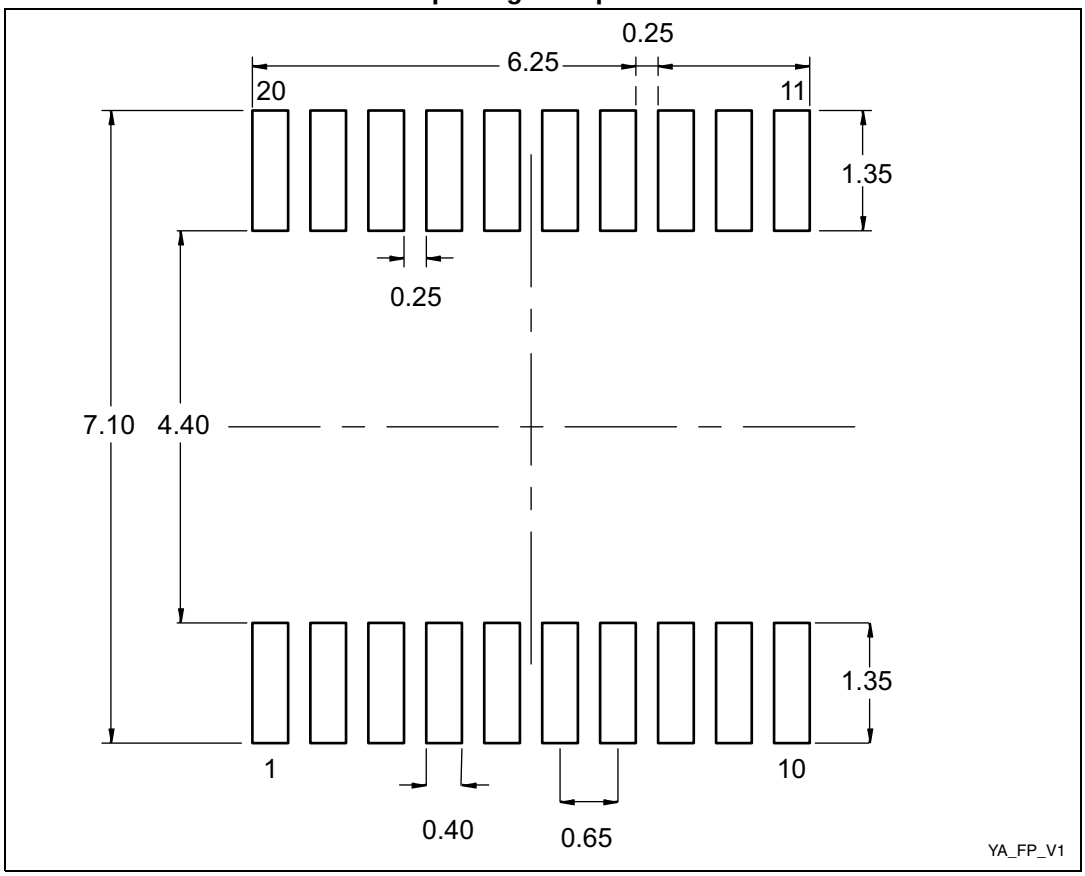
Symbol	Parameter	Class
LU	Static latch-up class	II

Table 61. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 55. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint



1. Dimensions are expressed in millimeters.

12 Revision history

Table 64. Document revision history

Date	Revision	Changes
08-Jun-2011	1	Initial release
02-Sep-2011	2	Modified *Figure: Memory map.* Modified OPT1 description in *Table: Option byte addresses.* Modified t_{prog} in *Table: Flash program and data EEPROM memory.* Modified *Figure: Recommended NRST pin configuration.* Modified L2 in *Figure: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline.* Replaced PM0051 with PM0054 and UM0320 with UM0470.
09-Feb-2012	3	Added part number STM8L151C2. Updated the captions of *Figure 3* and *Figure 4*. *Table: Low-density STM8L151x2/3 pin description*: updated OD column of NRST/PA1 pin. *Figure: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline:* removed the line over A1. *Figure Recommended UFQFPN28 footprint (dimensions in mm):* updated title. *Table: TSSOP20 - 20-pin thin shrink small outline package mechanical data:* updated title.
06-Jul-2012	4	Added “I/O level” in *Table: Legend/abbreviation for table 4* and *Table: Low-density STM8L151x2/3 pin description.* Updated *Figure: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3).* Updated *Figure: SPI1 timing diagram - master mode.* Updated *Table: Voltage characteristics* and *Table: I/O static characteristics.*
11-Apr-2014	5	Updated *Table: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3x3) package mechanical data,* added notes on *Table: TSSOP20 - 20-pin thin shrink small outline package mechanical data.* Changed reset value of SYSCFG_RMPCR1 register on *Table: General hardware register map.* Updated *Table: Low-density STM8L151x2/3 pin description* and *Table: Embedded reset and power control block characteristics.*

Table 64. Document revision history (continued)

Date	Revision	Changes
18-Dec-2014	6	Updated *Section: UFQFPN20 package information.* Replaced “ultralow power” occurrences with “ultra-low-power”, and “Low density” with “low-density” where applicable.
08-Apr-2015	7	Added: – *Figure 44: LQFP48 marking example (package top view)*, – *Figure 47: UFQFPN32 marking example (package top view)*, – *Figure 50: UFQFPN28 marking example (package top view)*, – *Figure 53: UFQFPN20 marking example (package top view)*, – *Figure 56: TSSOP20 marking example (package top view)*. Updated: – *Table 63: Low-density STM8L151x2/3 ordering information scheme*. Moved *Section 10.7: Thermal characteristics* to *Section 10: Package information*.
01-Oct-2016	8	In *Table 4: Low-density STM8L151x2/3 pin description* row corresponding to pin names PD6/ADC1_IN8 / RTC_CALIB/COMP1_INP, inserted pin number 35 in LQFP48 column.