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2 Registers

How to Read Register Tables

① Bit Numbers: Each register is connected with an internal bus of 16-bit wide, so the bit numbers of the registers located at odd addresses are b15-b8, and those at even addresses are b7-b0.

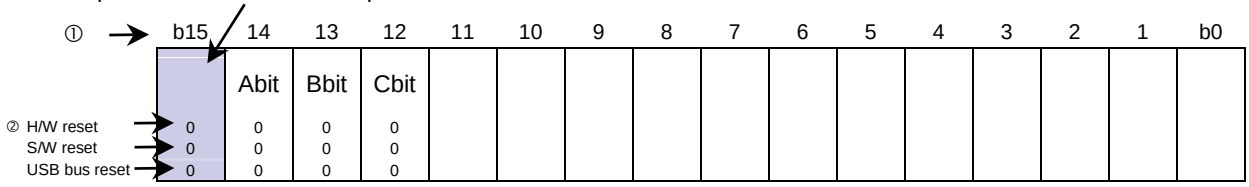
② State of Register at Reset:
Represents the initial state of each register immediately after reset with hexadecimal numbers. The “H/W reset” is the reset by an external reset signal; the “S/W reset” is the reset by the USBE bit of the USB Operation Enable Register.

③ At Read:
○ ... Read enabled
? ... Read disabled (Read value invalid)
0 ... Read always as 0
1 ... Read always as 1

④ At Write:
○ ... Write enabled
Δ ... Write enable conditionally (includes some conditions at write)
— ... Write disabled (Don’t care “0” and “1” at write)
X ··· Write disabled

<Example of representation>

Not implemented in the shaded portion.



②

<H/W reset: H’0000>

<S/W reset: ->

<USB bus reset: ->

b	Bit name	Function	R	W
15	Reserved.		0	-
14	A bit (----------)	0: ---------- 1: ----------	0	0
13	B bit (----------)	0: ---------- 1: ----------	0	0
12	C bit (----------)	0: ---------- 1: ----------	0	0
			③	④

Address	+1 address b15 – b8	+0 address b7 – b0	Reset state H/W	Reset state S/W	Reset state USB bus
H'48	INT Pin Configuration Register 3		0000h	0000h	-
H'4A					
H'4C	INT Pin Configuration Register 4		0000h	0000h	-
H'4E					
H'50					
H'52					
H'54					
H'56					
H'58					
H'5A					
H'5C					
H'5E					
H'60	Interrupt Status Register 0		0000 0000 ?000 0000b	0000 0000 ?000 0000b	---1 ---- -001 ----b
H'62					
H'64	Interrupt Status Register 1		0000h	0000h	-
H'66					
H'68	Interrupt Status Register 2		0000h	0000h	-
H'6A					
H'6C	Interrupt Status Register 3		0000h	0000h	-
H'6E					
H'70					
H'72					
H'74	USB Address Register		0000h	0000h	0000h
H'76					
H'78	USB Request Register 0		0000h	0000h	0000h
H'7A	USB Request Register 1		0000h	0000h	0000h
H'7C	USB Request Register 2		0000h	0000h	0000h
H'7E	USB Request Register 3		0000h	0000h	0000h
H'80					
H'82	DCP Configuration Register 1		0000h	0000h	-
H'84	DCP Configuration Register 2		0000h	0000h	-
H'86					
H'88	DCP Control Register		0000h	0000h	---- ---- ---- -000b
H'8A					
H'8C	PIPE Configuration Select Register		0000h	0000h	-
H'8E					
H'90	PIPE Configuration Window Register 0		0000h	0000h	00-- ---- ---- ----b
H'92					
H'94					
H'96					
H'98					

Note: Refer to each register described below.

Figure 2.2 Register Mapping (2)

2.8 Data Pin & FIFO/DMA Control Pin Configuration Register 1

■ Data Pin & FIFO/DMA Control Pin Configuration Register 1 (PinCtrlCfg1) <Address: H'0A>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
LDRV							big_end						PAdir		DB_Cfg
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: ->
<USB bus reset: ->

b	Bit name	Function	R	W
15	LDRV Drive Current Adjust	0: When VIF=1.7~2.0V 1: When VIF=2.7~3.6V	○	○
14~9	Reserved. Set it to "0".		"0"	"0"
8	big_end Big Endian Mode	0: Little endian 1: Big endian	○	○
7~3	Reserved. Set it to "0".		"0"	"0"
2	PAdir Port A Direction	0: Input 1: Output	○	○
1	Reserved. Set it to "0".		"0"	"0"
0	DB_Cfg Data Bus Configuration	0: SD7-SD0/PA7-PA0 are set as the general-purpose port 1: SD7- SD0/PA7-PA0 are set as the split bus	○	○

(1) LDRV (Drive Current Adjust) Bit (b15)

This bit is used to adjust the drive current of the output pins.
The output pins here refer to SD7-0, D15-0, INT, DREQ, DEND, SUSP_ON and CONF_ON pins.

(2) big_end (Big Endian Mode) Bit (b8)

This bit sets the endian of the C_FIFO port and the D0_FIFO port.
When this bit is set to "0", the C_FIFO port and the D0_FIFO port becomes little endian.
When this bit is set to "1", the C_FIFO port and the D0_FIFO port becomes big endian.

	b15~b8	b7~b0
Little Endian	Odd number address	Even number address
Big Endian	Even number address	Odd number address

(3) PAdir (Port A Direction) Bit (b2)

This bit sets the port A direction. This bit is valid only when the DB_Cfg bit is set to "0".
General purpose port PA7-PA0 is input port when this bit is set to "0".
General purpose port PA7-PA0 is output port when this bit is set to "1".

(4) DB_Cfg (Data Bus Configuration) Bit (b0)

This bit sets the operations of SD7-SD0/PA7-PA0.
When this bit is set to "0", SD7-SD0/PA7-PA0 becomes the general-purpose port (GPIO).
When this bit is set to "1", SD7-SD0/PA7-PA0 becomes the split bus for the D0_FIFO port. In this case, CPU access to the D0_FIFO Port Register is invalid.

2.15 C_FIFO Port Control Register 2

■ C_FIFO Port Control Register 2 (C_FIFOPortCtrl2) <Address: H'2E>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
TGL	SCLR	SBUSY													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15	TGL Buffer Toggle	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Toggles access buffer <When set to IN buffer> • Write Set it to "0"	"0"	○
14	SCLR Buffer Clear	<When set to OUT buffer> • Write 0: Invalid (Ignored when written) 1: Inhibited <When set to IN buffer> • Write 0: Invalid (Ignored when written) 1: Clear the SIE side buffer	"0"	○
13	SBUSY SIE side Buffer Busy	0: SIE no access state 1: SIE access state	○	-
12~0	Reserved. Set it to "0".		"0"	"0"

(1) TGL (Buffer Toggle) Bit (b15)

The SIE side buffer is changed over to the CPU side buffer by writing "1" to this bit while the FIFO buffer is not full in continuous transfer mode. At this time, the buffer ready interrupt occurs. This bit is valid only for the PIPE of OUT direction. Further, when the PIPE which has been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is DCP, writing "1" to this bit is invalid.

Writing "0" to this bit is invalid.

Explanation of Terms: Refer to "1.5 Block Diagram" about "SIE side" and "CPU side".

(2) SCLR (Buffer Clear) Bit (b14)

The SIE side buffer is cleared and the SIE side buffer is changed over to the CPU side buffer by writing "1" to this bit. This bit is valid only for the PIPE of IN direction. Further, when the PIPE which has been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 is DCP, writing "1" to this bit is invalid.

Please set according to the following procedures in order to use this bit:

(1) Set the PID [1:0] bits of the PIPE i Control Register corresponding to the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0 to the NAK so that it does not respond to the IN transaction.

(2) Confirm that the SBUSY bit is "0". (Confirm that no buffer access exists.)

(3) Clear the SIE-side buffer by writing "1" to the SCLR bit.

Writing "0" to this bit is invalid.

(3) SBUSY (SIE side Buffer Busy) Bit (b13)

This bit indicates that SIE is accessing the buffer of the PIPE having been set to the Current_PIPE [2:0] bits of the C_FIFO Port Control Register 0. Further, when the PIPE which has been set to the Current_PIPE [2:0] bits is DCP, reading of this bit is invalid.

2.23 INT Pin Configuration Register 4

■ INT Pin Configuration Register 4 (INTPinCfg4) <Address: H'4C>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_EMPE6 0 0 -	PIPEB_EMPE5 0 0 -	PIPEB_EMPE4 0 0 -	PIPEB_EMPE3 0 0 -	PIPEB_EMPE2 0 0 -	PIPEB_EMPE1 0 0 -	DCP_EMPE 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_EMPE6 PIPE6 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
5	PIPEB_EMPE5 PIPE5 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
4	PIPEB_EMPE4 PIPE4 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
3	PIPEB_EMPE3 PIPE3 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
2	PIPEB_EMPE2 PIPE2 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
1	PIPEB_EMPE1 PIPE1 Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O
0	DCP_EMPE DCP_FIFO Buffer Empty/Size-Error Interrupt Enable	0: Disable the BEMP bit set 1: Enable the BEMP bit set	O	O

(1) PIPEB_EMPE6 (PIPE6 Buffer Empty/Size Error Interrupt Enable) Bits (b6)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR6 bit of the Interrupt Status Register 3 is set to "1".

(2) PIPEB_EMPE5 (PIPE5 Buffer Empty/Size Error Interrupt Enable) Bits (b5)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR5 bit of the Interrupt Status Register 3 is set to "1".

(3) PIPEB_EMPE4 (PIPE4 Buffer Empty/Size Error Interrupt Enable) Bits (b4)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR4 bit of the Interrupt Status Register 3 is set to "1".

(4) PIPEB_EMPE3 (PIPE3 Buffer Empty/Size Error Interrupt Enable) Bits (b3)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR3 bit of the Interrupt Status Register 3 is set to "1".

(5) PIPEB_EMPE2 (PIPE2 Buffer Empty/Size Error Interrupt Enable) Bits (b2)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR2 bit of the Interrupt Status Register 3 is set to "1".

(6) PIPEB_EMPE1 (PIPE1 Buffer Empty/Size Error Interrupt Enable) Bits (b1)

These bits select whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the PIPEB_EMP_OVR1 bit of the Interrupt Status Register 3 is set to "1".

(7) DCP_EMPE (DCP_FIFO Buffer Empty/Size Error Interrupt Enable) Bit (b0)

This bit selects whether to set the BEMP bit of Interrupt Status Register 0 to "1" or not when the DCP_EMP_OVR bit of the Interrupt Status Register 3 is set to "1".

2.26 Interrupt Status Register 2

■ Interrupt Status Register 2 (INTStatus2) <Address: H'68>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	0 0 -	PIPEB_NRDY6 0 0 -	PIPEB_NRDY5 0 0 -	PIPEB_NRDY4 0 0 -	PIPEB_NRDY3 0 0 -	PIPEB_NRDY2 0 0 -	PIPEB_NRDY1 0 0 -	DCP_NRDY 0 0 -

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6	PIPEB_NRDY6 PIPE6 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
5	PIPEB_NRDY5 PIPE5 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
4	PIPEB_NRDY4 PIPE4 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
3	PIPEB_NRDY3 PIPE3 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
2	PIPEB_NRDY2 PIPE2 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
1	PIPEB_NRDY1 PIPE1 Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○
0	DCP_NRDY Default Control PIPE Buffer Not Ready Interrupt	• Read 0: No occurrence of interrupt 1: Occurrence of interrupt • Write 0: Clear interrupt 1: Invalid (Ignored when written)	○	○

Note for clearing the buffer not ready interrupt (PIPEB_NRDY6-PIPEB_NRDY1/DCP_NRDY) status bits:

In order to continuously clear status bits while the PIPEB_NRDY6-PIPEB_NRDY1/DCP_NRDY status bits are set to "1" by being multiplexed, the access cycle time of 100ns or more is required from clear to the next clear. For example, where both the PIPEB_NRDY1 status bit and the PIPEB_NRDY2 status bit are simultaneously set, the access cycle required from when "0" is written to the PIPEB_NRDY1 bit until when "0" is written to the PIPEB_NRDY2 bit is 100ns or more. Also at this time, it is enable to clear the PIPEB_NRDY1 bit and the PIPEB_NRDY2 bit at the same time.

2.33 DCP Configuration Register 1

■ DCP Configuration Register 1 (DCPCfg1) <Address: H'82>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
0	0	0	0	0	0	0	CNTMD	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~9	Reserved. Set it to "0".		"0"	"0"
8	CNTMD Continuous Transmit/Receive Mode	0: Non-continuous transmit/receive mode 1: Continuous transmit/receive mode	○	○
7~0	Reserved. Set it to "0".		"0"	"0"

(1) CNTMD (Continuous Transmit/Receive Mode) Bits (b8)

These bits set the transmit/receive mode in data stage of the control read/write transfer.

In case of the control read transfer:
CNTMD = "0": Non-continuous transmit mode
The transmit completes under the conditions as follows:
- Transmits the data equivalent to the size set by the DCP_MXPS [6:0] bits of DCP Configuration Register 2 or transmits the short packet by setting the BVAL bit of C_FIFO Port Control Register 1 to "1".

The writing completes under the conditions as follows:
- Writes to the buffer the data equivalent to the size set by the DCP_MXPS [6:0] bits. (BVAL bit changes to "1").
- Writes "1" to the BVAL bit.

CNTMD = "1": Continuous transmit mode
The transmit completes under the conditions as follows:
- Transmits the data equivalent to the size set by the SDLN [8:0] bits of DCP Continuous Transmit Data Length Register or transmits the short packet by setting the BVAL bit to "1".

The writing completes under the conditions as follows:
- Writes to the buffer the data equivalent to the size set by the SDLN [8:0] bits. (BVAL bit changes to "1").
- Writes "1" to the BVAL bit.

In case of the control write transfer:
CNTMD = "0": Non-continuous receive mode. The receive completes by receiving one packet under the condition as follows:
- Receives the data equivalent to the size set by the DCP_MXPS [6:0] bits of DCP Configuration Register 2.
- Receives the short packet.

CNTMD = "1": Continuous receive mode. The receive completes by receiving several packets under the condition as follows:
- Receives the data equivalent to 256 bytes set by buffer size of DCP.
- Receives the short packet.

2.34 DCP Configuration Register 2

■ DCP Configuration Register 2 (DCPCfg2) <Address: H'84>

b15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	b0
									DCP_MXPS [6:0]						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

<H/W reset: H'0000>
<S/W reset: H'0000>
<USB bus reset: ->

b	Bit name	Function	R	W
15~7	Reserved. Set it to "0".		"0"	"0"
6~0	DCP_MXPS [6:0] DCP Maximum Packet Size	Upper limit of the transmit/receive data for one packet transfer (Settable only 8,16,32 and 64)	○	○

(1) DCP_MXPS [6:0] (DCP Maximum Packet Size) Bits (b6-b0)

These bits set the upper limit (byte count) of the transmit/receive data for one packet transfer in data stage.

For these bits, 8, 16, 32 and 64 are available during operation in the Full-Speed mode, and 64 during operation in the Hi-Speed mode. Other values are not permitted.

At the time of transmitting, the data equivalent to the size set by these bits are read from the buffer for transmission. When the buffer does not have the data equivalent to the size set by these bits, the data are transmitted as the short packet.

At the time of receiving, the data equivalent to the size set by these bits are written to the buffer. If the received packet data are larger than the size set by these bits, the DCP_EMP_OVR bit of the Interrupt Status Register 3 is set to "1".

When initializing DCP, be sure to set these bits before setting the PID bits of DCP Control Register to "01". Also, when changing the value of these bits, be sure to set beforehand the PID bits of DCP Control Register to "00" (NAK).

(3) SQCLR (Sequence Bit Clear) Bit (b8)

This bit clears the sequence bit of the PIPE1 to PIPE4 to set the next data PID to the "DATA0".
The sequence bit is toggled through hardware control in the transfers after the sequence bit is cleared.
With the USB bus reset, the sequence toggle bit is not cleared. It is necessary to clear the sequence bit by software.
Writing "0" to this bit is invalid. This bit is always read "0". Before setting this bit, be sure to set the PID [1:0] bits to "00" (NAK).

Note: To clear two or more sequence toggle bits of the PIPE continuously, the access cycle time of 200ns or more is required from one SQCLR bit of the PIPE access to the next SQCLR bit of the PIPE access. For example, when the sequence toggle bits of both PIPE1 and PIPE2 are cleared, the access cycle required from when "1" is written to the SQCLR bit of PIPE1 to when "1" is written to the SQCLR bit of PIPE2 is 200ns or more.

(4) NYETMD (NYET Handshake Mode) Bit (b4)

This bit sets the NYET response mode.
0: Automatic response mode (ACK/NYET is automatically selected.)
1: ACK response only mode (Always with ACK response. No NYET response.)
This bit is valid when the PID [1:0] bits of the OUT transfer are "01"(BUF) in case the bulk transfer operated in the Hi-Speed mode. In any other case, this bit is invalid.
In the automatic response mode, hardware automatically selects an appropriate response PID (NAK/ACK/NYET) according to the buffer status below:
(1) When the buffer to receive the data packet is the buffer full, the NAK response is executed.
(2) When an empty space existing in the buffer is equal to or more than twice as large as the max packet size before receiving of the data packet, the ACK response is executed.
(3) When an empty space existing in the buffer is less than twice as large as the max packet size before receiving of the data packet, the NYET response is executed.

In the ACK response only mode, the device does not transmit the NYET packet. The ACK/NAK response is executed.

(5) PID [1:0] (Response PID) Bits (b1-b0)

These bits set the PID for response of PIPE1 to PIPE4.
00: NAK response
The NAK response is executed irrespective of buffer status.
01: BUF response
The response ID is selected according to the buffer status, the value of the NYETMD bit and the value of the sequence toggle bit.
When the NYETMD bit is "00" and in the bulk OUT transfer, the NYET response is executed in the following conditions:
(1) When the non-continuous transmit/receive mode and the single buffer mode.
(2) When the buffer on the CPU-side is not empty in the non-continuous transmit/receive mode and the double buffer mode before receiving the data packet.
1x: STALL response
The STALL response is executed irrespective of buffer status.
When the data packet exceeding the max packet size (512 bytes when Hi-Speed, 64 bytes when Full-Speed) of PIPE1 to PIPE4 has been received while setting the transfer direction of the PIPE to OUT, these bits are automatically set to "1x".
To set the STALL response, follow the procedure below in accordance with this bit value before setting:
(1) Set to "10" when PID [1:0] are set to "00"
(2) Set to "11" when PID [1:0] are set to "01"

3.2.2 Process After Detection of Attach/Detach (VBUS Interrupt)

M66591 uses VBUS interrupt to detect attach to the host to or detach from the host.

The VBUS interrupt occurs when either “Low”->”High” or “High”->“Low” change has occurred in the VBUS pin input. The attach to the host or detach from the host is judged by polling of the VBUSSTS bit of the Interrupt Status Register 0.

When attach to the host has been determined, M66591 execute the USB attach processing.

When detach from the host has been determined, M66591 execute the USB detach processing.

The detailed process flowchart is shown in the following Figure 3.4.

The VBUS interrupt is occurred even while the internal clock (SCKE bit of the USB Transceiver Control Register 0 = “0”) is not supplied. Also, The VBUSSTS bit is capable of reading correct value even if the internal clock is not supplied.

The VBUS interrupt (VBUSINT bit) is cleared by the following two methods according to the internal clock:

(1) State when the internal clock is supplied (SCKE bit of the USB Transceiver Control Register 0 = “1”)
This bit is cleared to “0” by writing “0” to the VBUSINT bit.

(2) State when the internal clock is not supplied (SCKE bit of the USB Transceiver Control Register 0 = “0”)
This bit is cleared to “0” by writing “0” to the VBUSINT bit. Write “1” to this bit once again to enable next VBUS interrupt.

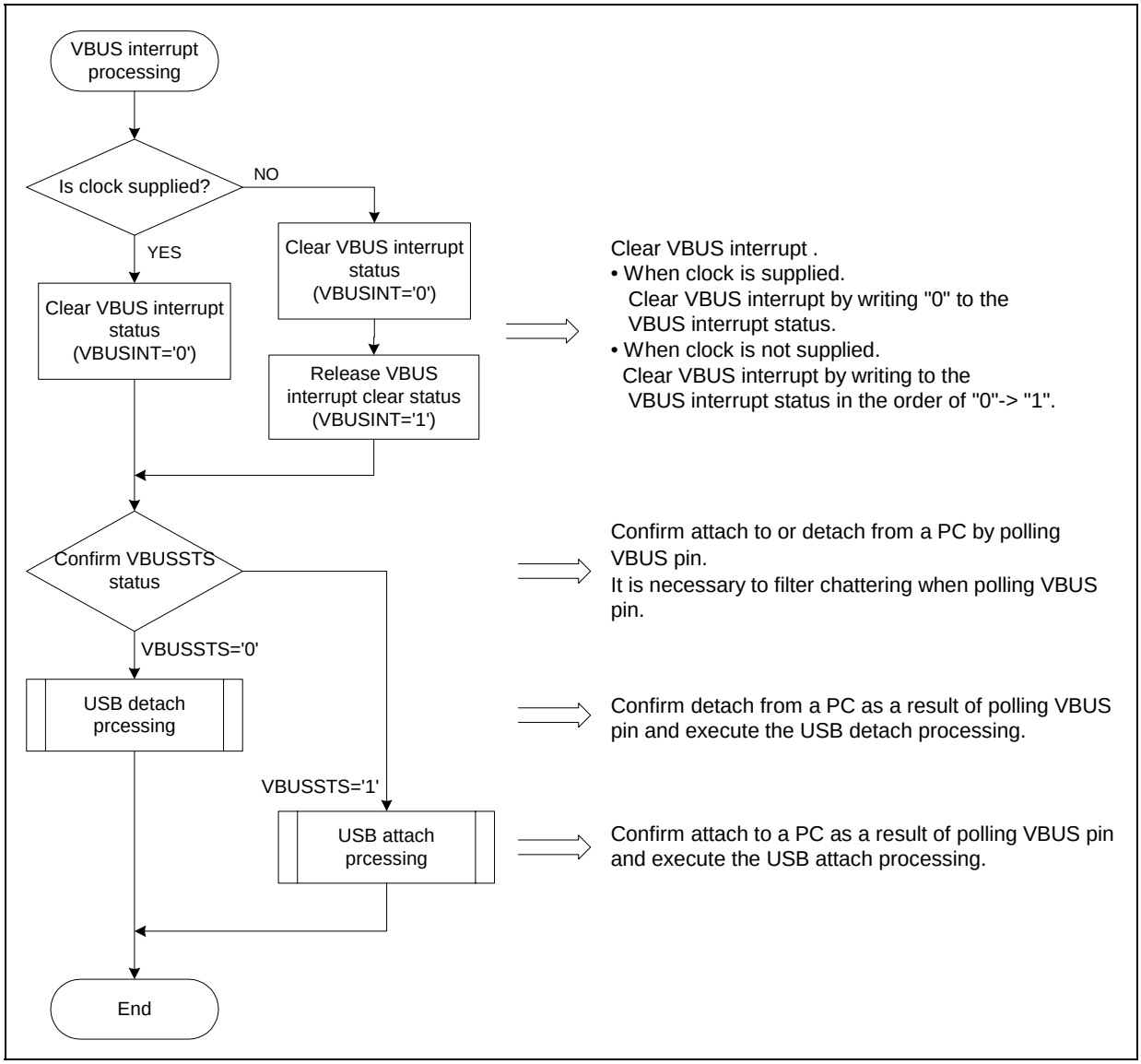


Figure 3.4 M66591 VBUS Interrupt Process Flowchart

3.3 Interrupt

3.3.1 Features

There are 7 factors of interrupts in M66591. The 7 factors of interrupts is shown in Table 3.2.

The interrupt factors can set to enable/disable by the INT Pin Configuration Register 0, 2, 3. A diagrams related to the interrupt is shown in Figure 3.10.

The sense mode and polarity of the interrupt output can set to enable by the INT Pin Configuration Register 1. Figure 3.11 shows the interrupt pin output timing.

Table 3.2 List of Interrupts

Status Bit	Interrupt Name	Interrupt Factor	Related Status Bit
VBUSINT	VBUS Interrupt (Detection of attach/detach)	Change of the VBUS input level (change of “Low”->”High”, “High”->”Low”)	VBUSSTS
RESM	Resume Interrupt	Change of the USB bus state in suspended state (J state -> K state, J state -> “SE0”)	-
DVST	Device State Transition Interrupt	Device State Transition • Detection of the USB bus reset • Detection of suspended state • Execution of the SET_ADDRESS • Execution of the SET_CONFIGURATION	DVST [2:0]
CTRT	Control Transfer Stage Transition Interrupt	Control Transfer Stage Transition • Completion of setup stage • Transition of control write transfer status stage • Transition of control read transfer status stage • Completion of control transfer • Occurrence of control transfer sequence error	CTSQ [2:0]
BEMP	PIPE Buffer Empty / Size Error Interrupt	In each PIPE; When all data in the FIFO buffer have been transmitted completely and the buffer has become empty for the IN token. When a packet exceeding the max packet size has been received for the OUT token.	PIPEB_EMP_OVR6, PIPEB_EMP_OVR5, PIPEB_EMP_OVR4, PIPEB_EMP_OVR3, PIPEB_EMP_OVR2, PIPEB_EMP_OVR1, DCP_EMP_OVR
INTN	PIPE Buffer Not Ready Interrupt	In each PIPE; When no transmittable data exist in the FIFO buffer for the IN token. When the FIFO buffer does not have any data storage space and disables receiving for the OUT token.	PIPEB_NRDY6, PIPEB_NRDY5, PIPEB_NRDY4, PIPEB_NRDY3, PIPEB_NRDY2, PIPEB_NRDY1, DCP_NRDY
INTR	PIPE Buffer Ready Interrupt	When each PIPE buffer is ready state (read/write enable state)	PIPEB_RDY6, PIPEB_RDY5, PIPEB_RDY4, PIPEB_RDY3, PIPEB_RDY2, PIPEB_RDY1, DCP_RDY

3.3.5 Control Transfer Stage Transition Interrupt

The control transfer stage transition of M66591 is shown in Figure 3.13. Control transfer stage transition interrupt occurs when a stage transition occurs by the control transfer. Interrupt occurs when stage transition is detected except for the SET_ADDRESS request because it is responded automatically. Each stage transition can be individually enabled/disabled by enabling bit of INT Pin Configuration Register 0. However, setup stage completion can not be disabled. The control transfer stage is shown in DVSQ [2:0] bits of Interrupt Status Register 0.

The control transfer sequence errors are shown below. When an error occurs, the PID [1:0] bits of Default Control PIPE Control Register are set to “1X” (STALL).

<In the case of control read transfer>

- Receives the OUT or PING token for the IN token of the data stage when data transfer has not occurred even once.
- Receives the IN token in the status stage
- Receives the DATA packet with PID = DATA0 in the status stage

<In the case of control write transfer>

- Receives the IN token for the OUT token of the data stage when ACK response has not executed even once.
- Receives the first DATA packet with DATA PID = DATA0 in the data stage
- Receives the OUT or PING token in the status stage

<When control write no data transfer>

- Receives the OUT or PING token in the status stage

Further, when the number of the receive data of the data stage in none no data control write transfer has exceeded the wLength value of the request, the control transfer sequence error cannot be detected.

When the CTRT interrupt occurs (“SEER = 1“ setting) by sequence error, the “CTSQ [2:0] = 110” bits is held until “CTRT = 0” is wrote. Therefore, the CTRT interrupt of setup stage completion will not occur even if a new USB request is received in the “CTSQ [2:0] = 110” held state.

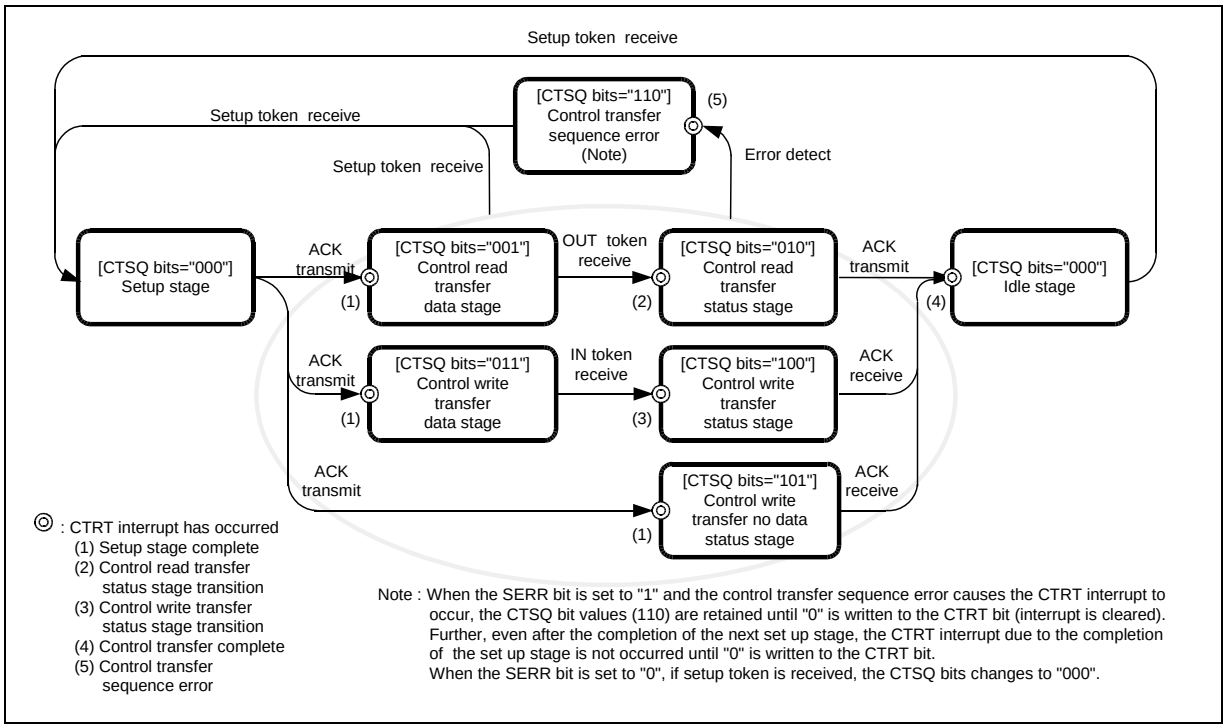


Figure 3.13 Control Transfer Stage Transition Diagram

3.3.6 PIPE Buffer Ready Interrupt

The condition of M66591 INTR interrupt occurring is shown in Table 3.3. The timing of M66591 INTR interrupt occurring is shown in Figure 3.14. The status of each PIPE is confirmed by the appropriate bit of Interrupt Status Register 1. When the DMA transfer is used, an interruption factor sets up by the BFRE bit of PIPE configuration window register 0 and the buffer memory access direction. So that the interrupt may not occur every transaction but every transfer. However, there is no BFRE bit in DCP.

The interrupt request is stored in Interrupt Status Register 1 even if INTRE bit of INT Pin Configuration Register 0 and PIPEB_RE6-1 bits, DCP_RE bit of INT Pin Configuration Register 2 is disabled.

INTR bit of Interrupt Status Register 0 is cleared by clearing all bits of Interrupt Status Register 1.

Table 3.3 INTR interrupt occurring condition

Buffer access	Direction	PIPE	BFRE	Occur condition of INTR interrupt	Remark
Read	OUT	DCP	-	Zero-length packet received	Necessary for buffer clear
				Short packet received, buffer full	
		1-4	0	Zero-length packet received	Necessary for buffer clear
				Short packet received, buffer full or completion of transaction counter	
			1	Zero-length packet received	Necessary for buffer clear
				Read completed after short packet received or completion of transaction counter	Necessary for buffer clear
Write	IN	DCP	-	Not occurred	
		1-4	0	Packet transmit (buffer full)	Writable
			1	Not occurred	
		5-6	-	Packet transmit (buffer full)	Writable

Although INTR bit is set to "1" when a zero-length packet is received, it is necessary to clear buffer even if the zero-length packet cannot be read-out.

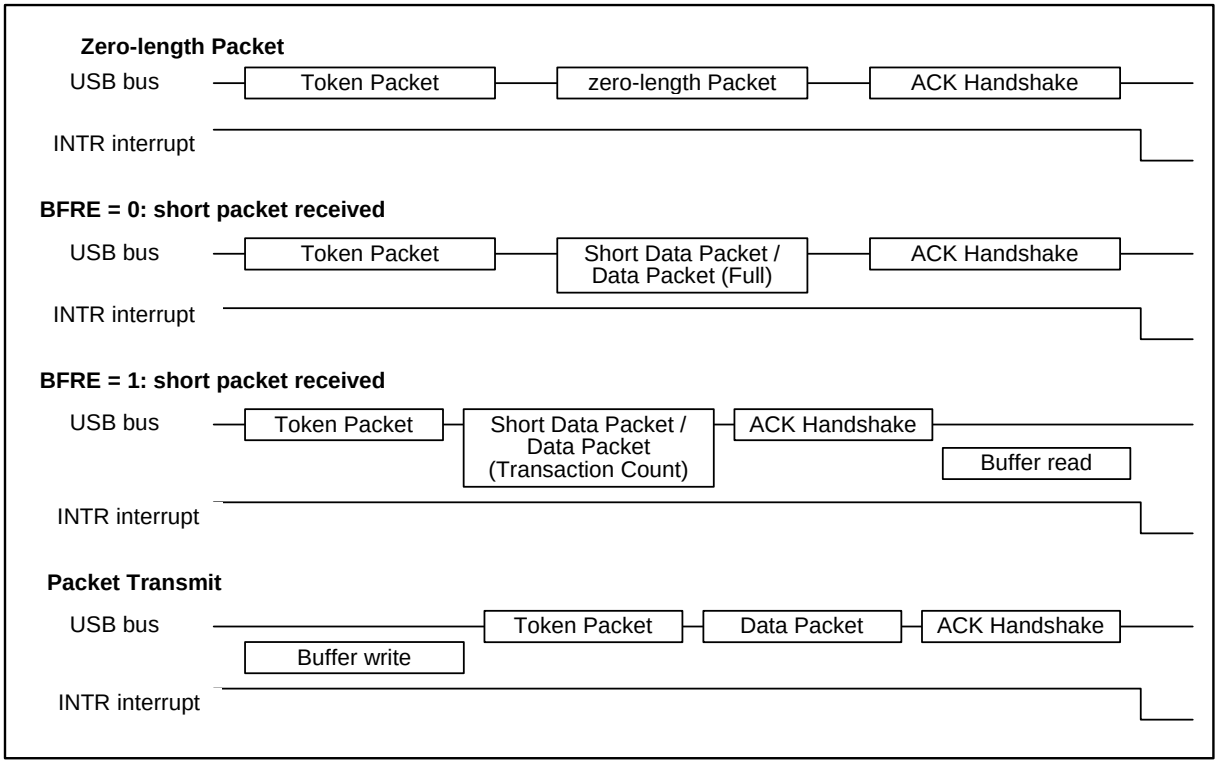


Figure 3.14 INTR interrupt occurring timing

3.4 Control Transfer and Enumeration

The control transfer consists of the setup stage, data stage, and status stage. M66591 executes the stage control and notifies the CPU of the stage transition by the interrupt.

The control transfer executes the data transfer by using the default control PIPE (EP0).

DCP buffer memory is a fixed 256 bytes single buffer shared with control read and write. The read and write to the DCP buffer is executed via C_FIFO Port Register. C_FIFO Port Register can be accessed only by CPU access.

3.4.1 Setup Stage

According to USB Specification, M66591 respond ACK to setup packet.

USB Request Register 0, USB Request Register 1, USB Request Register 2 and USB Request Register 3 are exclusive registers for storing USB request. The VALID bit of Interrupt Status Register 0 is set to “1”, and PID [1:0] bits of DCP Control Register are set “00 (NAK)” when these request registers are renewed (New USB request is received.).

In order to confirm if new USB request is received, it is necessary to clear VALID bit of Interrupt Status Register 0 to “0” before respond to control transfer. The register bits shown below are protected when VALID = 1. So it is possible to respond to the newest request any time.

1. PID [1:0] bits of DCP Control Register
   These bits can not to be set to “01 (ACK)” to complete data stage when VALID = 1.
2. CCPL bit of DCP Control Register
   This bit can not to be set to “1” to complete status stage correctly (Respond zero-length packet and ACK) when VALID = 1.

M66591 judges if the control transfer is control read transfer or control write transfer or control write no data transfer according to the direction bit (bit 8 of bmRequestType) and request data length (wLength) automatically.

3.4.2 Data Stage

Using DCP buffer memory to send data according to USB request received.

Before access DCP buffer memory, it is necessary to specify the access direction by ISEL bit of C_FIFO Port Control Register 0. It is possible to transfer plural packets using INTR interrupt and BEMP interrupt.

NYET is responded according to the condition of buffer memory in control write transfer. Refer to “3.5.6 PING/NYET Control” about NYET response.

3.4.3 Status Stage

Complete control transfer only by accessing CCPL bit of DCP Control Register not using buffer memory.

M66591 does sending zero-length packet then receiving ACK or receiving zero-length packet then sending ACK.

3.4.4 Automatic Response Control

M66591 respond to correct SET_ADDRESS request automatically. It is necessary to respond to all request except for SET_ADDRESS by software. It is necessary to respond to SET_ADDRESS by software if any error shown below occurs.

1. In the case of control transfer except control read transfer, bmRequestTypq is not equal 0x00.
2. In the case of control transfer with an error, wIndex is not equal 0x00.
3. In the case of control transfer except control write no data transfer, wLength is not 0x00.
4. In the case of control transfer with an request error, wValue is large than 0x7F.
5. In the case of control transfer with an device state error, DVSQ is equal “011 (Configured State)”.

3.6 Buffer Memory

3.6.1 Buffer Memory Assignment and Buffer Area

The buffer memory of DCP and PIPE1-PIPE6 is assigned to a fixed buffer memory area and size. It is not necessary to assign by S/W.

The FIFO buffer memory area mapping is shown in Table 3.5.

Table 3.5 Buffer Memory Mapping

Buffer memory	Buffer size	Remark
Buffer for DCP	256 bytes	Single buffer, Continuous transfer
Buffer for PIPE1	1K bytes	Double buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE2	1K bytes	Double buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE3	512 bytes	Single buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE4	512 bytes	Single buffer, Continuous transfer for Full-Speed mode
Buffer for PIPE5	64 bytes	Single buffer, Non-continuous transfer only
Buffer for PIPE6	64 bytes	Single buffer, Non-continuous transfer only

3.6.2 FIFO Buffer Access

The FIFO buffer assigned to the DCP and PIPE1 to PIPE6 of M66591 can be accessed via the two FIFO port registers. M66591 contains two FIFO port registers including C_FIFO port (for the CPU access) and D0_FIFO port (for the DMA access).

The FIFO port functional setting of M66591 is shown in Table 3.6.

In the case of access of writing data, the buffer will be ready (VALID state) automatically for transmitting when the data is written till the buffer full (or till the number of max packet size when the PIPE setting is non-continuous transmission). It is necessary to report the end of writing to let buffer be ready for transmitting fraction data by setting BVAL bit of "C_FIFO Port Control Register 1" and "D0_FIFO Port Control Register 2". It is possible to report the end of writing by DEND signal when DMA transfer is used.

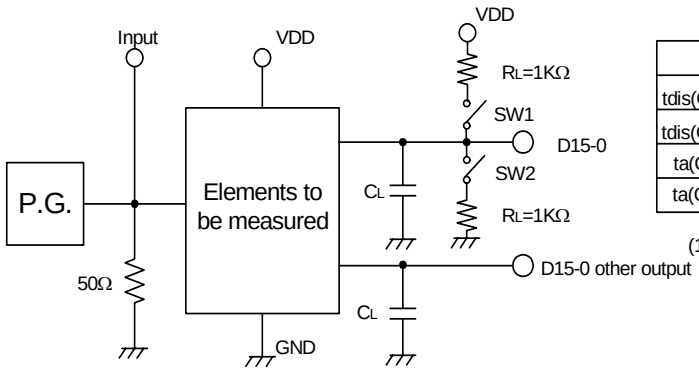
In the case of access of reading data, the buffer will be ready (empty state) automatically for receiving new data packets when the all data in the buffer is read out. The received data length can be confirmed by the DTLN [9:0] bits of "C_FIFO Port Control Register 1" and "D0_FIFO Port Control Register 2". Although the buffer will be available to read (ready state) when a zero-length packet is received (DTLN = 0), no data can be read out. At this time, it is necessary to clear the buffer by the BCLR bit of the same register.

Table 3.6 The table of FIFO port functional setting

Register Name	Bit Name	Contents of Setting and Function
C_FIFO Port Control Register 0	RCNT	Read Count Mode
	REW	Buffer Rewind (Re-reading, Re-writing)
	MBW	FIFO Access Maximum Bit Width
	ISEL	DCP Buffer Select
	Current_PIPE [2:0]	C_FIFO Port Access PIPE Designate
C_FIFO Port Control Register 1	BVAL	Buffer Valid Flag
	BCLR	Buffer Clear
	FRDY	C_FIFO Port Ready
	CPU_DTLN	Receive Data Length
C_FIFO Port Control Register 2	TGL	CPU/SIE Buffer Toggle
	SCLR	SIE Buffer Clear
	SBUSY	SIE Buffer Busy
D0_FIFO Port Control Register 0	RCNT	Read Count Mode
	REW	Buffer Rewind (Re-reading, Re-writing)
	ABCR	Automatic Buffer Clear Mode, Only used for D0_FIFO port
	MBW	FIFO Access Maximum Bit Width
	TREnb	Transaction Counter Enable
	TRclr	Transaction Counter Clear
	Current_PIPE [2:0]	D0_FIFO Port Access PIPE Designate
D0_FIFO Port Control Register 2	BVAL	Buffer Valid Flag
	BCLR	Buffer Clear
	FRDY	D0_FIFO Port Ready
	DMA_DTLN	Receive Data Length
D0_FIFO Port Control Register 3	TRNCNT [15:0]	Transaction Counter

4.5 Measurement circuit

4.5.1 Pins except for USB buffer block

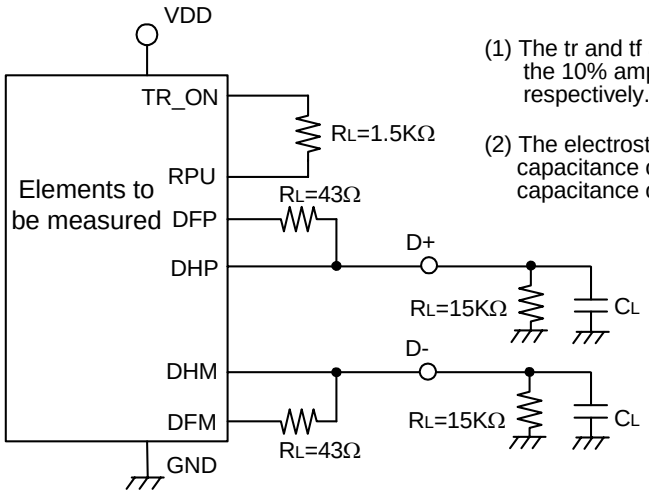


Item	SW1	SW2
tdis(CTRL(LZ))	close	open
tdis(CTRL(HZ))	open	close
ta(CTRL(ZL))	close	open
ta(CTRL(ZH))	open	close

(1) Input pulse level : 0 ~ 3.3V, 0 ~ 1.8V
Input pulse rise/fall time : tr,tf=3ns
Input timing standard voltage : VIF/2
Output timing judge voltage : VIF/2
(The tdis (LZ) is judged by 10% of the output amplitude and the tdis (HZ) by 90% of the output amplitude.)

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

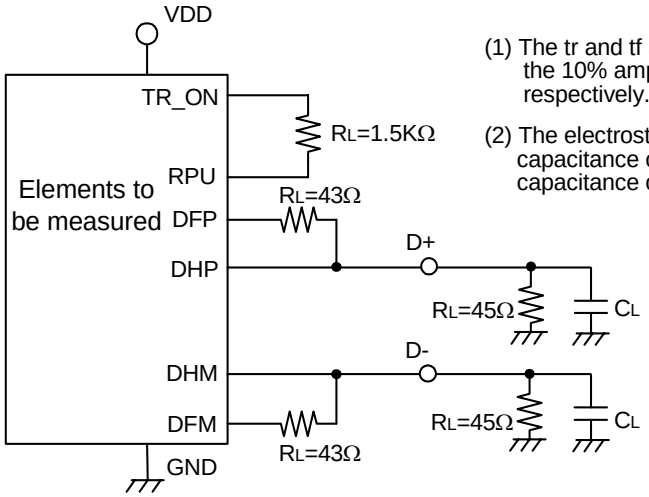
4.5.2 USB buffer block (Full-Speed)



(1) The tr and tf are judged by the transition time of the 10% amplitude point and 90% amplitude point respectively.

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

4.5.3 USB buffer block (Hi-Speed)



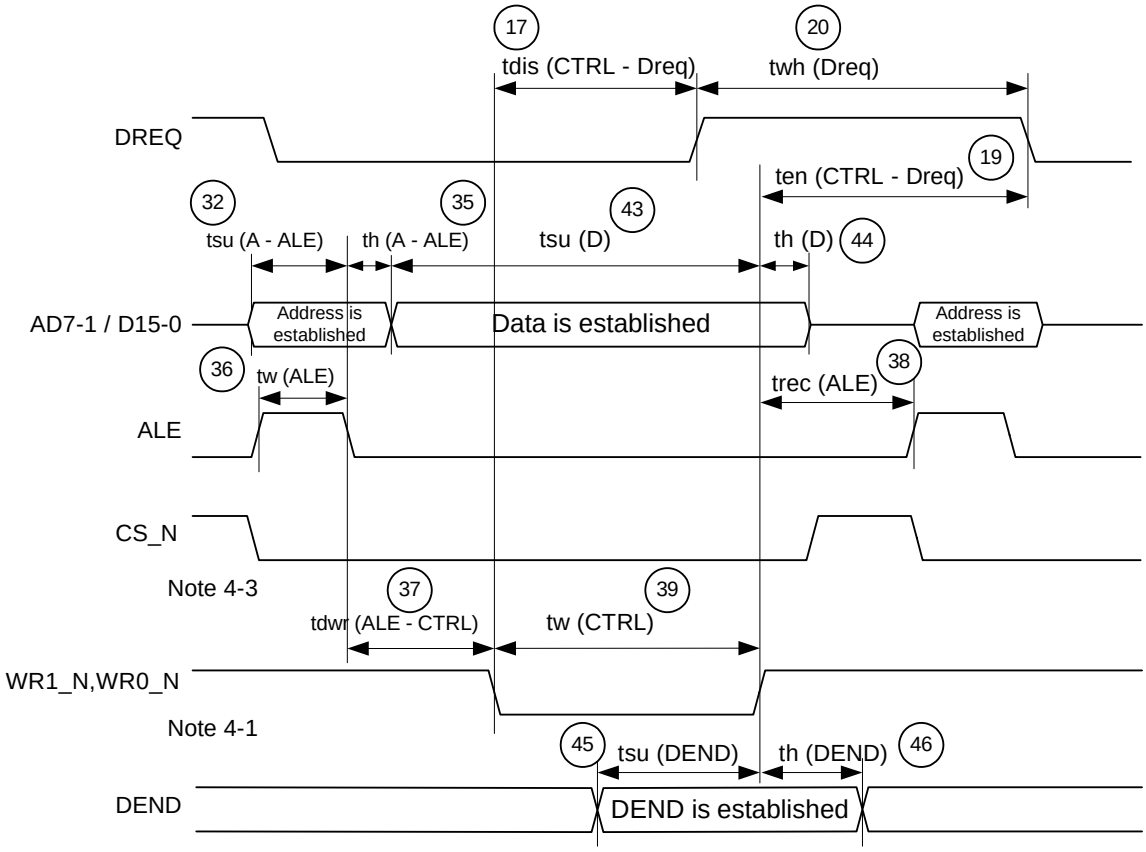
(1) The tr and tf are judged by the transition time of the 10% amplitude point and 90% amplitude point respectively.

(2) The electrostatic capacity CL includes the stray capacitance of the wire connection and the input capacitance of the probe.

4.7 Switching Characteristics (VIF = 3.0~3.6V or 1.7~2.0V)

Symbol	Parameter	Conditions, others	Limits			Unit	Refer No.
			Min.	Typ.	Max.		
ta (A)	Address access time	CL=50pF			40	ns	1
tv (A)	Data valid time after address	CL=10pF	2			ns	2
ta (CTRL - D)	Data access time after control	CL=50pF			30	ns	3
tv (CTRL - D)	Data valid time after control	CL=10pF	2			ns	4
ten (CTRL - D)	Data output enable time after control		2			ns	5
tdis (CTRL - D)	Data output disable time after control	CL=50pF			30	ns	6
ta (CTRL - DV)	Data access time after control when set to split bus (DMA Interface) Obus=0	CL=30pF			30	ns	9
tv (CTRL – DV)	Data valid time after control when set to split bus (DMA Interface) Obus=0	CL=10pF	2			ns	10
ta (CTRL - DendV)	DEND output access time after control	CL=30pF			30	ns	11
tv (CTRL - DendV)	DEND output valid time after control	CL=10pF	2			ns	12
ta (CTRL - Dend)	DEND output access time after control when set to split bus (DMA Interface) Obus=1	CL=30pF			30	ns	13
tv (CTRL - DendV)	DEND output valid time after control when set to split bus (DMA Interface) Obus=1	CL=10pF	2			ns	14
ten (CTRL - DendV)	DEND output enable time after control when set to split bus (DMA Interface) Obus=1		2			ns	15
tdis (CTRL-DendV)	DEND output disable time after control when set to split bus (DMA Interface) Obus=1	CL=30pF			30	ns	16
tdis (CTRL – Dreq)	DREQ output disable time after control				70	ns	17
tdis (CTRLH –Dreq)	DREQ output disable time after control when completed transfer End signal by the DEND signal				70	ns	18
ten (CTRL – Dreq)	DREQ output enable time after control		30			ns	19
twh (Dreq)	DREQ output high pulse width		20		50	ns	20
td (CTRL - INT)	INT output negate delay time				250	ns	21
twh (INT)	INT output high pulse width		650			ns	22
td (DREQ - DV)	Data access time after starting assert the DREQ signal when set to split bus Obus=0				0	ns	23
td (DREQ - DendV)	DEND output access time after starting assert the DREQ signal when set to split bus Obus=0				0	ns	24

4.9.12 DMA transfer write timing (when set to multiplex bus and cycle steal transfer)



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