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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 16x12b, 21x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	66-UFBGA, WLCSP
Supplier Device Package	66-WLCSP (3.8x4.2)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f383rcy6tr

Contents

3.12 12-bit analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, V_{BAT} voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 63: Temperature sensor calibration values on page 101*.

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

Table 3. Capacitive sensing GPIOs available on STM32F383xx devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 4. No. of capacitive sensing channels available on STM32F383xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F383Cx	STM32F383Rx	STM32F383Vx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

3.17 Timers and watchdogs

The STM32F383xx includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complemen-tary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7, TIM18	16-bit	Up	Any integer between 1 and 65536	Yes	0	0

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I^2C interfaces can be served by the DMA controller

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F383xx I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I2S interfaces can operate in half-duplex mode only.

Refer to *Table 9* for the features between SPI1, SPI2 and SPI3.

Table 9. STM32F383xx SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	X	X	X
TI mode	X	X	X
I2S full-duplex mode			

1. X = supported.

3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.23 Controller area network (CAN)

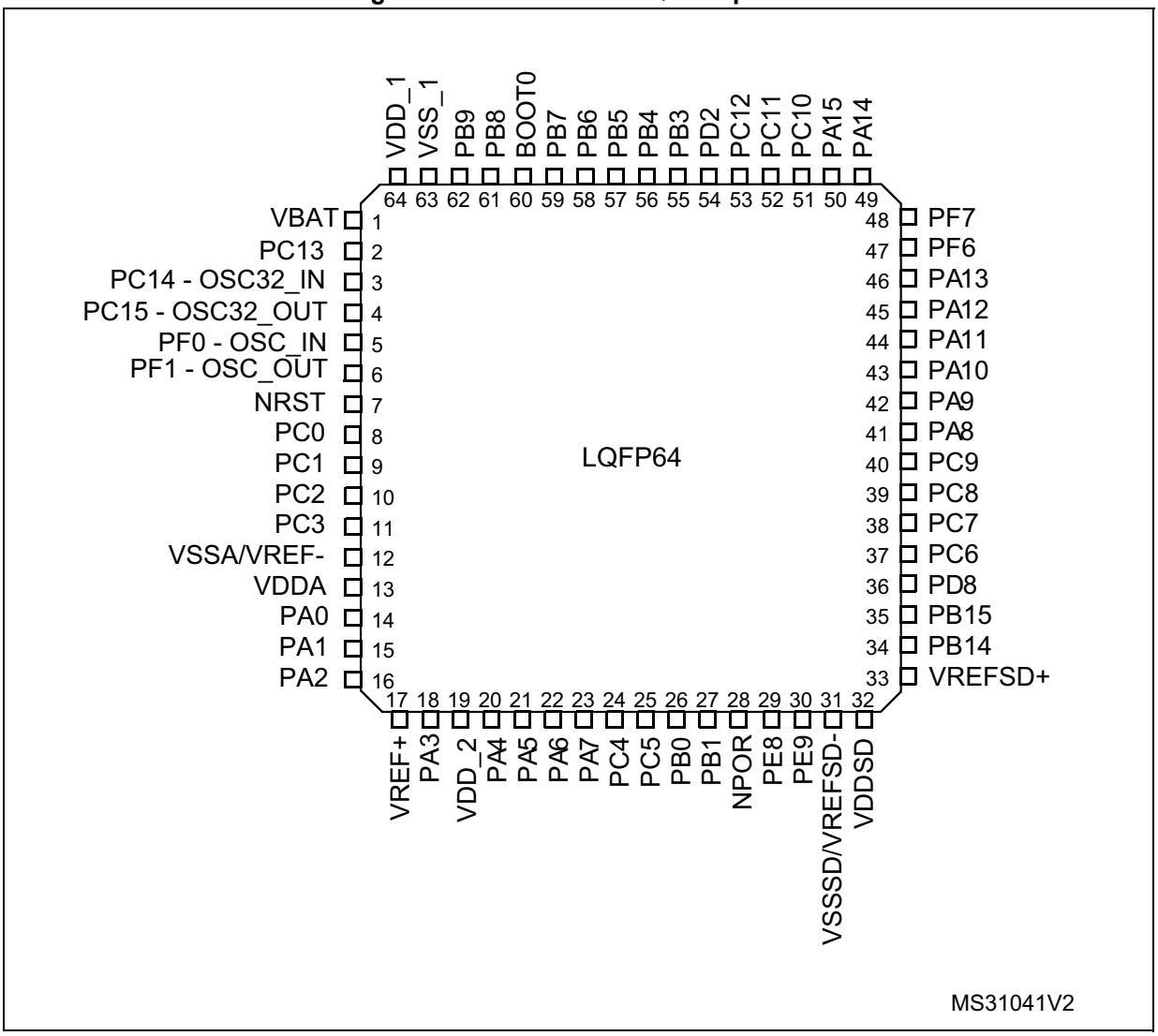
The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

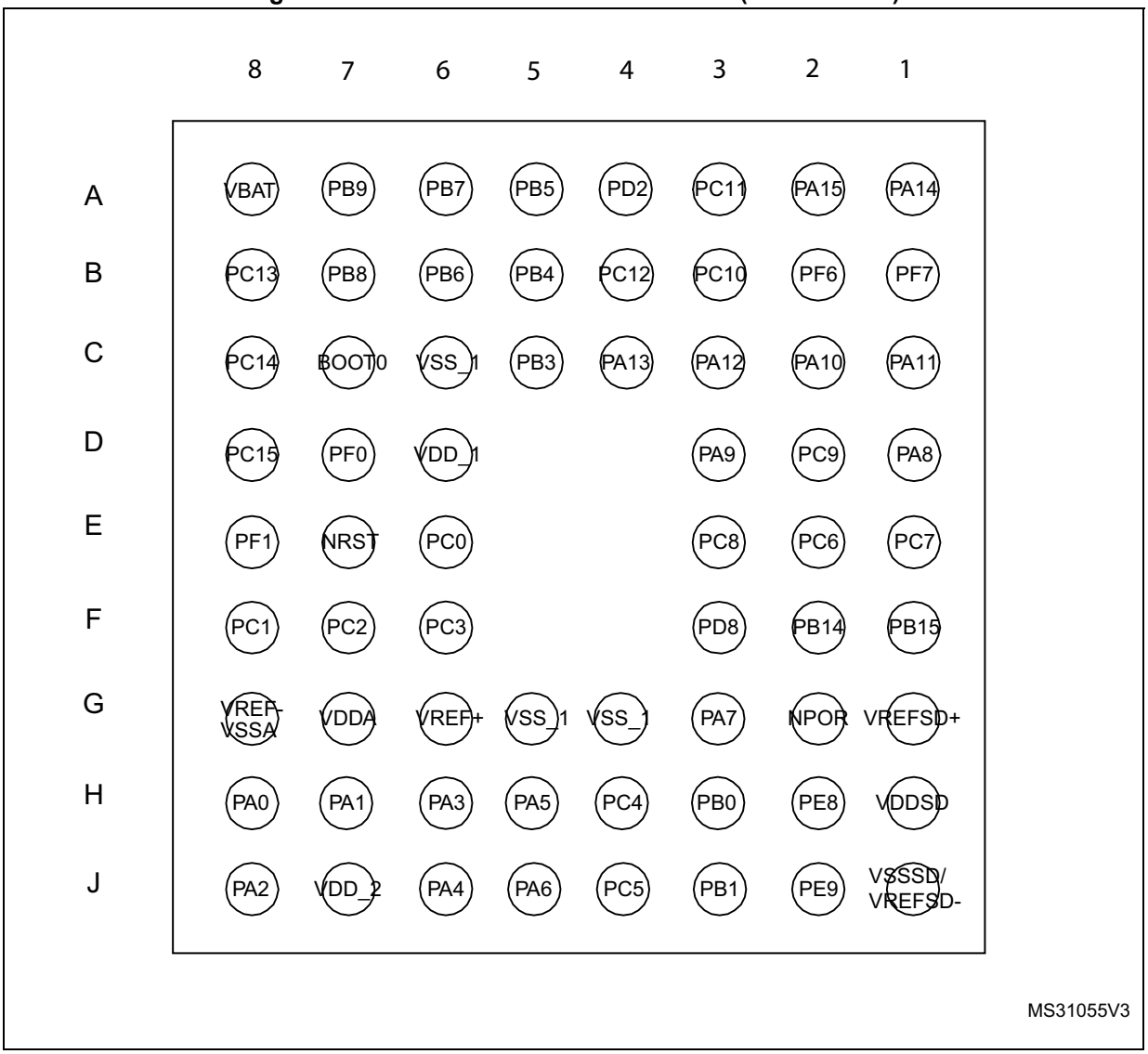
The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 3. STM32F383xx LQFP64 pinout



1. The above figure shows the package top view.

Figure 6. STM32F383xx WLCSP66 ballout (bottom view)



1. The above figure shows the package bottom view.

Table 11. STM32F383xx pin definitions

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
1	B2				PE2	I/O	(1)	FT	TSC_G7_IO1, TRACECLK	
2	A1				PE3	I/O	(1)	FT	TSC_G7_IO2, TRACED0	
3	B1				PE4	I/O	(1)	FT	TSC_G7_IO3, TRACED1	
4	C2				PE5	I/O	(1)	FT	TSC_G7_IO4, TRACED2	
5	D2				PE6	I/O	(1)	FT	TRACED3	WKUP3, RTC_TAMPER3
6	E2	1	1	A8	VBAT	S	(2)		Backup power supply	
7	C1	2	2	B8	PC13	I/O		TC		WKUP2, ALARM_OUT, CALIB_OUT, TIMESTAMP, RTC_TAMPER1
8	D1	3	3	C8	PC14 - OSC32_IN	I/O		TC		OSC32_IN
9	E1	4	4	D8	PC15 - OSC32_ OUT	I/O		TC		OSC32_OUT
10	F2				PF9	I/O	(1)	FT	TIM14_CH1	
11	G2				PF10	I/O	(1)	FT		
12	F1	5	5	D7	PF0 - OSC_IN	I/O		FTf	I2C2_SDA	OSC_IN
13	G1	6	6	E8	PF1 - OSC_OUT	I/O		FTf	I2C2_SCL	OSC_OUT
14	H2	7	7	E7	NRST	I/O		RST	Device reset input / internal reset output (active low)	
15	H1	8		E6	PC0	I/O	(1)	TTa	TIM5_CH1_ETR	ADC_IN10
16	J2	9		F8	PC1	I/O	(1)	TTa	TIM5_CH2	ADC_IN11
17	J3	10		F7	PC2	I/O	(1)	TTa	SPI2_MISO/I2S2_MCK, TIM5_CH3	ADC_IN12
18	K2	11		F6	PC3	I/O	(1)	TTa	SPI2_MOSI/I2S2_SD, TIM5_CH4	ADC_IN13
19	J1				PF2	I/O	(1)	FT	I2C2_SMBA	
20	K1	12	8	G8	VSSA/ VREF-	S			Analog ground	

Table 11. STM32F383xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
63	E12	37		E2	PC6	I/O	(1)	FT	SPI1_NSS/I2S1_WS, TIM3_CH1	
64	E11	38		E1	PC7	I/O	(1)	FT	SPI1_SCK/I2S1_CK, TIM3_CH2	
65	E10	39		E3	PC8	I/O	(1)	FT	SPI1_MISO/I2S1_MCK, TIM3_CH3	
66	D12	40		D2	PC9	I/O	(1)	FT	SPI1_MOSI/I2S1_SD, TIM3_CH4	
67	D11	41	29	D1	PA8	I/O		FT	SPI2_SCK/I2S2_CK, I2C2_SMBA, USART1_CK, TIM4_ETR, TIM5_CH1_ETR, CLK_CLKOUT	
68	D10	42	30	D3	PA9	I/O		FTf	SPI2_MISO/I2S2_MCK, I2C2_SCL, USART1_TX, TIM2_CH3, TIM15_BKIN, TIM13_CH1, TSC_G4_IO1	
69	C12	43	31	C2	PA10	I/O		FTf	SPI2_MOSI/I2S2_SD, I2C2_SDA, USART1_RX, TIM2_CH4, TIM17_BKIN, TIM14_CH1, TSC_G4_IO2	
70	B12	44	32	C1	PA11	I/O		FT	SPI2_NSS/I2S2_WS, SPI1_NSS/I2S1_WS, USART1_CTS, CAN_RX, TIM4_CH1, TIM5_CH2, COMP1_OUT	
71	A12	45	33	C3	PA12	I/O		FT	SPI1_SCK/I2S1_CK, USART1_RTS, CAN_TX, TIM16_CH1, TIM4_CH2, TIM5_CH3, COMP2_OUT	
72	A11	46	34	C4	PA13	I/O		FT	SPI1_MISO/I2S1_MCK, USART3_CTS, IR_OUT, TIM16_CH1N, TIM4_CH3, TIM5_CH4, G4_IO3, SWDIO-JTMS	
73	C11	47	35	B2	PF6	I/O		FTf	SPI1_MOSI, I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL	
74	F11				VSS_3	S	(1)		Ground	

Table 12. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0		TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1				USART2_CTS	COMP1_OUT			TIM19_CH1		EVENTOUT
PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	TSC_G1_IO2			SPI3_SCK/I2S3_CK	USART2_RTS		TIM15_CH1N		TIM19_CH2		EVENTOUT
PA2		TIM2_CH3	TIM5_CH3	TSC_G1_IO3			SPI3_MISO/I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1		TIM19_CH3		EVENTOUT
PA3		TIM2_CH4	TIM5_CH4	TSC_G1_IO4			SPI3_MOSI/I2S3_SD	USART2_RX		TIM15_CH2		TIM19_CH4		EVENTOUT
PA4			TIM3_CH2	TSC_G2_IO1		SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK			TIM12_CH1			EVENTOUT
PA5		TIM2_CH1_ETR		TSC_G2_IO2		SPI1_SCK/I2S1_CK		CEC		TIM14_CH1	TIM12_CH2			EVENTOUT
PA6		TIM16_CH1	TIM3_CH1	TSC_G2_IO3		SPI1_MISO/I2S1_MCK			COMP1_OUT	TIM13_CH1				EVENTOUT
PA7		TIM17_CH1	TIM3_CH2	TSC_G2_IO4		SPI1_MOSI/I2S1_SD			COMP2_OUT	TIM14_CH1				EVENTOUT
PA8	MCO		TIM5_CH1_ETR		I2C2_SMBA	SPI2_SCK/I2S2_CK		USART1_CK			TIM4_ETR			EVENTOUT
PA9			TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO/I2S2_MCK		USART1_TX		TIM15_BKIN	TIM2_CH3			EVENTOUT
PA10		TIM17_BKIN		TSC_G4_IO2	I2C2_SDA	SPI2_MOSI/I2S2_SD		USART1_RX		TIM14_CH1	TIM2_CH4			EVENTOUT
PA11			TIM5_CH2			SPI2_NSS/I2S2_WS	SPI1_NSS/I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1			EVENTOUT
PA12		TIM16_CH1	TIM5_CH3				SPI1_SCK/I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2			EVENTOUT

Table 12. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	SWDIO -JTMS	TIM16_ CH1N	TIM5_ CH4	TSC_ G4_IO3		IR-OUT	SPI1_MISO /I2S1_MCK	USART3_CTS			TIM4_ CH3			EVENT OUT
PA14	SWCLK -JTCK			TSC_ G4_IO4	I2C1_ SDA						TIM12 _CH1			EVENT OUT
PA15	JTDI	TIM2_ CH1_ETR		TSC_ SYNC	I2C1_ SCL	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS				TIM12 _CH2			EVENT OUT

Table 16. Alternate functions for port PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0		EVENTOUT	TIM4_ETR					USART1_TX
PE1		EVENTOUT						USART1_RX
PE2	TRACECLK	EVENTOUT		TSC_G7_IO1				
PE3	TRACED0	EVENTOUT		TSC_G7_IO2				
PE4	TRACED1	EVENTOUT		TSC_G7_IO3				
PE5	TRACED2	EVENTOUT		TSC_G7_IO4				
PE6	TRACED3	EVENTOUT						
PE7		EVENTOUT						
PE8		EVENTOUT						
PE9		EVENTOUT						
PE10		EVENTOUT						
PE11		EVENTOUT						
PE12		EVENTOUT						
PE13		EVENTOUT						
PE14		EVENTOUT						
PE15		EVENTOUT						USART3_RX

5 Memory mapping

Figure 7. STM32F383xx memory map

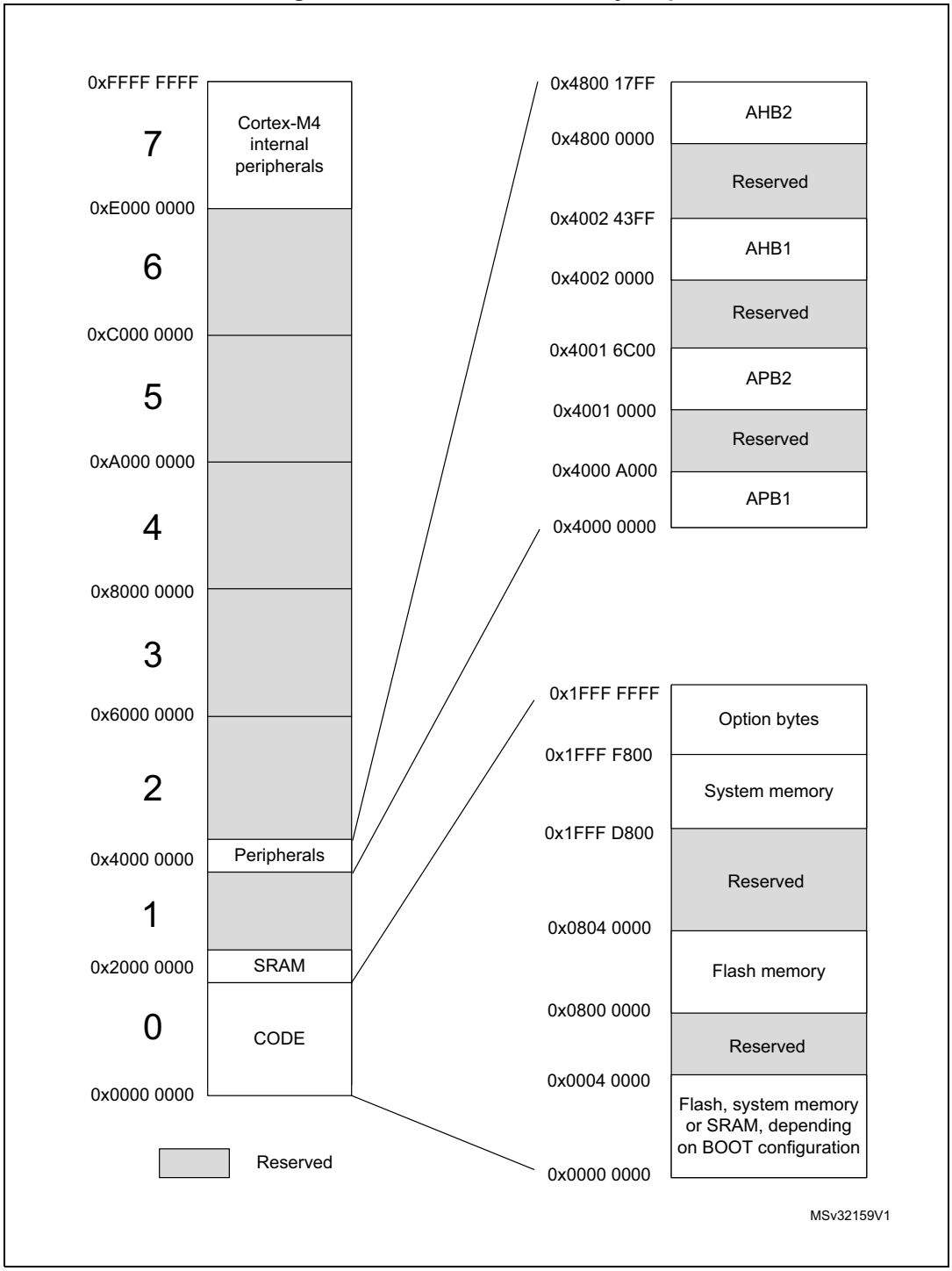


Table 18. STM32F383xx peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 49: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on V_{DD} supply and also on V_{DDSDx} supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 33: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = 1.8 V, V_{DDA} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode		3.6	5.21	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	After WFE instruction	6		CPU clock cycles

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

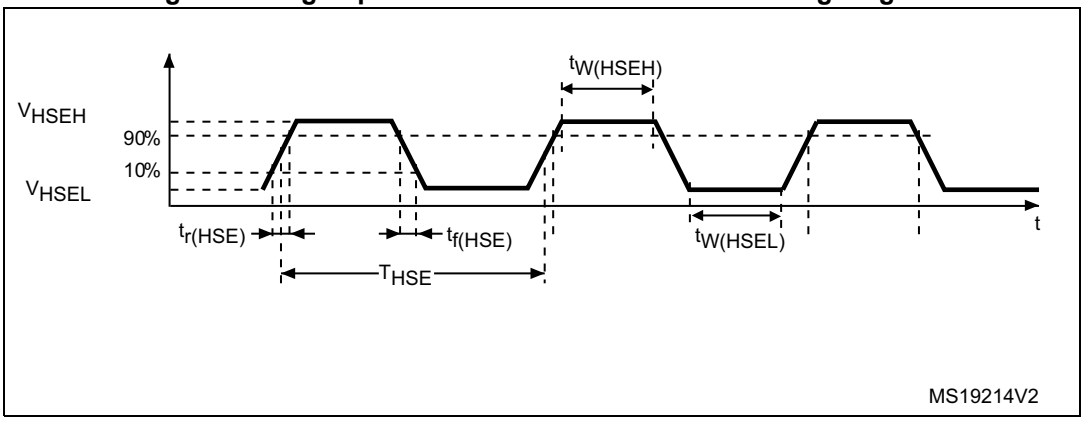
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 35. High-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage		0.7 V_{DD}		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 12. High-speed external clock source AC timing diagram



Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- The PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 49 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology parameters. The coverage of these requirements is shown in *Figure 17* for standard I/Os, and in *Figure 18* for 5 V tolerant I/Os.

Figure 17. TC and TTa I/O input characteristics

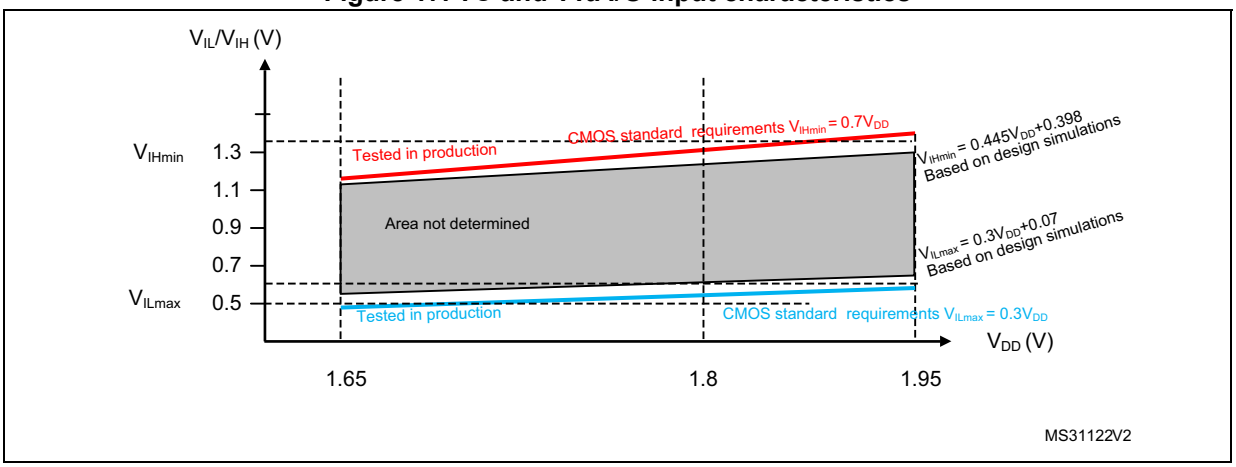
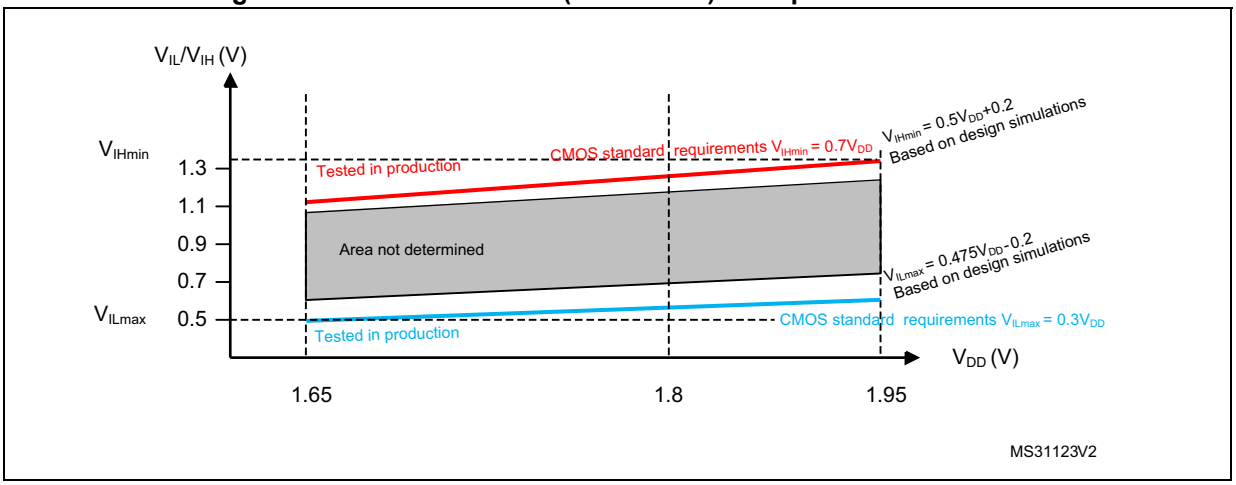


Figure 18. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

6.3.15 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 54*. Refer also to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 54. I2C characteristics(1)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4	-	0.6	-	0.26	-	µs
tr	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF

1. The I2C characteristics are the requirements from the I2C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

6.3.18 Comparator characteristics

Table 62. Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage			1.65	-	3.6	V
V_{IN}	Comparator input voltage range			0	-	V_{DDA}	V
V_{BG}	Scaler input voltage			-	1.2	-	V
V_{SC}	Scaler offset voltage			-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down			-	-	0.1	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	µs
		Medium power mode		-	0.3	0.6	µs
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	ns
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	µs
		Medium power mode		-	0.3	1.2	µs
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	ns
V_{offset}	Comparator offset error			-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient			-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	µA
		Medium power mode		-	10	15	µA
		High speed mode		-	75	100	µA