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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc938fa-129

4. Block diagram

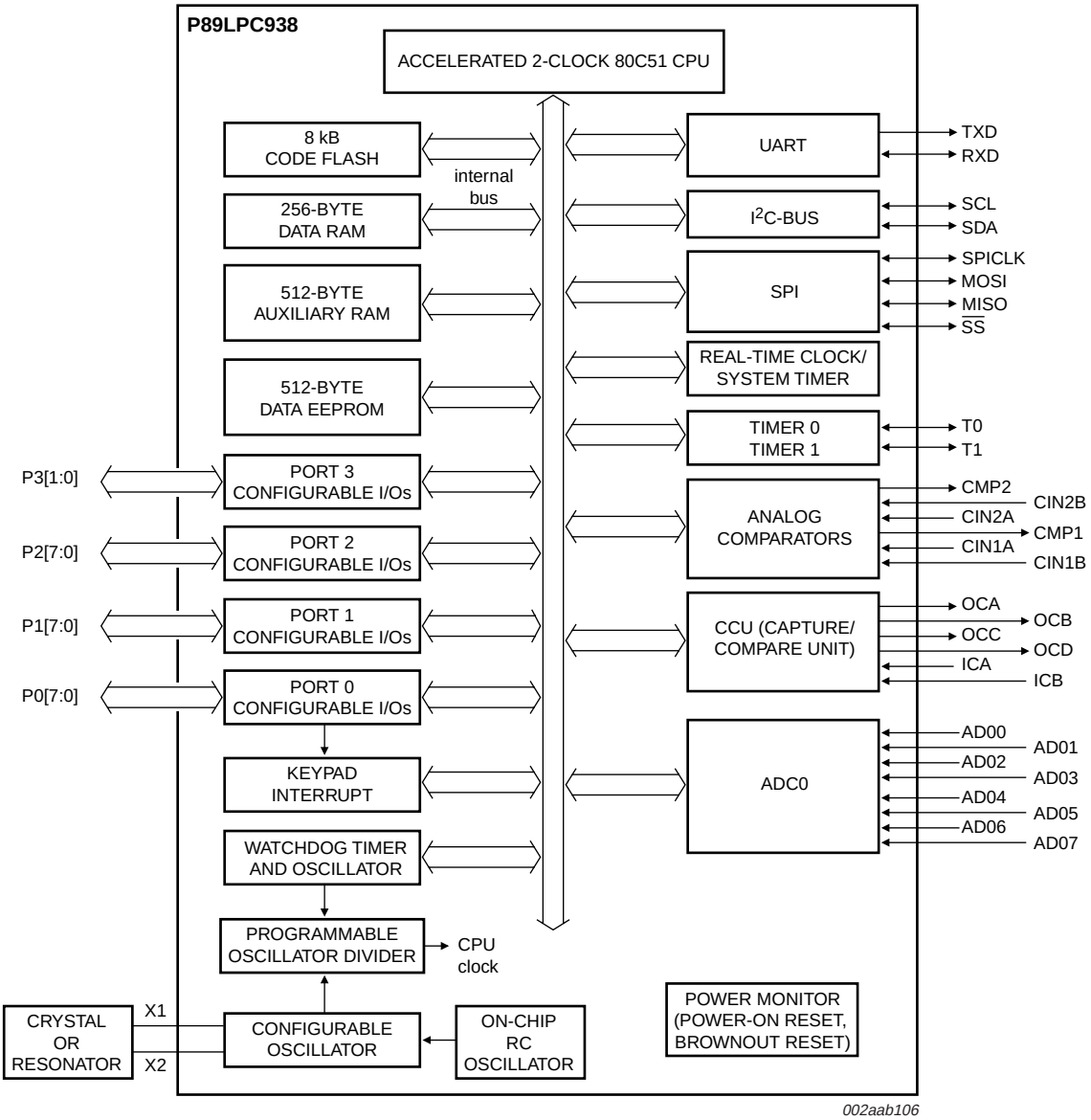


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

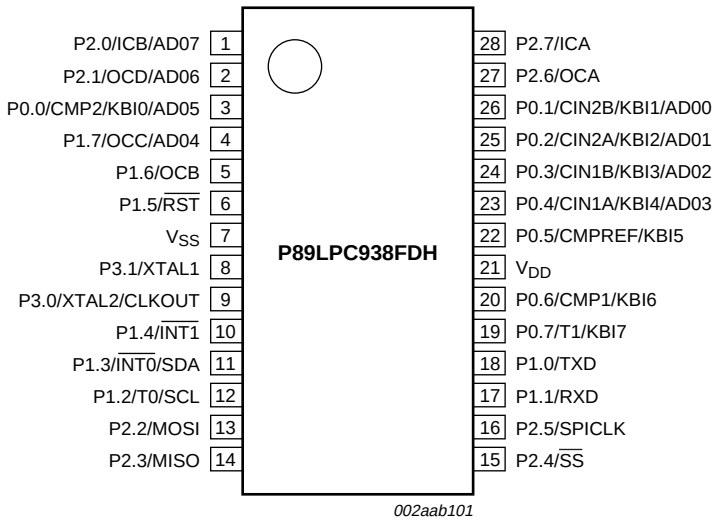


Fig 3. TSSOP28 pin configuration.

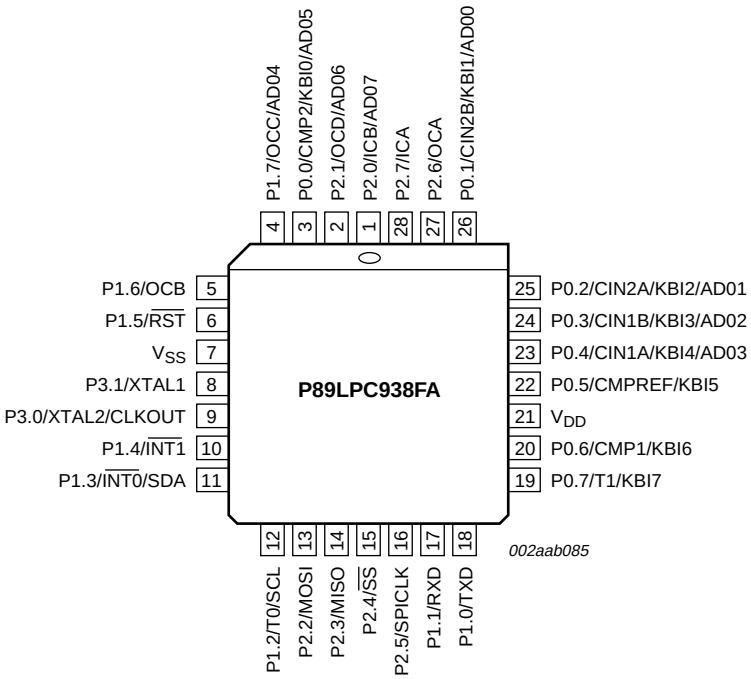


Fig 4. PLCC28 pin configuration.

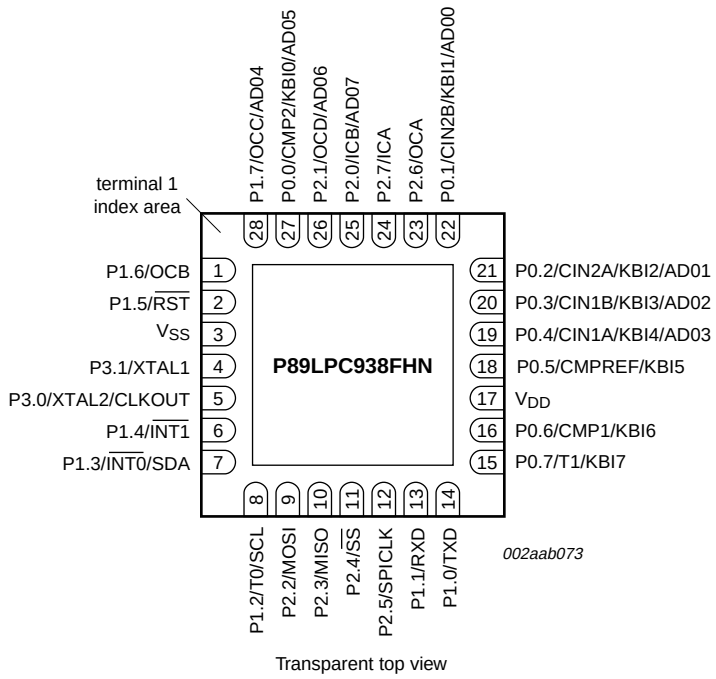


Fig 5. HVQFN28 pin configuration (top view).

6.2 Pin description

Table 3: Pin description

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.0 to P0.7			I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 "Port configurations" and Table 10 "DC electrical characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD05	3	27	I/O	**P0.0 —** Port 0 bit 0.
			O	**CMP2 —** Comparator 2 output.
			I	**KBI0 —** Keyboard input 0.
			I	**AD05 —** ADC0 channel 5 analog input.
P0.1/CIN2B/ KBI1/AD00	26	22	I/O	**P0.1 —** Port 0 bit 1.
			I	**CIN2B —** Comparator 2 positive input B.
			I	**KBI1 —** Keyboard input 1.
			I	**AD00 —** ADC0 channel 0 analog input.

Table 3: Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.2/CIN2A/ KBI2/AD01	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
			I	**AD01 —** ADC0 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD02	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.
			I	**AD02 —** ADC0 channel 2 analog input.
P0.4/CIN1A/ KBI4/AD03	23	19	I/O	**P0.4 —** Port 0 bit 4.
			I	**CIN1A —** Comparator 1 positive input A.
			I	**KBI4 —** Keyboard input 4.
			I	**AD03 —** ADC0 channel 3 analog input.
P0.5/CMPREF/ KBI5	22	18	I/O	**P0.5 —** Port 0 bit 5.
			I	**CMPREF —** Comparator reference (negative) input.
			I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	20	16	I/O	**P0.6 —** Port 0 bit 6.
			O	**CMP1 —** Comparator 1 output.
			I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	19	15	I/O	**P0.7 —** Port 0 bit 7.
			I/O	**T1 —** Timer/counter 1 external count input or overflow output.
			I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7			I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 “Port configurations” and Table 10 “DC electrical characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	14	I/O	**P1.0 —** Port 1 bit 0.
			O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	17	13	I/O	**P1.1 —** Port 1 bit 1.
			I	**RXD —** Receiver input for the serial port.
P1.2/T0/SCL	12	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
			I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
			I/O	**SCL —** I^2C serial clock input/output.

Table 4: P89LPC938 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AD0CON	ADC0 control register	97H	ENBI0	ENADCI 0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	00000000
AD0INS	ADC0 input select	A3H	ADI07	ADI06	ADI05	ADI04	ADI03	ADI02	ADI01	ADI00	00	00000000
AD0MOD A	ADC0 mode register A	C0H	BNDI0	BURST0	SCC0	SCAN0	-	-	-	-	00	00000000
AD0MOD B	ADC0 mode register B	A1H	CLK2	CLK1	CLK0	-	-	-	-	-	00	000x0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0 [1]	Baud rate generator rate low	BEH									00	00000000
BRGR1 [1]	Baud rate generator rate high	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00 [1]	xxxxxx00
CCCRA	Capture compare A control register	EAH	ICECA2	ICECA1	ICECA0	ICESA	ICNFA	FCOA	OCMA1	OCMA0	00	00000000
CCCRB	Capture compare B control register	EBH	ICECB2	ICECB1	ICECB0	ICESB	ICNFB	FCOB	OCMB1	OCMB0	00	00000000
CCCRC	Capture compare C control register	ECH	-	-	-	-	-	FCOC	OCMC1	OCMC0	00	xxxxx000
CCCRD	Capture compare D control register	EDH	-	-	-	-	-	FCOD	OCMD1	OCMD0	00	xxxxx000
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 [2]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 [2]	xx000000
DEECON	Data EEPROM control register	F1H	EEIF	HVERR	ECTL1	ECTL0	-	-	-	EADR8	0E	00001110
DEEDAT	Data EEPROM data register	F2H									00	00000000
DEEADR	Data EEPROM address register	F3H									00	00000000
DIVM	CPU clock divide-by-M control	95H									00	00000000

Table 5: P89LPC938 extended special function registers

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
ADC0HBND	ADC0 high _boundary register, left (MSB)	FFEFh			FF	11111111
ADC0LBND	ADC0 low_boundary register (MSB)	FFEEh			00	00000000
AD0DAT0R	ADC0 data register 0, right (LSB)	FFFEh	AD0DAT0[7:0]		00	00000000
AD0DAT0L	ADC0 data register 0, left (MSB)	FFFFh	AD0DAT0[9:2]		00	00000000
AD0DAT1R	ADC0 data register 1, right (LSB)	FFFCh	AD0DAT1[7:0]		00	00000000
AD0DAT1L	ADC0 data register 1, left (MSB)	FFFDh	AD0DAT1[9:2]		00	00000000
AD0DAT2R	ADC0 data register 2, right (LSB)	FFFAh	AD0DAT2[7:0]		00	00000000
AD0DAT2L	ADC0 data register 2, left (MSB)	FFFBh	AD0DAT2[9:2]		00	00000000
AD0DAT3R	ADC0 data register 3, right (LSB)	FFF8h	AD0DAT3[7:0]		00	00000000
AD0DAT3L	ADC0 data register 3, left (MSB)	FFF9h	AD0DAT3[9:2]		00	00000000
AD0DAT4R	ADC0 data register 4, right (LSB)	FFF6h	AD0DAT4[7:0]		00	00000000
AD0DAT4L	ADC0 data register 4, left (MSB)	FFF7h	AD0DAT4[9:2]		00	00000000
AD0DAT5R	ADC0 data register 5, right (LSB)	FFF4h	AD0DAT5[7:0]		00	00000000
AD0DAT5L	ADC0 data register 5, left (MSB)	FFF5h	AD0DAT5[9:2]		00	00000000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2h	AD0DAT6[7:0]		00	00000000
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3h	AD0DAT6[9:2]		00	00000000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0h	AD0DAT7[7:0]			
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1h	AD0DAT7[9:2]			
BNDSTA0	ADC0 boundary status register	FFEDh				

The frequency of this clock output is ½ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.4 On-chip RC oscillator option

The P89LPC938 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies.

7.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

7.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 18 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

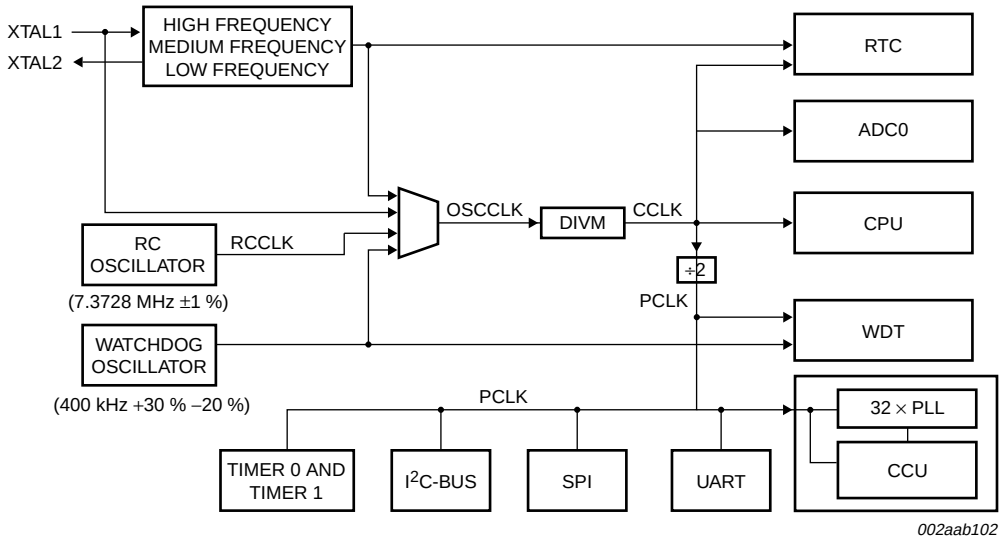


Fig 6. Block diagram of oscillator control.

7.7 CCLK wake-up delay

The P89LPC938 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

7.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.9 Low power select

The P89LPC938 is designed to run at 12 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.10 Memory organization

The various P89LPC938 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  ‘External’ Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the SPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC938 has 512 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.

7.14.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 10 “DC electrical characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC938 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 10 “DC electrical characteristics” for specifications.

7.14.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.15 Power reduction modes

The P89LPC938 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC938 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention voltage (V_{DDR}). This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: brownout detect, watchdog timer, comparators (note that comparators can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to '1', enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, The RPE selection is overridden and this pin will always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1);
- Power-on detect;
- Brownout detect;
- Watchdog timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.16.1 Reset vector

Following reset, the P89LPC938 will fetch instructions from either address 0000h or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00h.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC938 User's Manual*). Otherwise, instructions will be fetched from address 0000H.

7.20.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

7.20.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.20.5 "Baud rate generator and selection").

7.20.5 Baud rate generator and selection

The P89LPC938 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 12). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses OSCCLK.

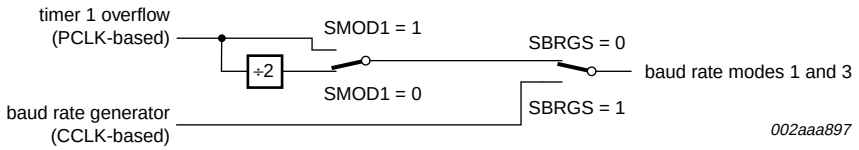


Fig 12. Baud rate sources for UART (Modes 1, 3).

7.20.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is '1', framing errors can be made available in SCON.7 respectively. If SMOD0 is '0', SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is '0'.

7.20.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.20.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

7.20.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

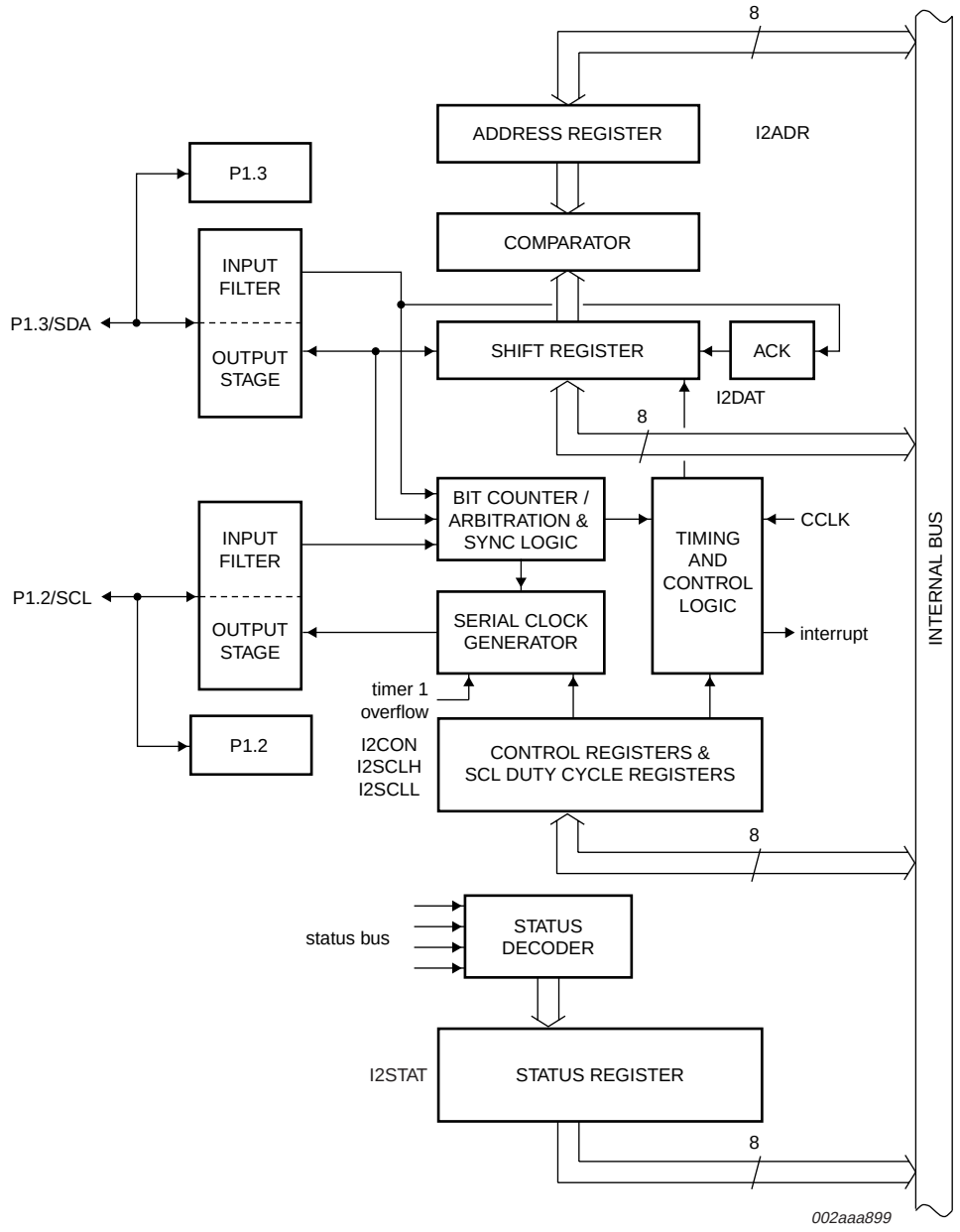


Fig 14. I²C-bus serial interface block diagram.

7.22.1 Typical SPI configurations

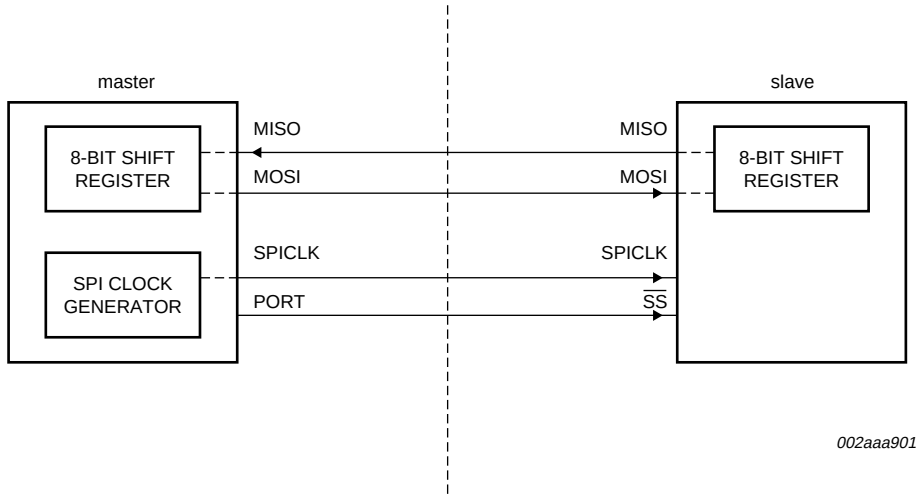


Fig 16. SPI single master single slave configuration.

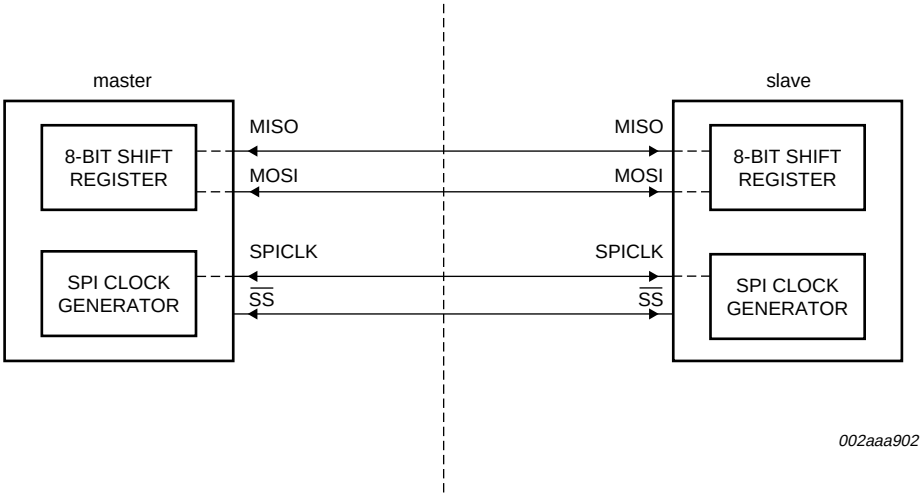


Fig 17. SPI dual device configuration, where either can be a master or a slave.

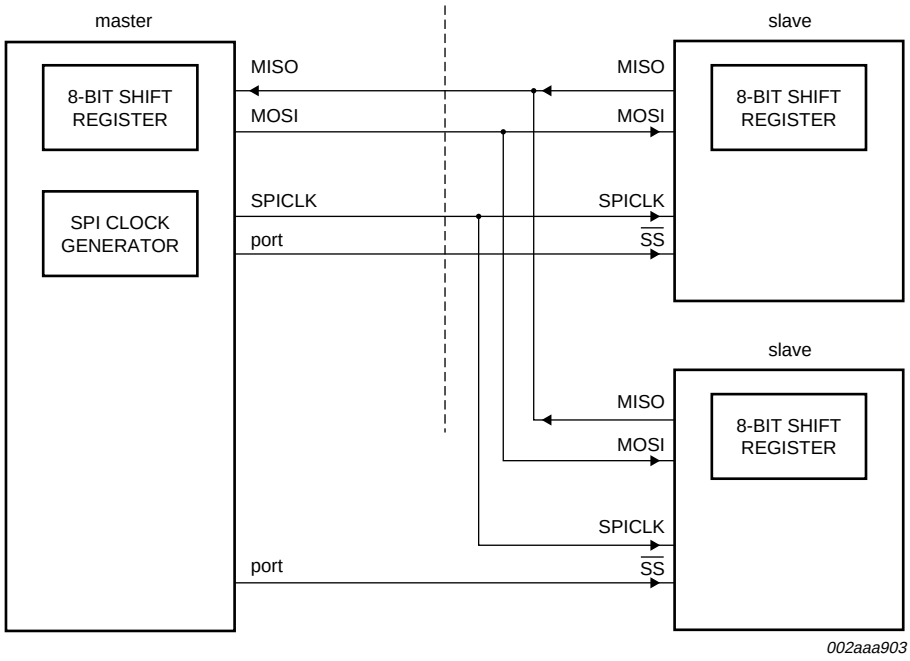


Fig 18. SPI single master multiple slaves configuration.

7.27 Data EEPROM

The P89LPC938 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- **Byte Mode:** In this mode, data can be read and written one byte at a time.
- **Row Fill:** In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00h.
- **Sector Fill:** In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00h.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

7.28 Flash program memory

7.28.1 General description

The P89LPC938 Flash memory provides in-circuit electrical erasure and programming. The Flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any Flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC938 Flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC938 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

7.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing In-System Programming via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided Flash loader code to reside anywhere in the Flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the Flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

7.28.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC938 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.28.4 Using Flash as data storage

The Flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.28.5 Flash programming and erasing

Four different methods of erasing or programming of the Flash are available. The Flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The Flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

7.28.6 ICP

In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC938 through a two-wire serial interface. The Philips In-Circuit Programming facility has made in-circuit programming in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC938 User's Manual*.

7.28.7 IAP

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips In-Application Programming has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of Flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00 to FEFF hex, thereby not conflicting with the user program memory space.

Table 10: DC electrical characteristics *...continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, V_{DD} = 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 9 “Limiting values” on page 50 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] Pin capacitance is characterized but not tested.

[6] Measured with port in quasi-bidirectional mode.

[7] Measured with port in high-impedance mode.

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

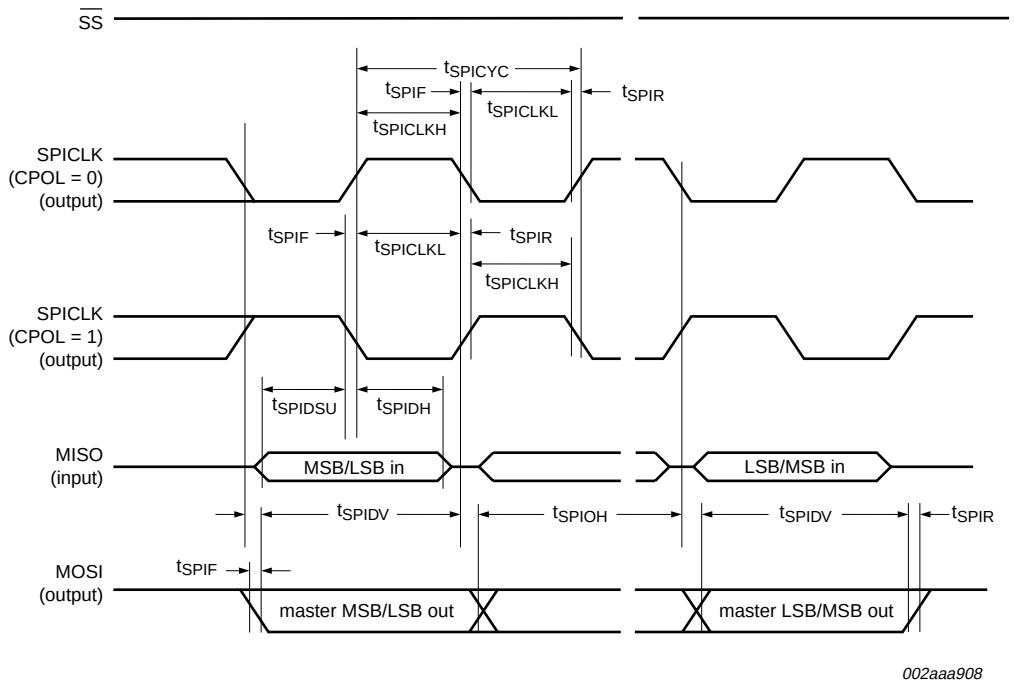


Fig 24. SPI master timing (CPHA = '0').

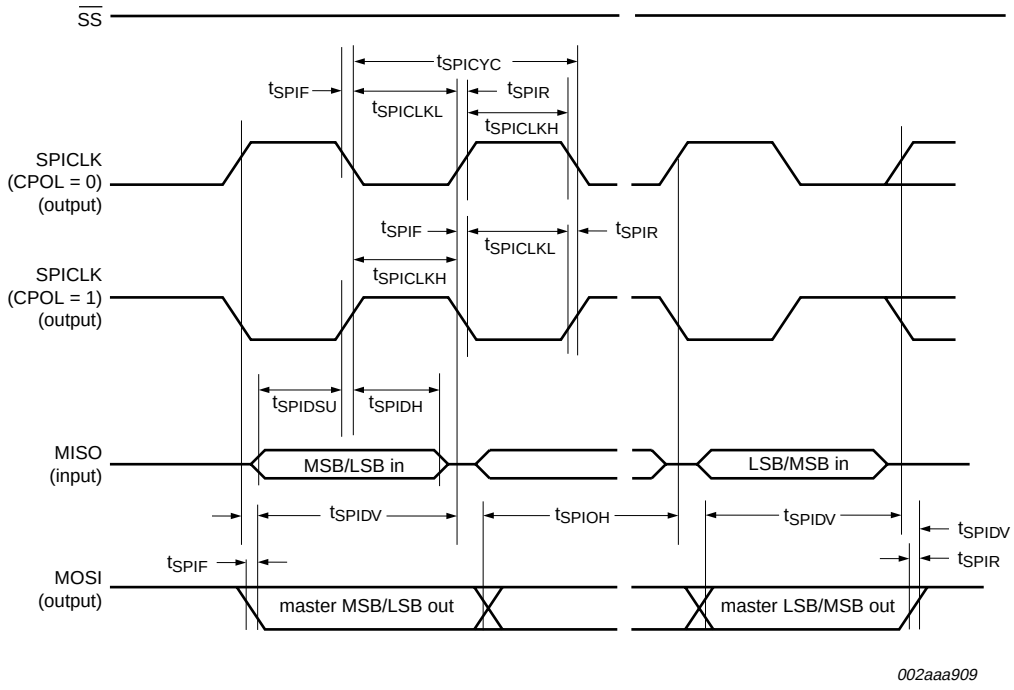
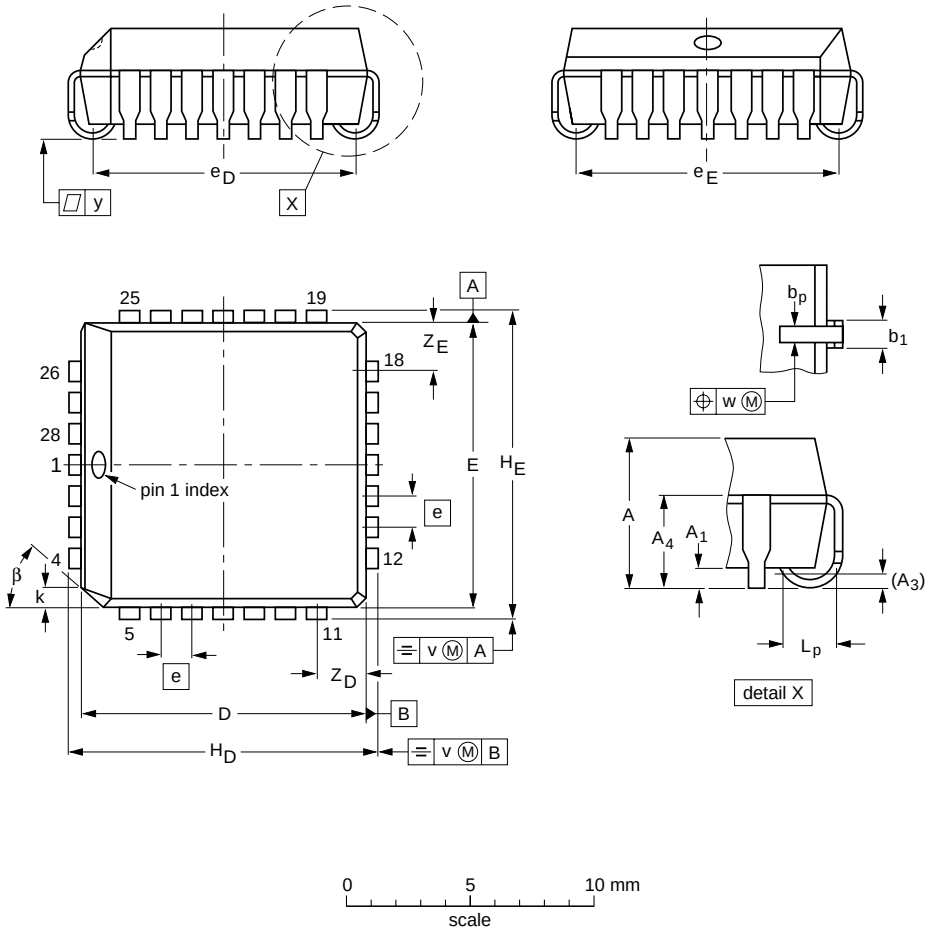


Fig 25. SPI master timing (CPHA = '1').

13. Package outline

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 29. Package outline SOT261-2 (PLCC28).