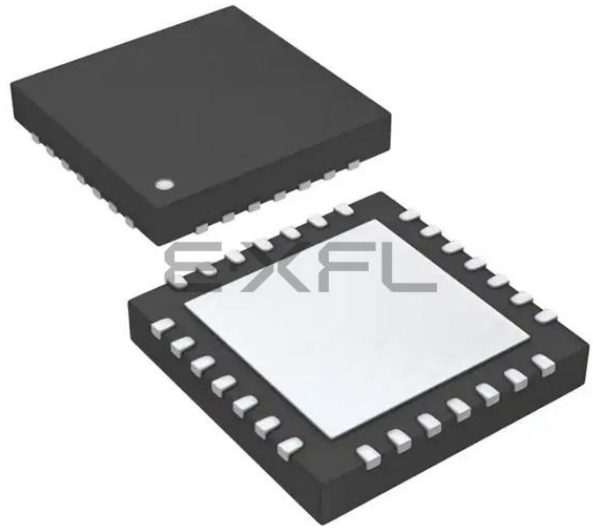

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-HVQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc938fhn-151

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial Flash ICP allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial Flash ISP allows coding while the device is mounted in the end application.
- In-Application Programming of the Flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed Flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC938 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

4. Block diagram

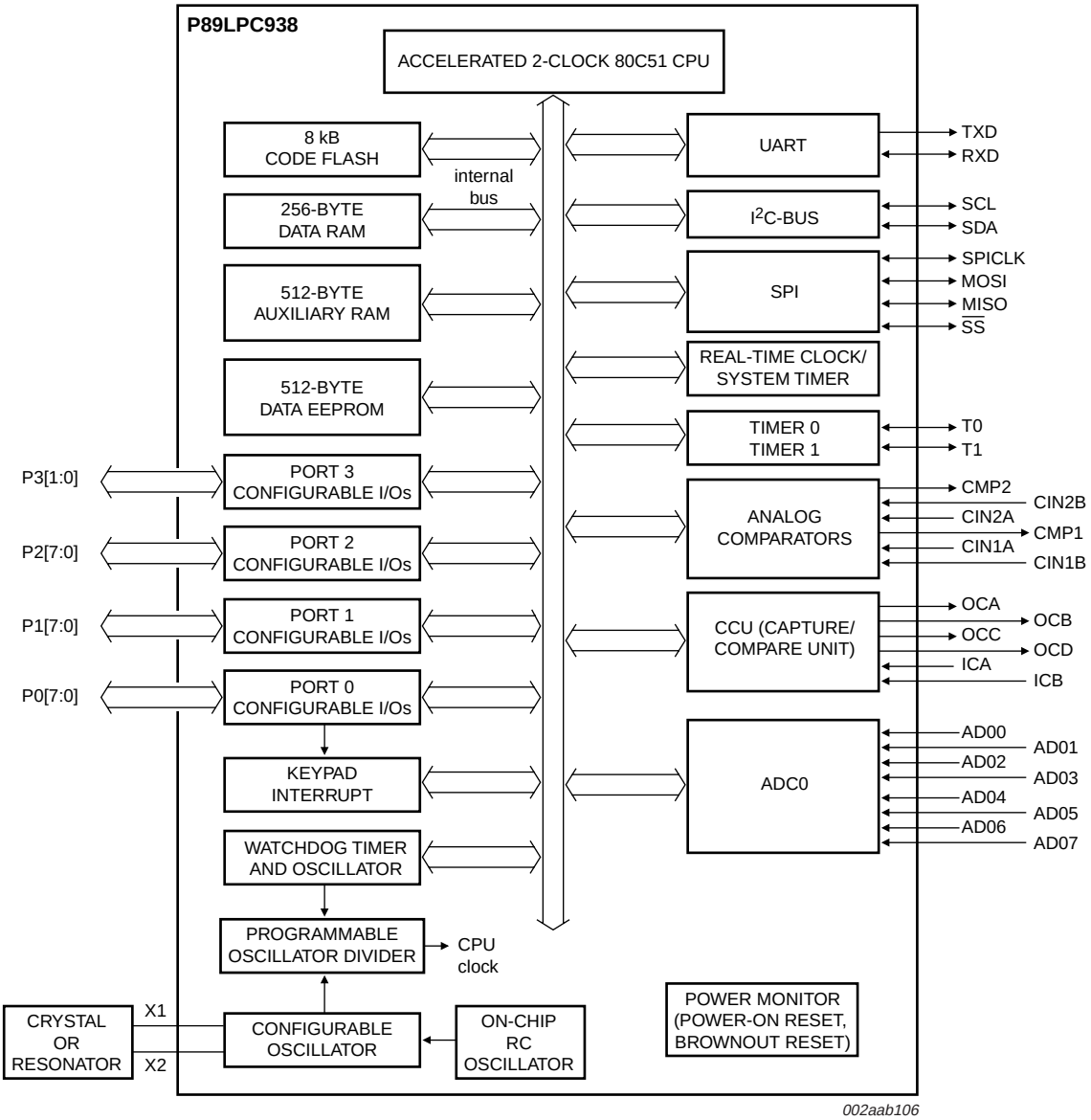

Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

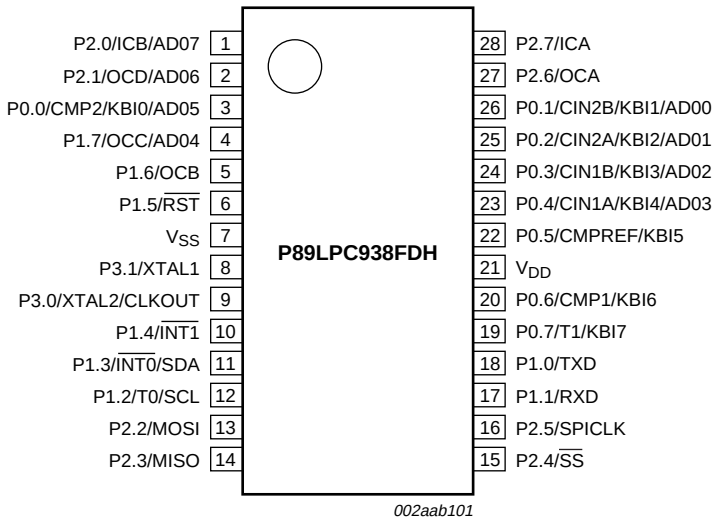

Fig 3. TSSOP28 pin configuration.

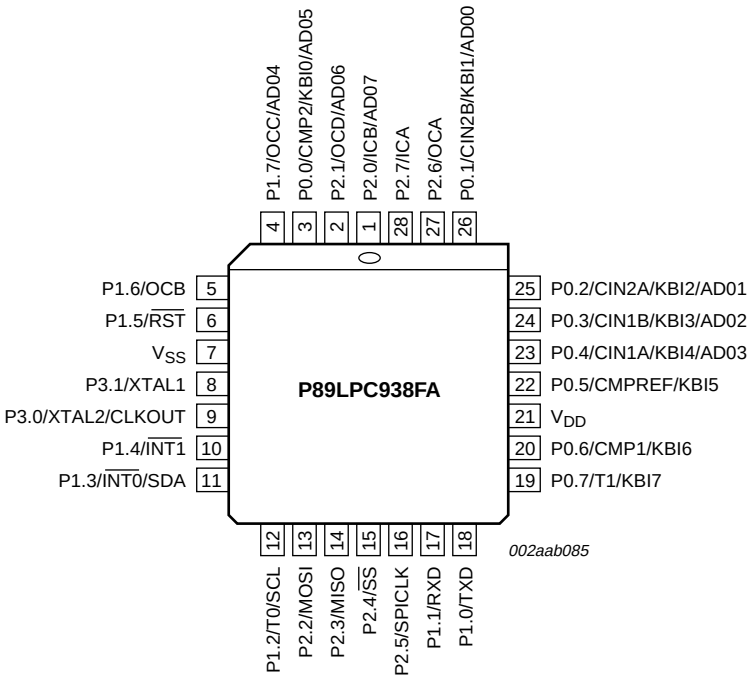

Fig 4. PLCC28 pin configuration.

Table 3: Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP28, PLCC28	HVQFN28		
P0.2/CIN2A/ KBI2/AD01	25	21	I/O	**P0.2 —** Port 0 bit 2.
			I	**CIN2A —** Comparator 2 positive input A.
			I	**KBI2 —** Keyboard input 2.
			I	**AD01 —** ADC0 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD02	24	20	I/O	**P0.3 —** Port 0 bit 3.
			I	**CIN1B —** Comparator 1 positive input B.
			I	**KBI3 —** Keyboard input 3.
			I	**AD02 —** ADC0 channel 2 analog input.
P0.4/CIN1A/ KBI4/AD03	23	19	I/O	**P0.4 —** Port 0 bit 4.
			I	**CIN1A —** Comparator 1 positive input A.
			I	**KBI4 —** Keyboard input 4.
			I	**AD03 —** ADC0 channel 3 analog input.
P0.5/CMPREF/ KBI5	22	18	I/O	**P0.5 —** Port 0 bit 5.
			I	**CMPREF —** Comparator reference (negative) input.
			I	**KBI5 —** Keyboard input 5.
P0.6/CMP1/ KBI6	20	16	I/O	**P0.6 —** Port 0 bit 6.
			O	**CMP1 —** Comparator 1 output.
			I	**KBI6 —** Keyboard input 6.
P0.7/T1/KBI7	19	15	I/O	**P0.7 —** Port 0 bit 7.
			I/O	**T1 —** Timer/counter 1 external count input or overflow output.
			I	**KBI7 —** Keyboard input 7.
P1.0 to P1.7			I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 “Port configurations” and Table 10 “DC electrical characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	18	14	I/O	**P1.0 —** Port 1 bit 0.
			O	**TXD —** Transmitter output for the serial port.
P1.1/RXD	17	13	I/O	**P1.1 —** Port 1 bit 1.
			I	**RXD —** Receiver input for the serial port.
P1.2/T0/SCL	12	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
			I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
			I/O	**SCL —** I^2C serial clock input/output.

Table 4: P89LPC938 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P1*	Port 1	90H	OCC	OCB	$\overline{RST}$	$\overline{INT1}$	$\overline{INT0}$/SDA	T0/SCL	RXD	TXD		[2]
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P2*	Port 2	A0H	ICA	OCA	SPICLK	$\overline{SS}$	MISO	MOSI	OCD	ICB		[2]
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		[2]
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF [2]	11111111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00 [2]	00000000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3 [2]	11x1xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00 [2]	00x0xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF [2]	11111111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00 [2]	00000000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03 [2]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00 [2]	xxxxxx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD	DEEPD	VCPD	ADPD	I2PD	SPPD	SPD	CCUPD	00 [2]	00000000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60 [2] [4]	011xxx00
RTCH	RTC register high	D2H									00 [4]	00000000
RTCL	RTC register low	D3H									00 [4]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial Port data buffer register	99H									xx	xxxxxxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000

Table 4: P89LPC938 Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] The RSTSRC register reflects the cause of the P89LPC938 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] The only reset source that affects these SFRs is power-on reset.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

7.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to '1', enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, The RPE selection is overridden and this pin will always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1);
- Power-on detect;
- Brownout detect;
- Watchdog timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.16.1 Reset vector

Following reset, the P89LPC938 will fetch instructions from either address 0000h or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00h.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC938 User's Manual*). Otherwise, instructions will be fetched from address 0000H.

the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the RTC and its associated SFRs to the default state.

7.19 CCU

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four compare/PWM outputs with selectable polarity
- Symmetrical/Asymmetrical PWM selection
- Two capture inputs with event counter and digital noise rejection filter
- Seven interrupts with common interrupt vector (one Overflow, two Capture, four Compare)
- Safe 16-bit read/write via shadow registers.

7.19.1 CCU Clock (CCUCLK)

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a PLL. The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

7.19.2 CCU clock prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

7.19.3 Basic timer operation

The Timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU Timer may also be used as an 8-bit up/down timer.

7.19.4 Output compare

There are four output compare channels A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

7.19.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input

7.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.20.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

7.20.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.22 SPI

The P89LPC938 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

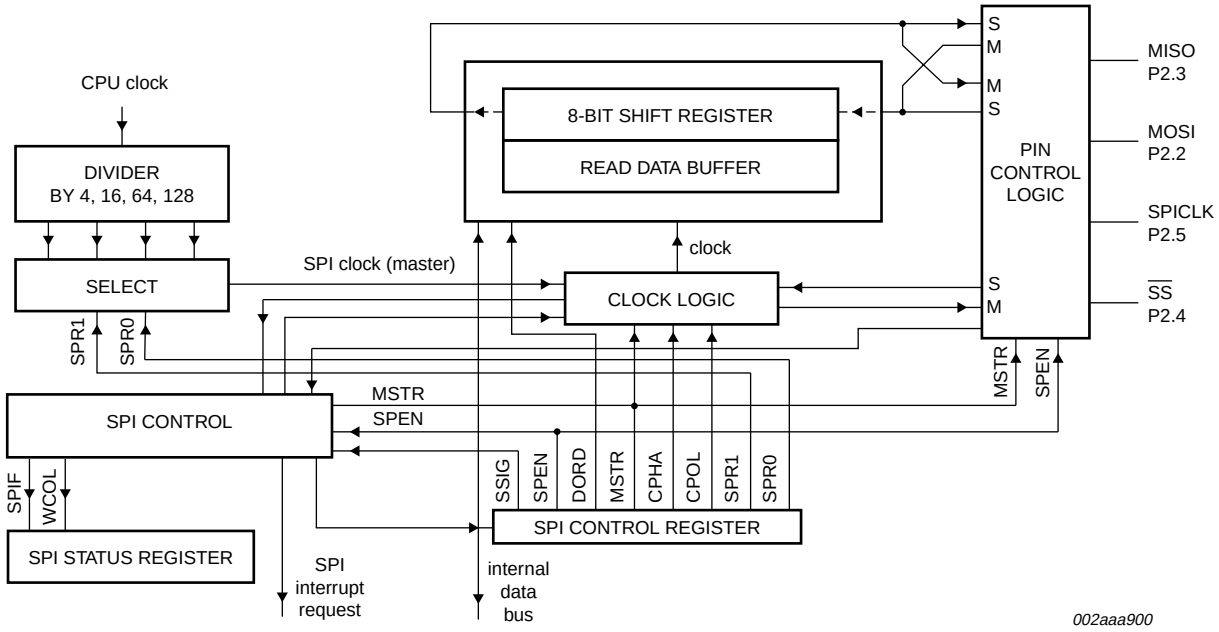

Fig 15. SPI block diagram.

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 16 through Figure 18.

7.22.1 Typical SPI configurations

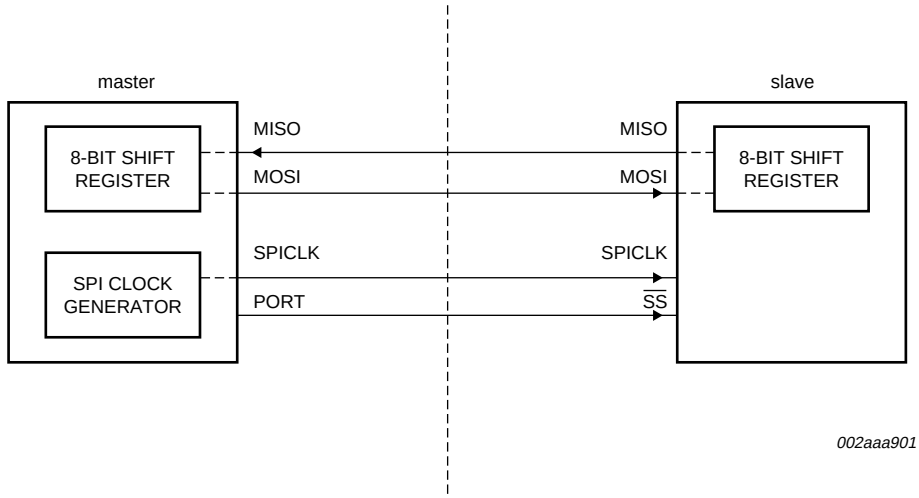

Fig 16. SPI single master single slave configuration.

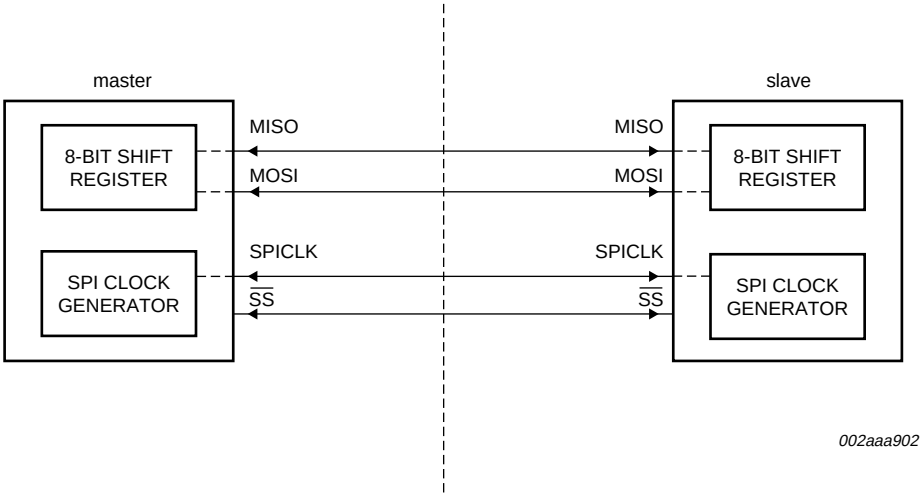

Fig 17. SPI dual device configuration, where either can be a master or a slave.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC938 User's Manual*.

7.28.8 ISP

In-System Programming is performed without removing the microcontroller from the system. The In-System Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC938 through the serial port. This firmware is provided by Philips and embedded within each P89LPC938 device. The Philips In-System Programming facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.28.9 Power-on reset code execution

The P89LPC938 contains two special Flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC938 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H.

Table 8 shows the factory default Boot Vector setting for this device. A factory-provided boot loader is pre-programmed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this boot loader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Table 8: Default Boot Vector values and ISP entry points

Device	Default Boot Vector	Default boot loader entry point	Default boot loader code range	1 kB sector range
P89LPC938	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.28.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC938 User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector (1FH) is changed, it will no longer point to the factory pre-programmed ISP boot loader code. After programming the Flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

after the remaining input channels have been converted. After all selected channels have been converted, the process will repeat starting with the first selected channel. Additional conversion results will again cycle through the eight result register pairs, overwriting the previous results.Continous conversions continue until terminated by the user.

8.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register pair, AD0DAT0R and AD0DAT0L. The result of the conversion of the second channel is placed in result register pair, AD0DAT1R and AD0DAT1L. The first channel is again converted and its result stored in AD0DAT2R and AD0DAT2L. The second channel is again converted and its result placed in AD0DAT3R and AD0DAT3L, etc. An interrupt is generated, if enabled, after every set of four or eight conversions (user selectable).

8.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the eight input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

8.5 Conversion start modes

8.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

8.5.2 Start immediately

Programming this mode immediately starts a conversion.This start mode is available in all A/D operating modes.

8.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

8.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt

9. Limiting values

Table 9: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature range		–65	+150	°C
V_{xtal}	voltage on XTAL1, XTAL2 pin to V_{SS}		-	V_{DD} + 0.5	V
$I_{OH(I/O)}$	HIGH-level output current per I/O pin		-	20	mA
$I_{OL(I/O)}$	LOW-level output current per I/O pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	100	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 9 “Limiting values”

a) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 10 “DC electrical characteristics” and Table 11 “AC characteristics” of this specification are not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

10. Static characteristics

Table 10: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$I_{DD(oper)}$	operating supply current	3.6 V; 12 MHz	[2]	-	14	23	mA
$I_{DD(idle)}$	Idle mode supply current	3.6 V; 12 MHz	[2]	-	5	7	mA
$I_{DD(pd)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2]	-	55	80	µA
$I_{DD(tpd)}$	total Power-down mode supply current	3.6 V	[3]	-	1	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{DDR}	data retention voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; V_{DD} = 2.4 V – 3.6 V, all ports, all modes except Hi-Z	[4]	-	0.6	1.0	V
		I_{OL} = 3.2 mA; V_{DD} = 2.4 V – 3.6 V, all ports, all modes except Hi-Z	[4]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −20 µA; V_{DD} = 2.4 V – 3.6 V; quasi-bidirectional mode, all ports		V_{DD} – 0.3	V_{DD} – 0.2	-	V
		I_{OH} = −3.2 mA; V_{DD} = 2.4 V – 3.6 V; push-pull mode, all ports		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = −20 mA; V_{DD} = 2.4 V – 3.6 V; push-pull mode, all ports		V_{DD} – 1.0	-	-	V
C_{iss}	input capacitance		[5]	-	-	15	pF
I_{IL}	logical 0 input current	V_I = 0.4 V	[6]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}, V_{IH}, V_{th(HL)}$	[7]	-	-	±10	µA
I_{TL}	logical 1-to-0 transition current, all ports	V_I = 1.5 V at V_{DD} = 3.6 V	[8]	−30	-	−450	µA
$R_{RST(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ

Table 11: AC characteristics *...continued*

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified. [1] [2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	3.0 MHz (master)		$^{2}/_{CCLK}$	-	165	-	ns
	2.0 MHz (slave)		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	3.0 MHz (master)		$^{2}/_{CCLK}$	-	165	-	ns
	2.0 MHz (slave)		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 24, 25, 26, 27	100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 26, 27					
	2.0 MHz (slave)		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 26, 27					
	2.0 MHz (slave)		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	2.0 MHz (slave)		-	240	-	240	ns
	3.0 MHz (master)		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

11.1 Waveforms

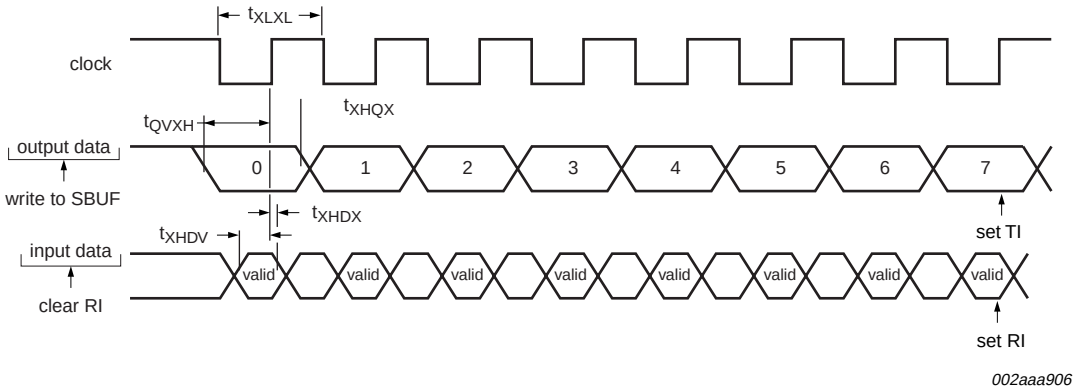

Fig 22. Shift register mode timing.

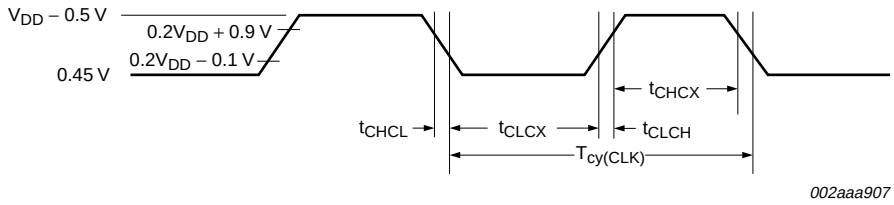

Fig 23. External clock timing.

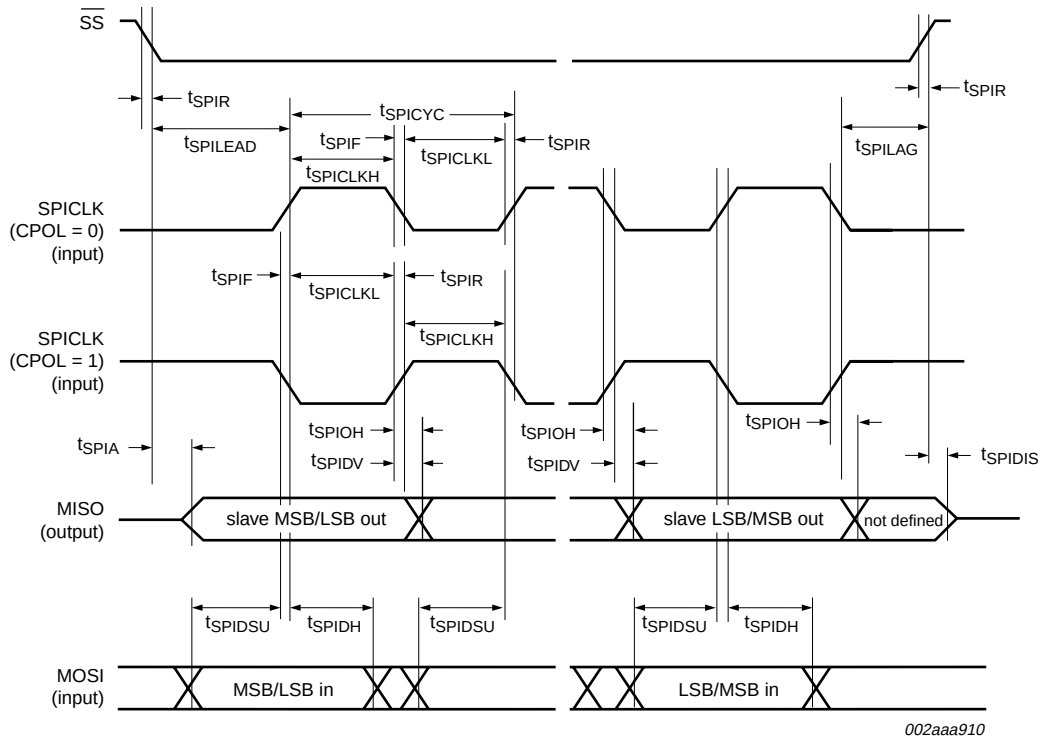

Fig 26. SPI slave timing (CPHA = '0').

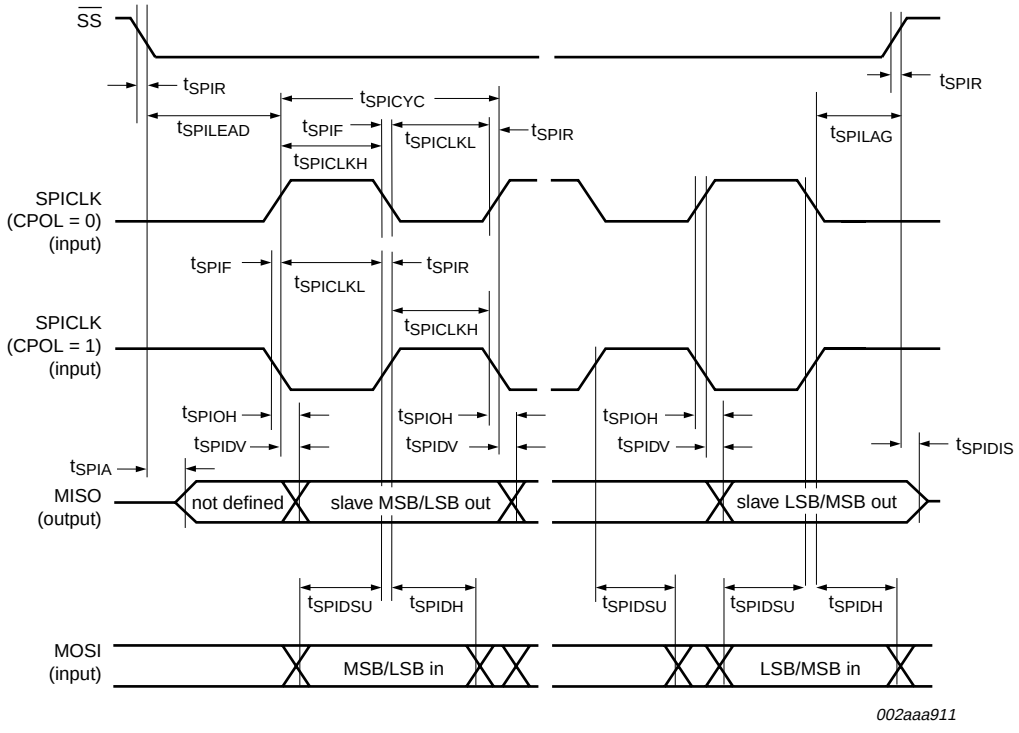

Fig 27. SPI slave timing (CPHA = '1').

12.2 A/D converter electrical characteristics

Table 15: A/D converter electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		V_{SS} − 0.2	-	V_{SS} + 0.2	V
C_{iss}	analog input capacitance		-	-	15	pF
E_D	differential non-linearity		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±1	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±1	%
$E_{u(tot)}$	total unadjusted error		-	-	±2	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	−60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle		111	-	3125	ns
t_{ADC}	conversion time	A/D enabled	-	-	$36T_{cy(ADC)}$	µs

20. Contents

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