What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc130rd2cn

- I^{2}C

    – Up to two sets of I^{2}C device
    – Master/Slave mode
    – Bidirectional data transfer between masters and slaves
    – Multi-master bus (no central master)
    – Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
    – Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
    – Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
    – Programmable clocks allow versatile rate control
    – Support multiple address recognition (four slave address with mask option)

- I^{2}S

    – Interface with external audio CODEC
    – Operate as either master or slave mode
    – Capable of handling 8-, 16-, 24- and 32-bit word sizes
    – Mono and stereo audio data supported
    – I^{2}S and MSB justified data format supported
    – Two 8 word FIFO data buffers are provided, one for transmit and one for receive
    – Generates interrupt requests when buffer levels cross a programmable boundary
    – Support two DMA requests, one for transmit and one for receive

- PS/2 Device Controller

    – Host communication inhibit and request to send detection
    – Reception frame error detection
    – Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
    – Double buffer for data reception
    – S/W override bus

- CAN 2.0

    – Supports CAN protocol version 2.0 part A and B
    – Bit rates up to 1M bit/s
    – 32 Message Objects
    – Each Message Object has its won identifier mask
    – Programmable FIFO mode (concatenation of Message Object)
    – Maskable interrupt
    – Disabled Automatic Re-transmission mode for Time Triggered CAN applications
    – Support power down wake-up function

- EBI (External bus interface) support (100-pin and 64-pin Package Only)

    – Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
    – Support 8-/16-bit data width
    – Support byte write in 16-bit data width mode

- ADC

    – 12-bit SAR ADC with 700K SPS
    – Up to 8-ch single-end input or 4-ch differential input
    – Single scan/single cycle scan/continuous scan
    – Each channel with individual result register
    – Scan on enabled channels
    – Threshold voltage detection
    – Conversion start by software programming or external input

- Support PDMA mode
- Analog Comparator

  - Up to two analog comparator
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake-up

- One built-in temperature sensor with 1℃ resolution

- Brown-Out detector

  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brown-Out Interrupt and Reset option

- Low Voltage Reset

  - Threshold voltage levels: 2.0 V

- Operating Temperature: -40℃~85℃

- Packages:

  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin

3   PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1   NuMicro™ NUC130 Products Selection Guide

3.1.1   NuMicro™ NUC130 Automotive Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	UART	SPI	I²C	USB	LIN	CAN	I²S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
NUC130LC1CN	32 KB	4 KB	4 KB	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130LD2CN	64 KB	8 KB	4 KB	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130LE3CN	128 KB	16 KB	Definable	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130RC1CN	32 KB	4 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130RD2CN	64 KB	8 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130RD3CN	128 KB	16 KB	Definable	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130VE3CN	128 KB	16 KB	Definable	4 KB	up to 80	4x32-bit	3	4	2	-	2	1	1	2	8	8x12-bit	v	v	v	LQFP100

NUC 1 0 0 - X X X X X

ARM-Based 32-bit Microcontroller

CPU core
1:   Cortex-M0
5/7: ARM7
9:   ARM9

Function
0: Advance Line
2: USB Line
3: Automotive Line
4: Connectivity Line

Package Type
Y: QFN 36
L: LQFP 48
R: LQFP 64
V: LQFP 100

Temperature
N: -40℃ ~ +85℃
E: -40℃ ~ +105℃
C: -40℃ ~ +125℃

Reserve

RAM Size
1: 4K
2: 8K
3: 16K

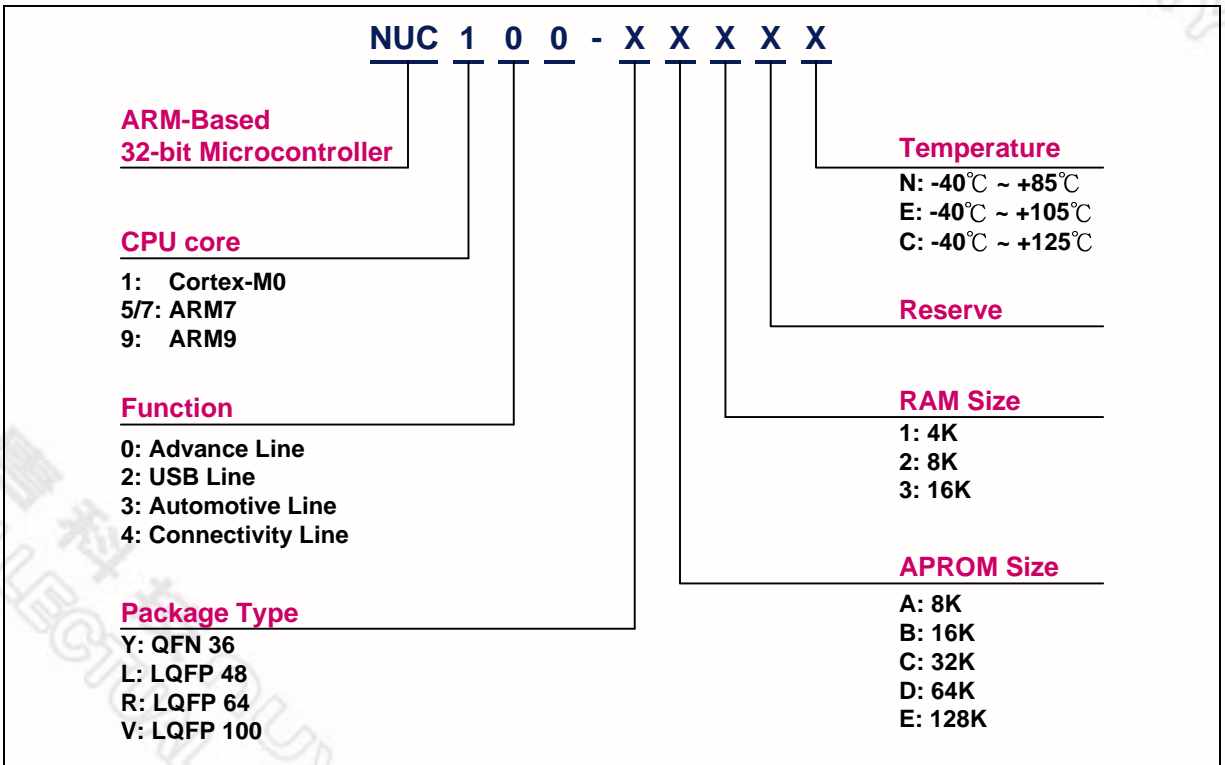**APROM Size**
A: 8K
B: 16K
C: 32K
D: 64K
E: 128K

Figure 3-1 NuMicro™ NUC100 Series selection code

5.2.5 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.6 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.3.6 Frequency Divider Output

This device is equipped a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When write 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When write 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.
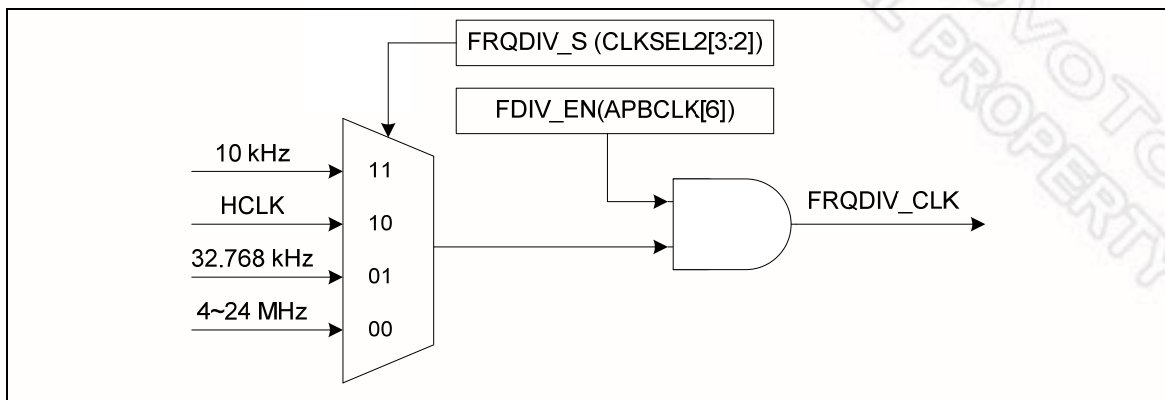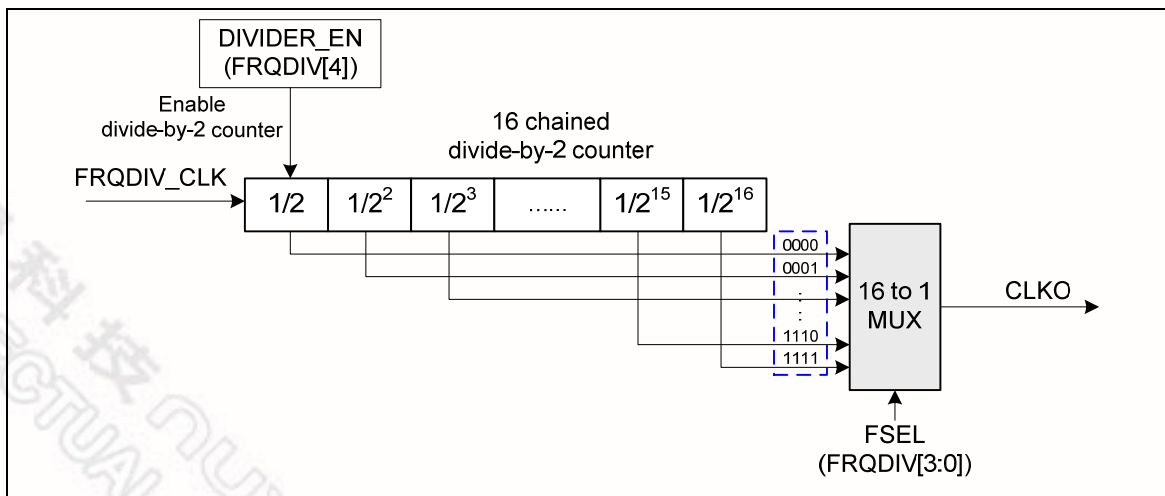

Figure 5-7 Clock Source of Frequency Divider

Figure 5-8 Block Diagram of Frequency Divider

5.6 PWM Generator and Capture Timer (PWM)

5.6.1 Overview

NuMicro™ NUC130/NUC140 has 2 sets of PWM group supports total 4 sets of PWM Generators which can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable dead-zone generators.

Each PWM Generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read

PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900ns ≈ 1000 kHz

5.6.2 Features

5.6.2.1 PWM function features:

- PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.

- Up to 16-bit resolution

- PWM Interrupt request synchronized with PWM period

- One-shot or Auto-reload mode PWM

- Up to 2 PWM group (PWMA/PWMB) to support 8 PWM channels or 4 PWM paired channels

5.6.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators

- Support 8 Capture input channels shared with 8 PWM output channels

- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

5.7 Real Time Clock (RTC)

5.7.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 kHz low speed crystal connected at pins X32I and X32O (reference to pin descriptions) or from an external 32.768 kHz low speed oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). Both RTC Time Tick and Alarm Match can cause chip wake-up from power down mode if wake-up function is enabled (TWKE (TTR[3])=1).

5.7.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time

- Alarm register (second, minute, hour, day, month, year)

- 12-hour or 24-hour mode is selectable

- Leap year compensation automatically

- Day of week counter

- Frequency compensate register (FCR)

- All time and calendar message is expressed in BCD code

- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second

- Support RTC Time Tick and Alarm Match interrupt

- Support wake-up chip from power down mode

5.10 Watchdog Timer (WDT)

5.10.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wake-up chip from power down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals. Table 5-5 show the watchdog timeout interval selection and Figure 5-64 shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * T_{WDT}) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks (T_{RST}) then chip restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wake-up function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]) , the chip is waken up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to wake up from power down state is 2^4 * T_{WDT}. When power down command is set by software, then, chip enters power down state. After 2^4 * T_{WDT} time is elapsed, chip is waken up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to wake up from power down state is 2^{18} * T_{WDT}. If power down command is set by software, then, chip enters power down state. After 2^{18} * T_{WDT} time is elapsed, chip is waken up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is waken up, software should clear the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over 1024 * T_{WDT} , the chip is reset by Watchdog Timer.

5.10.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.

- Selectable time-out interval (2^4 ~ 2^{18}) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).

- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

5.11 UART Interface Controller (UART)

NuMicro™ NUC130/NUC140 provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART, besides, only UART0 and UART1 support flow control function.

5.11.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wake-up status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR) and LIN receiver break field detected interrupt (INT_LIN_RX_BREAK). Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART1~2 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 5-6 lists the equations in the various conditions and Table 5-7 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5-6 UART Baud Rate Equation

System clock = internal 22.1184 MHz high speed oscillator						
Baud rate	Mode0		Mode1		Mode2	
	Parameter	Register	Parameter	Register	Parameter	Register
921600	x	x	A=0,B=11	0x2B00_0000	A=22	0x3000_0016
460800	A=1	0x0000_0001	A=1,B=15 A=2,B=11	0x2F00_0001 0x2B00_0002	A=46	0x3000_002E

5.15 Analog-to-Digital Converter (ADC)

5.15.1 Overview

NuMicro™ NUC100 Series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converters can be started by software and external STADC pin.

5.15.2 Features

- Analog input voltage range: 0~V_{REF}

- 12-bit resolution and 10-bit accuracy is guaranteed

- Up to 8 single-end analog input channels or 4 differential analog input channels

- Maximum ADC clock frequency is 16 MHz

- Up to 700K SPS conversion rate

- Three operating modes

  - Single mode: A/D conversion is performed one time on a specified channel

  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel

  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion

- An A/D conversion can be started by

  - Software write 1 to ADST bit

  - External pin STADC

- Conversion results are held in data registers for each channel with valid and overrun indicators

- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting

- Channel 7 supports 3 input sources: external analog voltage, internal bandgap voltage, and internal temperature sensor output

- Support Self-calibration to minimize conversion error

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD8}		6		mA	V_{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		11		mA	V_{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD10}		3		mA	V_{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I_{DD11}		10		mA	V_{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		2.5		mA	V_{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current Idle Mode @ 50 MHz	I_{IDLE1}		35		mA	V_{DD}= 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		15		mA	V_{DD}=5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		33		mA	V_{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		13		mA	V_{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		10		mA	V_{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		4.5		mA	V_{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE7}		9		mA	V_{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

7.3 AC Electrical Characteristics

7.3.1 External 4~24 MHz High Speed Oscillator
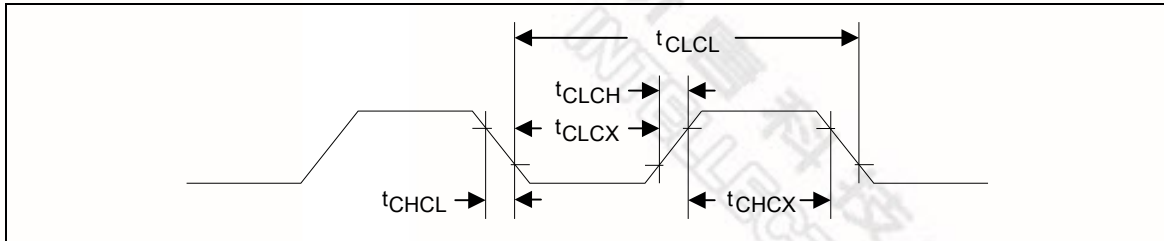
Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

7.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz@ V_{DD} = 5V	-	1	-	mA

7.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without
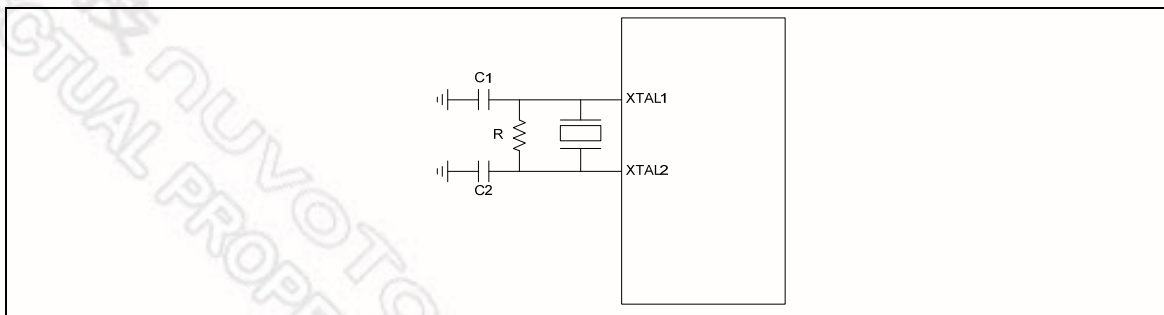
7.4.3　Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD}=5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25℃	1.7	2.0	2.3	V
	Temperature=-40℃	-	2.4	-	V
	Temperature=85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4　Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD}=5.5 V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5　Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
N_{endu}	Endurance		10000			cycles[1]
T_{ret}	Retention time	Temp=25 ℃	100			year
T_{erase}	Page erase time		20		40	ms
T_{mass}	Mass erase time		40	50	60	ms
T_{prog}	Program time		35	40	55	us
V_{dd}	Supply voltage		2.25	2.5	2.75	V[2]
I_{dd1}	Read current				14	mA
I_{dd2}	Program/Erase current				7	mA
I_{pd}	Power down current				10	uA

1. Number of program/erase cycles.
2. V_{dd} is source from chip LDO output voltage.
3. This table is guaranteed by design, not test in production.

7.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI master mode (V_{DD} = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI master mode (V_{DD} = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns
SPI slave mode (V_{DD} = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+19	ns
SPI slave mode (V_{DD} = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns