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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Last Time Buy
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc130ve3cn

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5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Brown-Out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-On Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external crystal circuit and ISPCON.BS bit. System Reset doesn't reset external crystal circuit and ISPCON.BS bit, but Power-On Reset does.

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 2.5 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO and V_{DD33} , require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 5-2 shows the power distribution of NuMicro™ NUC130.

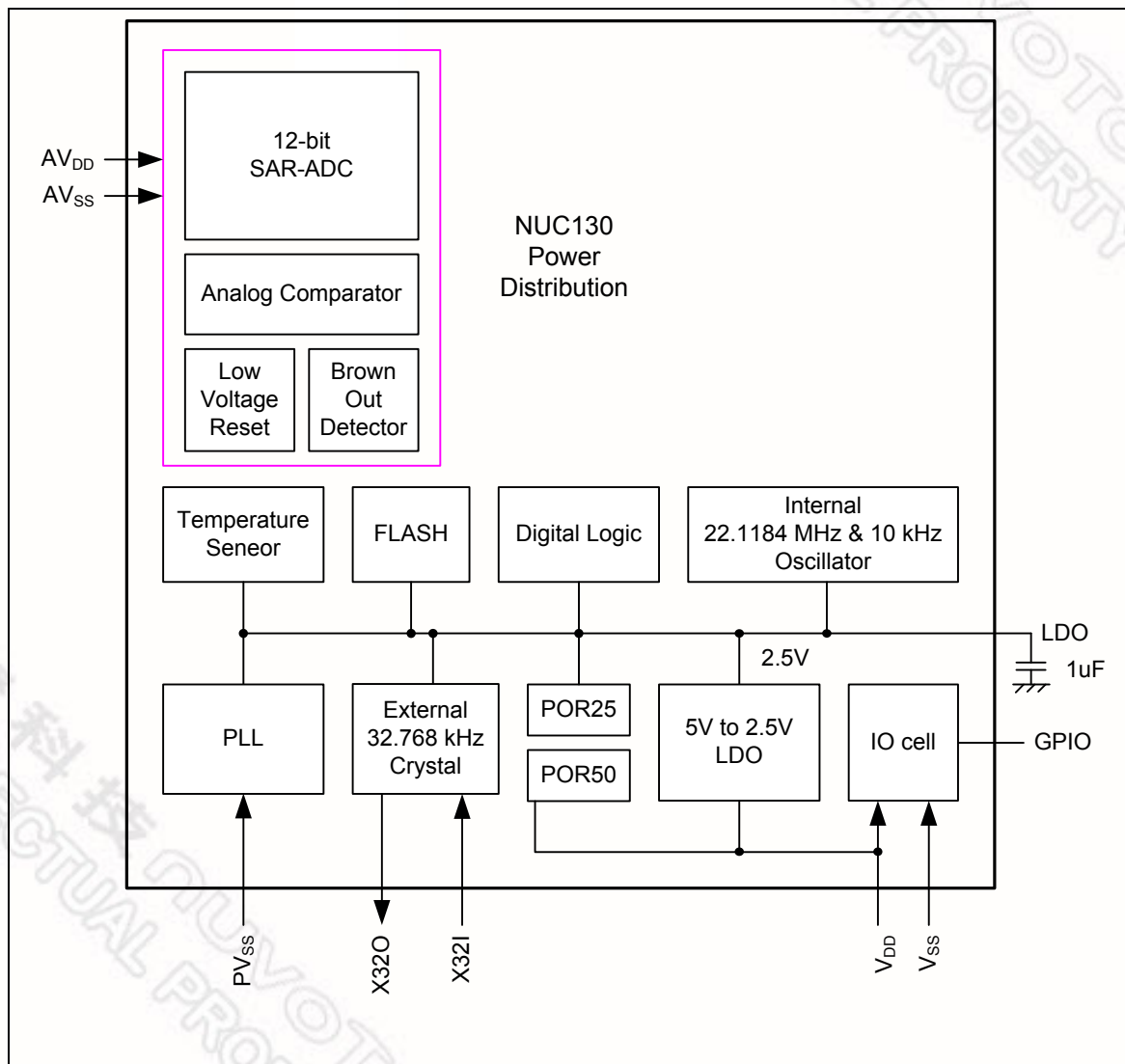


Figure 5-2 NuMicro™ NUC130 Power Distribution Diagram

5.2.4 System Memory Map

NuMicro™ NUC100 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. NuMicro™ NUC100 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6001_FFFF	EXTMEM_BA	External Memory Space (128KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I ² C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers

5.2.5 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

5.3 Clock Controller

5.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter power down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power down mode and wait for wake-up interrupt source triggered to leave power down mode. In the power down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

5.5 I²C Serial Interface Controller (Master/Slave) (I²C)

5.5.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 5-9 for more detail I²C BUS Timing.

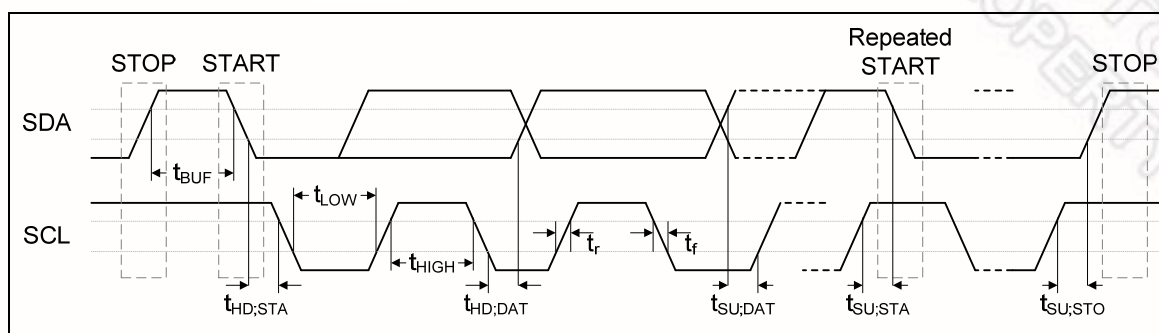


Figure 5-9 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will be $1/900\text{ns} \approx 1000\text{ kHz}$

5.6.2 Features

5.6.2.1 PWM function features:

- PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Up to 2 PWM group (PWMA/PWMB) to support 8 PWM channels or 4 PWM paired channels

5.6.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators
- Support 8 Capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

5.10.2 Features

- 18-bit free running counter to avoid chip from Watchdog timer reset before the delay time expires.
- Selectable time-out interval ($2^4 \sim 2^{18}$) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).
- Reset period = $(1 / 10 \text{ kHz}) * 63$, if WDT_CLK = 10 kHz.

5.13 PS/2 Device Controller (PS2D)

5.13.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

5.13.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

5.16 Analog Comparator (CMP)

5.16.1 Overview

NuMicro™ NUC100 Series contains two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **Error! Reference source not found.**

5.16.2 Features

- Analog input voltage range: 0~5.0 V
- Hysteresis function supported
- Two analog comparators with optional internal reference voltage input at negative end
- One interrupt vector for both comparators

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

7.2 DC Electrical Characteristics

7.2.1 NuMicro™ NUC130/NUC140 DC Electrical Characteristics

($V_{DD}-V_{SS}=3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{OSC} = 50\text{ MHz}$ unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	$V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$ up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	$V_{DD} > 2.7\text{ V}$
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	V_{ref}	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I_{DD1}		51		mA	$V_{DD} = 5.5\text{ V}@50\text{ MHz}$, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		25		mA	$V_{DD} = 5.5\text{ V}@50\text{ MHz}$, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		48		mA	$V_{DD} = 3\text{ V}@50\text{ MHz}$, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		23		mA	$V_{DD} = 3\text{ V}@50\text{ MHz}$, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		19		mA	$V_{DD} = 5.5\text{ V}@12\text{ MHz}$, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		7		mA	$V_{DD} = 5.5\text{ V}@12\text{ MHz}$, disable all IP and disable PLL, XTAL=12 MHz
	I_{DD7}		17		mA	$V_{DD} = 3\text{ V}@12\text{ MHz}$, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I _{DD8}		6		mA	V _{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I _{DD9}		11		mA	V _{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{DD10}		3		mA	V _{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I _{DD11}		10		mA	V _{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I _{DD12}		2.5		mA	V _{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current Idle Mode @ 50 MHz	I _{IDLE1}		35		mA	V _{DD} = 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{IDLE2}		15		mA	V _{DD} = 5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I _{IDLE3}		33		mA	V _{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I _{IDLE4}		13		mA	V _{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I _{IDLE5}		10		mA	V _{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I _{IDLE6}		4.5		mA	V _{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I _{IDLE7}		9		mA	V _{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V _{IH2}	0.7 V _{DD}	-	V _{DD} +0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V _{HY}		0.2 V _{DD}		V	
Input Low Voltage XT1 ^[*2]	V _{IL3}	0	-	0.8	V	V _{DD} = 4.5 V
		0	-	0.4		V _{DD} = 3.0 V
Input High Voltage XT1 ^[*2]	V _{IH3}	3.5	-	V _{DD} +0.2	V	V _{DD} = 5.5 V
		2.4	-	V _{DD} +0.2		V _{DD} = 3.0 V
Input Low Voltage X32I ^[*2]	V _{IL4}	0	-	0.4	v	
Input High Voltage X32I ^[*2]	V _{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V _{ILS}	-0.5	-	0.3 V _{DD}	V	
Positive going threshold (Schmitt input), /RESET	V _{IHS}	0.7 V _{DD}	-	V _{DD} +0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I _{SR11}	-300	-370	-450	μA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR12}	-50	-70	-90	μA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR13}	-40	-60	-80	μA	V _{DD} = 2.5 V, V _S = 2.0 V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I _{SR21}	-20	-24	-28	mA	V _{DD} = 4.5 V, V _S = 2.4 V
	I _{SR22}	-4	-6	-8	mA	V _{DD} = 2.7 V, V _S = 2.2 V
	I _{SR23}	-3	-5	-7	mA	V _{DD} = 2.5 V, V _S = 2.0 V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I _{SK11}	10	16	20	mA	V _{DD} = 4.5 V, V _S = 0.45 V
	I _{SK12}	7	10	13	mA	V _{DD} = 2.7 V, V _S = 0.45 V
	I _{SK13}	6	9	12	mA	V _{DD} = 2.5 V, V _S = 0.45 V
Brown-Out voltage with BOV_VL [1:0] = 00b	V _{BO2.2}	2.1	2.2	2.3	V	
Brown-Out voltage with BOV_VL [1:0] = 01b	V _{BO2.7}	2.6	2.7	2.8	V	
Brown-Out voltage with BOV_VL [1:0] = 10b	V _{BO3.8}	3.6	3.8	4.0	V	
Brown-Out voltage with BOV_VL [1:0] = 11b	V _{BO4.5}	4.3	4.5	4.7	V	
Hysteresis range of BOD voltage	V _{BH}	30	-	150	mV	V _{DD} = 2.5 V~5.5 V

Figure 7-1 Typical Crystal Application Circuit

7.3.3 External 32.768 kHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	°C
V _{DD}	-	2.5	-	5.5	V

7.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} = 5 V	-1	-	+1	%
	-40°C ~ +85°C; V _{DD} = 2.5 V ~ 5.5 V	-3	-	+3	%
Operation Current	V _{DD} = 5 V	-	500	-	uA

7.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} = 5 V	-30	-	+30	%
	-40°C ~ +85°C; V _{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 Specification of 12-bit SARADC

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	±3	-	LSB
INL	Integral nonlinearity error	-	±4	-	LSB
EO	Offset error	-	±1	10	LSB
EG	Gain error (Transfer gain)	-	1	1.005	-
-	Monotonic	Guaranteed			
FADC	ADC clock frequency ($AV_{DD}=5V/3V$)	-	-	16/8	MHz
FS	Sample rate	-	-	700	K SPS
V_{DDA}	Supply voltage	3	-	5.5	V
I_{DD}	Supply current (Avg.)	-	0.5	-	mA
I_{DDA}		-	1.5	-	mA
V_{REF}	Reference voltage	-	V_{DDA}	-	V
I_{REF}	Reference current (Avg.)	-	1	-	mA
V_{IN}	Input voltage	0	-	V_{REF}	V

7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V _{DD} =5.5 V	-	-	5	uA
Temperature	-	-40	25	85	°C
Threshold voltage	Temperature=25°C	1.7	2.0	2.3	V
	Temperature=-40°C	-	2.4	-	V
	Temperature=85°C	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV _{DD} =5.5 V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brown-out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

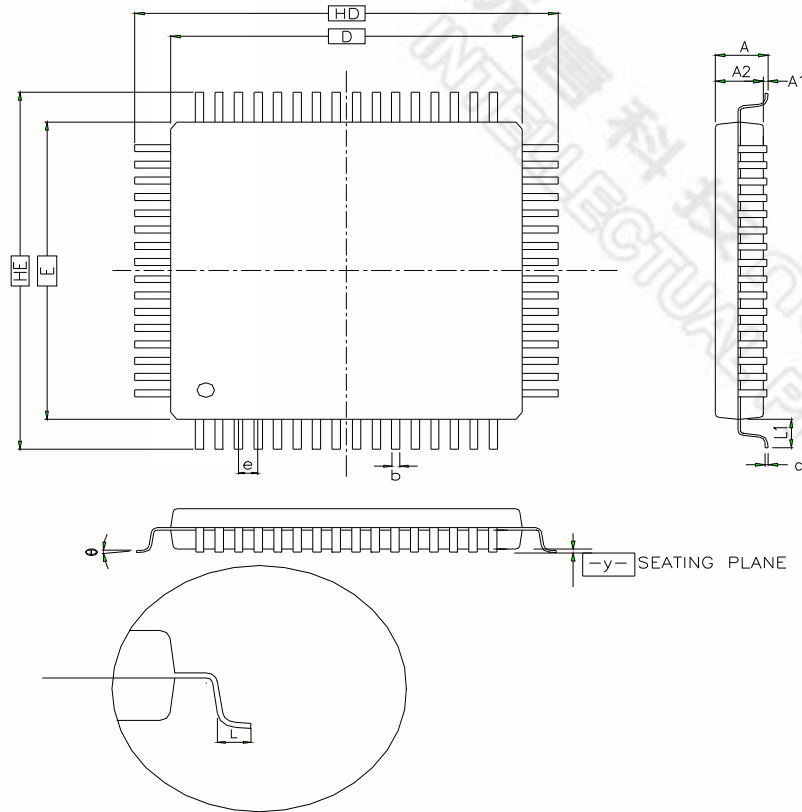
7.4.5 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	V _{in} >reset voltage	-	1	-	nA

7.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI master mode ($V_{DD} = 4.5V \sim 5.5V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI master mode ($V_{DD} = 3.0V \sim 3.6V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns
SPI slave mode ($V_{DD} = 4.5V \sim 5.5V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 4$	-	-	ns
t_V	Data output valid time	-	$2 \cdot PCLK + 11$	$2 \cdot PCLK + 19$	ns
SPI slave mode ($V_{DD} = 3.0V \sim 3.6V$, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	$2 \cdot PCLK + 6$	-	-	ns
t_V	Data output valid time	-	$2 \cdot PCLK + 19$	$2 \cdot PCLK + 25$	ns

8.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A₁	0.002	—	0.006	0.05	—	0.15
A₂	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L₁	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°